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M32C/82,83 Group

Variable-length clocked synchronous serial communication by using Intellingent I/O Group 2

1. Abstract

This application note describes the variable-length clock serial I/O (synchronous serial I/O) operation of Intelligent I/O Group 2.

2. Introduction

This application note is applied to the M32C/83 group microcomputer.

This program can also be used when operating other microcomputers within M16C family, provided they have the same SFR (Special Function Registers) as the M32C/83 group. However, some functions may have been modified. Refer to the User's Manual for details. Use functions covered in this Application Note only after careful evaluation.

3. Detailed description

This application example offers features of the variable-length serial I/O shown in Table 1.

The transmit data is output from pin ISTxD2, and the transfer clock is output from pin ISCLK2. Also the receive data is input from ISRxD2.

Table 1 Clock Synchronous Serial I/O Option Features and Selected Features

Item	Definition	Selection in this example
Transfer clock	Internal Clock	Yes
	External Clock	
Transfer format	LSB First	Yes
	MSB First	
Polarity Selection of pins TxD and RxD	Non Reverse Output	Yes
	Reverse Output	
Transmit Interrupt Factor	When register G2TB becomes empty	
	When the transmission is completed	Yes

(1) Transfer speed definition when using Channel 0

This example uses Channel 0 in the wave generation function. Select "Use the output of the communication function" for this operation. Base Timer is reset when the set value of register G2P00 matches the content of Base Timer. The transfer speed (the period of the transfer clock) is defined by the following equation. Here "fBT2" and "n" represents the count source of Base Timers and value of register G2P00 respectively.

Transfer Speed = fBT2 / {2x(n+2)}

When using in transmitting only, the transfer clock must be 6 divide or greater of Base Timer clock (n=1 or greater).

When using in transmitting and receiving, the transfer clock must be 20 divide or greater of Base Timer clock (n=8 or greater).

For example, when fBT2=30MHz, the max transfer speed is 5Mbps in transmitting and 1.5 Mbps in transmitting and receiving.

(2) How to generate the transfer clock by using Channel 2

This example uses Channel 2 in the phase-delayed waveform output mode of the wave generation function. The set value of register G2P02 must be “(n+2)/2” when register G2P00 is set to “n”.

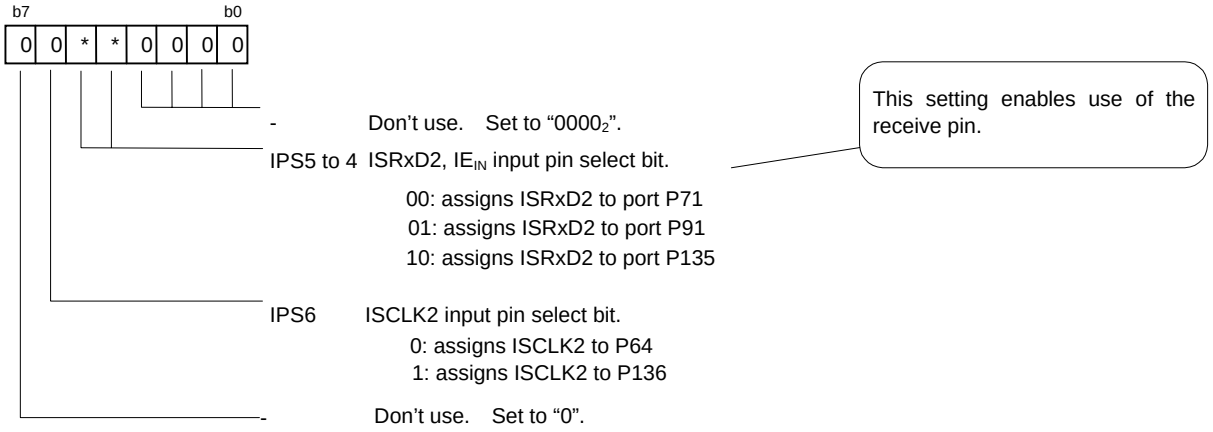
3.1 Register setting

This section shows the setting procedures and setting values to proceeds section “3. Detailed Description”. For detail configuration of each register, please refer to M32C/83 Group HARDWARE MANUAL.

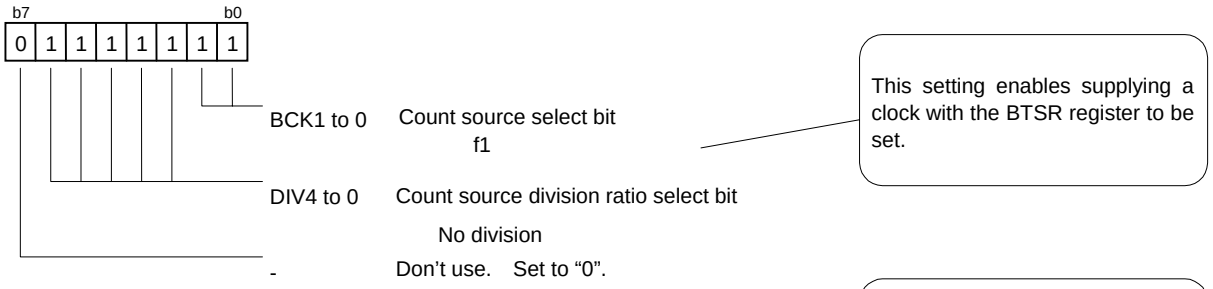
(1) Disabling an Interrupt

Set I flag=0. Or set bits ILV2 to 0=000_2 in register IIOkIC (k=0 to 11) where the interrupt request of the Intelligent I/O is assigned.

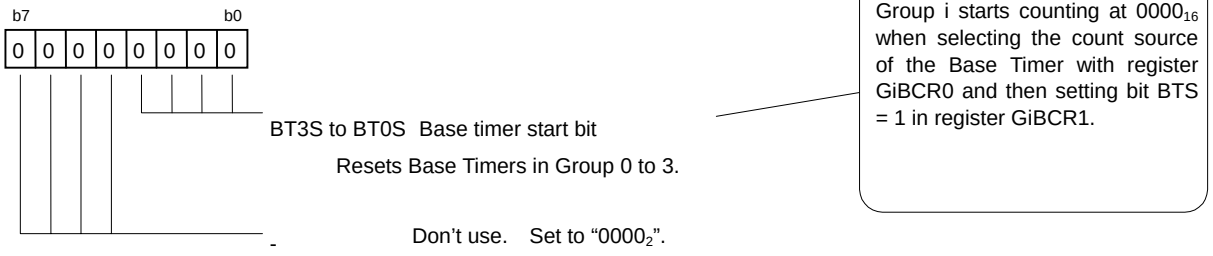
(2) IPS register



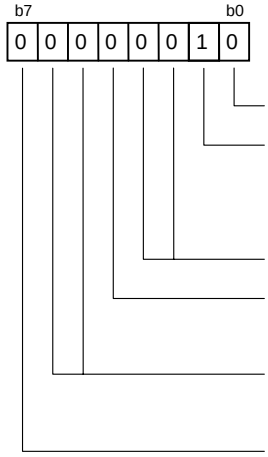
(3) G2BCR0 register



(4) BTSR register



(5) G2BCR1 register



- Don't use. Set to "0".

RST1 — Base timer reset cause select bit 1
Resets the timer by matching the register G2PO0 and base timer

- Don't use. Set to "00_2".

BTS — Base timer start bit
Resets the base timer

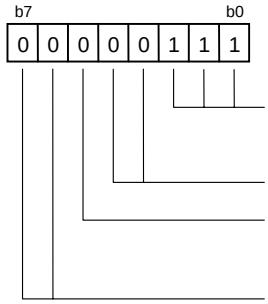
UD1 to 0 — Up-down control bit
Up count mode

- Don't use. Set to "0".

This setting is used to generate a transfer clock. Set the RST1 bit to "1" (reset the Base Timer by matching with G2PO0 register)

Set the bit to "1" (start the Base Timer counting) after setting Group 2 Intelligent I/O related register.

(6) G2POCR0 register



MOD2 to 0 — Operation mode select bit
Uses the output of the communication function

- Don't use. Set to "00_2".

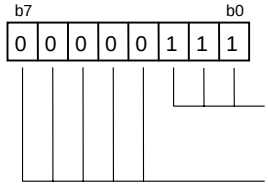
RLD — G2PO0 register value reload timing select bit
Reload when writing

- Don't use. Set to "00_2".

This setting enables the transmit data to be output from the pin ISTxD2.

This setting enables the value in G2PO0 register to be effective after writing to this register.

(7) G2POCR1 register

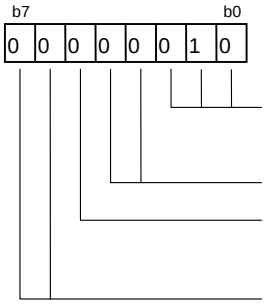


MOD2 to 0 — Operation mode select bit
Uses the output of the communication function

- Don't use. Set to "00000_2".

This setting enables the transfer clock to be output from the pin ISCLK2.

(8) G2POCR2 register



MOD2 to 0 — Operation mode select bit
Selects the phase-delayed waveform output mode

- Don't use. Set to "00_2".

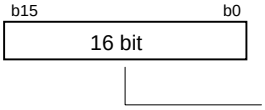
RLD — G2PO2 register value reload timing select bit
Reload when writing

- Don't use. Set to "00_2".

The transfer clock is generated by the phase-delayed waveform output mode.

This setting enables the setting value in the GiPO2 register to be effective after writing to this register.

(9) G2PO0 register

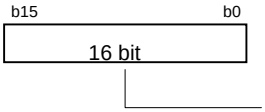


Set the transfer speed

When the setting value is “n”, the transfer speed is as follows.

fBT2 /{2 x (n+2)} n=1 to $FFFD_{16}$

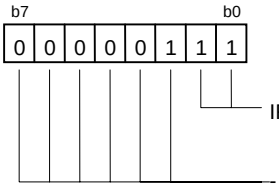
(10) G2PO2 register



Set to “0001_{16}”.

Setting to “0001_{16}” enables the transfer clock to be generated after starting the Base Timer counting in step (12).

(11) G2FE register



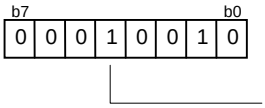
IFE2 to 0 Channel 2 to 0 function enable bit

Enables Channel 2 to 0 to function

Don’t use. Set to “00000_2”.

Set the IFE bit of unused Channel to “0”.

(12) G2BCR1 register

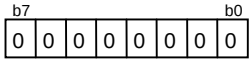


BTS Base timer start bit

Starts counting base timer

Setting the BTS bit to 1 (start the Base Timer counting) enables the transfer clock to be generated.

(13) G2CR register



TE Transmit enable bit

No transmitting

TXEPT Transmit register empty flag

TI Transfer buffer empty flag

- Don’t use. Set to “0”.

RE Receive enable bit

Not receiving

RI Receive complete flag

OPOL ISTxD output parity reverse select bit

Not reversing

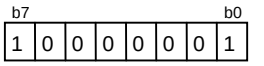
IPOL ISRxD input parity reverse select bit

Not reversing

TI, TXEPT and RI bits are read-only. Write-action to these bits effect nothing.

Transmission and Receive Enable bits must be set after setting the other communication related registers.

(14) G2MR register



GMD1 to 0 Communication mode select bit
Selects clock synchronous serial I/O mode

CKDIR Internal/external clock select bit
Selects internal clock

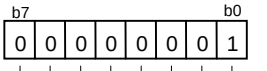
\- Don't use. Set to "000_2".

UFORM Transfer format select bit
Selects LSB first

IRS Transmit interrupt cause select bit
Completes transmit (TXEPT = 1)

Select clock synchronous serial I/O mode.

(15) IIOkIE register (k=5 to6)

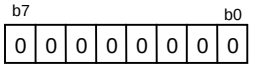


IRLT Interrupt request select bit
Uses interrupt request for an interrupt

Bit 7 to 1 Interrupt enable bit 7 to 1
Set to "0000000_2".

The IRLT bit and bit 7-1 must not be set to "1" at the same time.

(16) IIOkIR register (k=5 to 6)

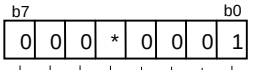


Don't use. Set to "0".

Initializes an interrupt request register

Set IIOkIR register to "00_{16}".
If the register holds a value other than 00_{16}, bit IR in register IIOkIC will not be set to "1" even when an interrupt request is generated. (No interrupt operation possible)

(17) IIOkIE register (k=5 to 6)



IRLT Interrupt request select bit
Uses interrupt request for an interrupt

\- Don't use. Set to "000_2".

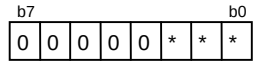
SIO2TE Enables Intelligent I/O Group i transmit interrupt request

SIO2RE Enables Intelligent I/O Group i receive interrupt request

\- Don't use. Set to "000_2".

Set unused interrupt request bit to "0"

(18) IIOkIC register (k=5 to 6)



ILVL2 to 0 Interrupt priority level select bit
Selects interrupt priority level

IR Interrupt request bit
No interrupt request

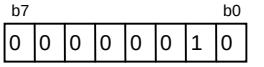
- Don't use. Set to "000_2".

(19) PSC register, PSLa register (a=0,1), PSb register (b=0,1,7)

Set the ISTxD2, ISCLK2 pin.

(20) Enabling an interrupt (I flag ="1")

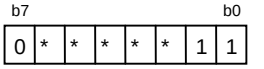
(21) G2BCR1 register



BTS Base timer start bit
Resets the base timer

Reset the Base Timer to set fBT2.

(22) G2BCR0 register



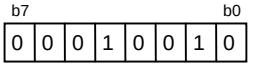
BCK1 to 0 Count source select bit
f1

DIV4 to 0 Count source division ratio select bit
Select a division ratio to be used.

- Don't use. Set to "0".

Set fBT2.

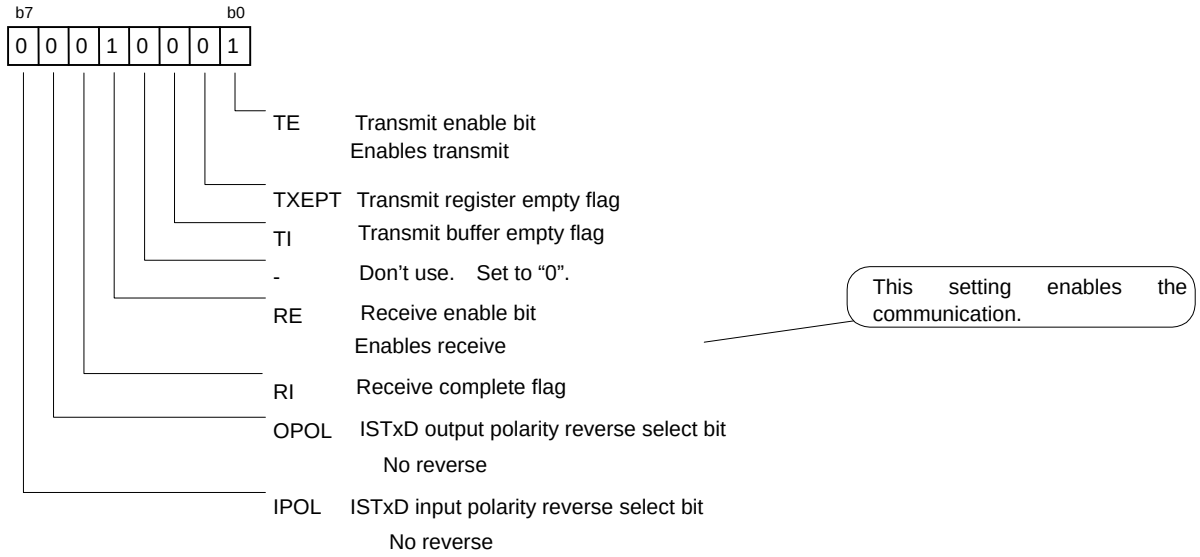
(23) G2BCR1 register



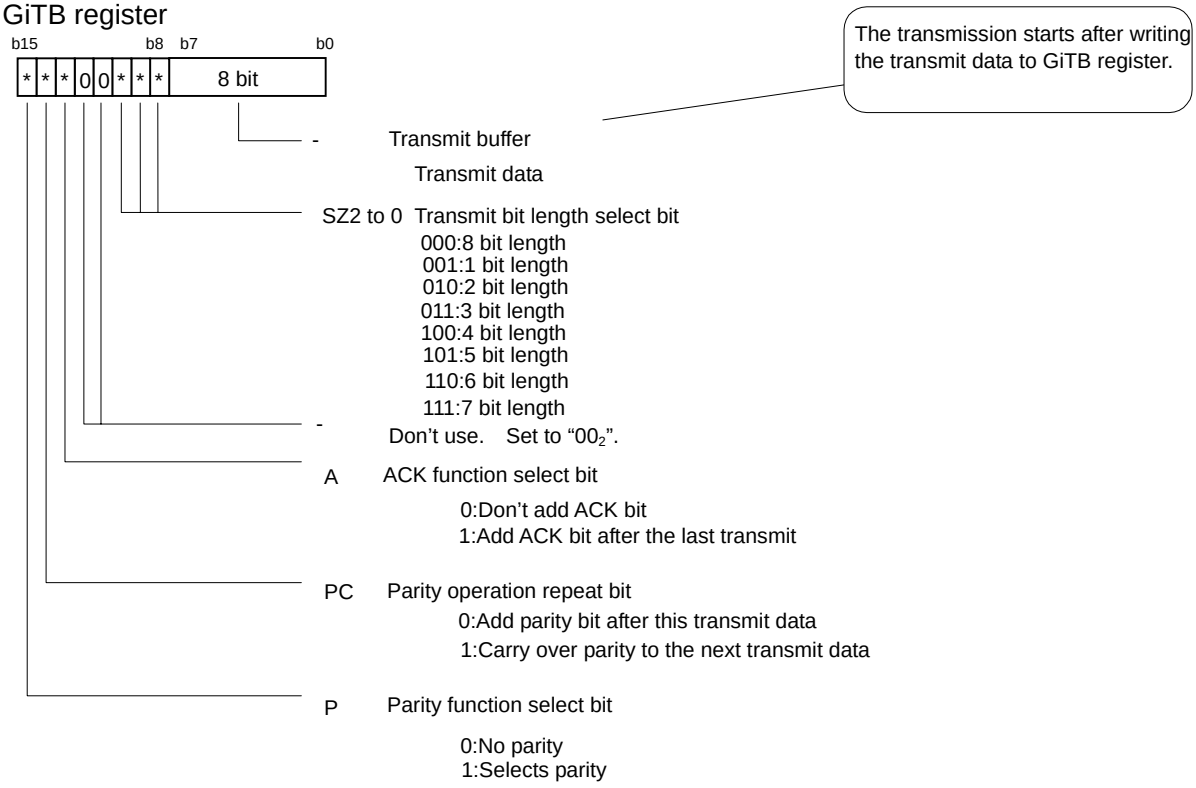
BTS Base timer start bit
Starts base timer counting

Start the Base Timer counting.

(24) G2CR register



(25) GiTB register

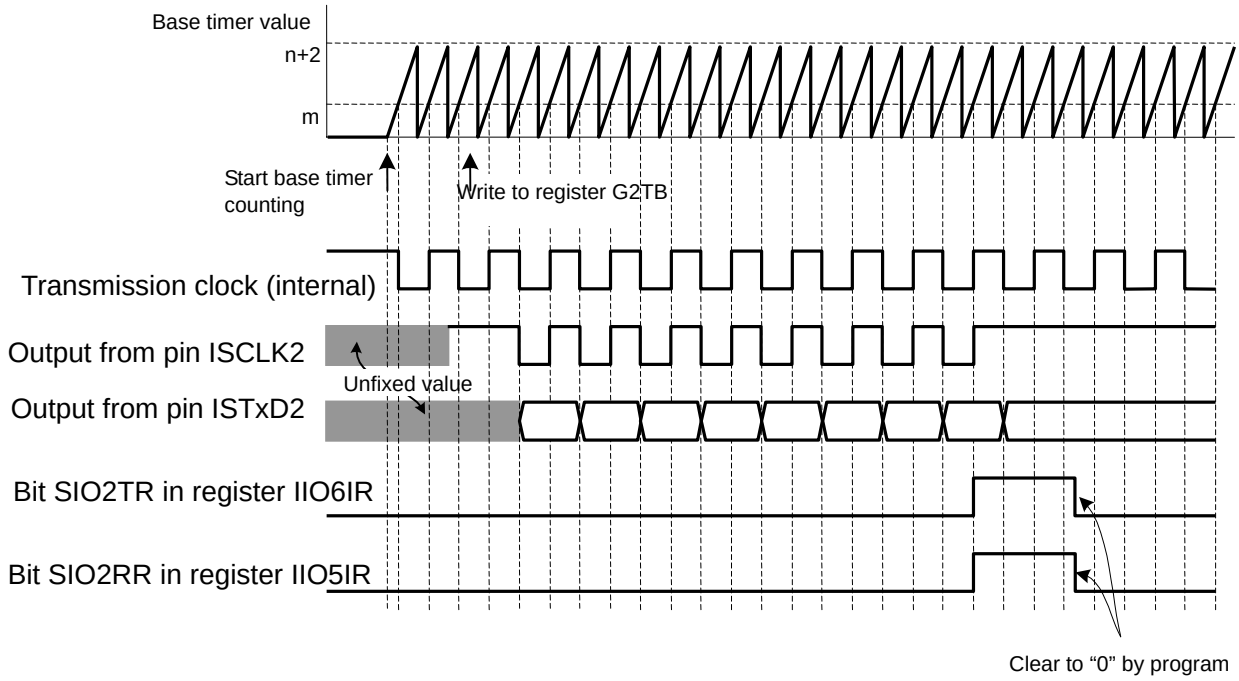


3.2 Precaution on Interrupts

You must clear register II0kIR to 00_{16} during the respective interrupt routine. If you skip this procedure, bit IR in register II0kIC will not be set to “1” when the respective Intelligent I/O generates the interrupt request, resulting in no interrupt being invoked.

3.3 Timing Diagram

The following time chart shows the serial I/O operation in this example.



n: setting value of G2PO0

m: setting value of G2PO2

4. The example of a reference program

```
/************************************************************/
/*  FILE NAME : rej05b0396_src.c                            */
/*  Version   : 1.00                                        */
/*  FUNCTION  :Variable-length clocked synchronous */
/*  serial communication  by using Intelligent I/O Group 2  */
/************************************************************/
/******************************/
/*    include file            */
/******************************/
#include <stdio.h>
#include "sfr32c83.h"

/******************************/
/*    Function difinition     */
/******************************/
void receive_int(void);
#pragma INTERRUPT receive_int
void trans_int(void);
#pragma INTERRUPT trans_int


/******************************/
/*    Global Variable Definition          */
/******************************/
static char rec_buff;
static unsigned short send_bits = 0;

/******************************/
/*    main Function           */
/******************************/
void main(void){
    _asm(" fclr  i");           /*  Disable the interrupt  */

    /*  main clock set     */
    prc0 = 1;                   /*  protect off  */
    mcd = 0x12;                 /*  main clock : no division    */
    prc0 = 0;                   /*  protect on  */
    ips = 0x00;                 /*  assigns ISRxD2 to P71  */

    /*  base clock initial set  */
    g2bcr0 = 0x7f;              /*  Supply clock with BTSR register  */
                                /*  b0,b1: count source f1
                                    b2 to b6 : count source division ratio : No division */
    btsr = 0x00;                /*  Reset the base timer  */
    g2bcr1 = 0x02;

    /*  iio group0 initial set  */
    g2pocr0 = 0x07;             /*  ISTxD2 select  */
    g2pocr1 = 0x07;             /*  ISCLK2 select  */
    g2pocr2 = 0x02;             /*  tarnsmit clock */

    g2po0 = 1000-2;             /*  BRG = fTB / [(998+2)*2]  */
    g2po2 = 1;

    g2fe = 0x07;                /*  ch0 ch1 ch2 enable  */
    g2bcr1 = 0x12;              /*  Start the base timer counting  */

    g2cr = 0x00;                /*  Disable the communications    */
    g2mr = 0x81;                /*  Clocked synchronous serial, LSB first  */
```

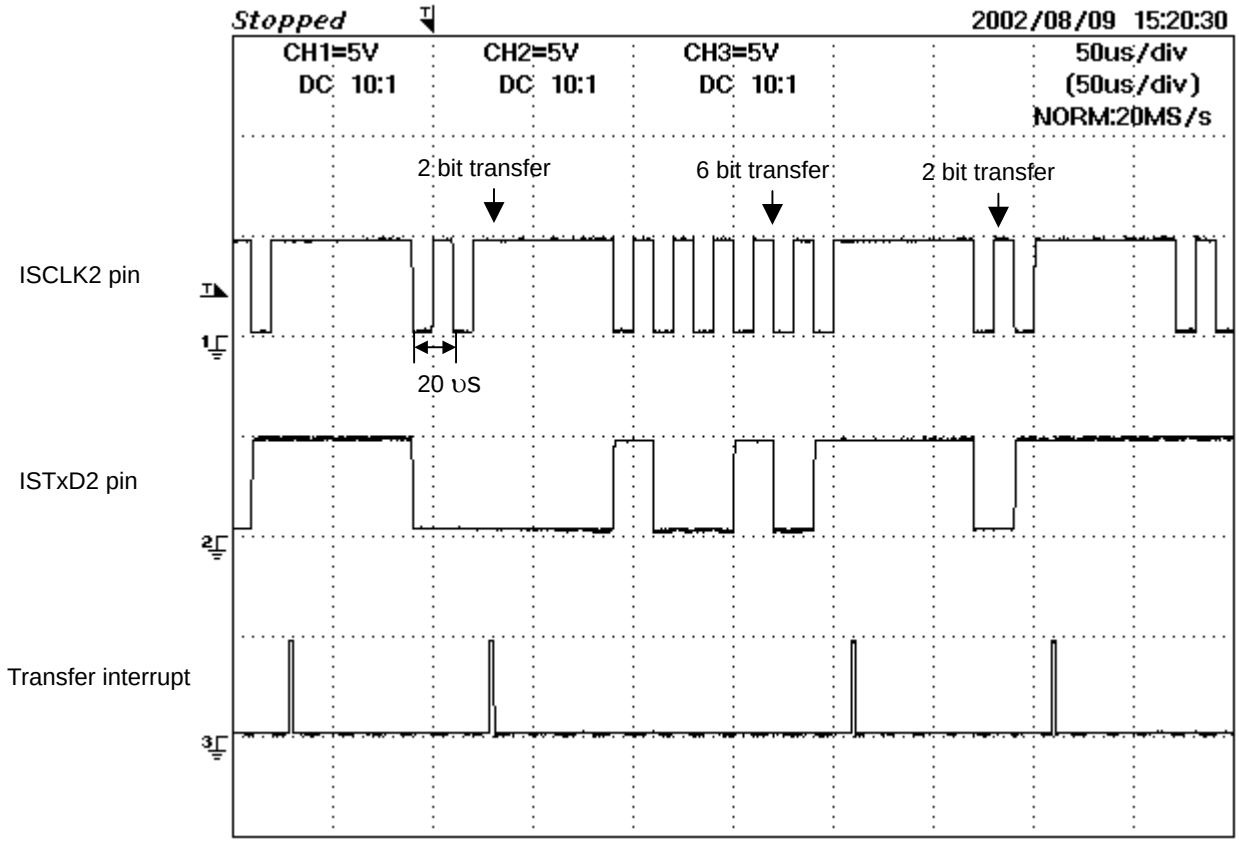
```
    /*   iio group0 interrupt initial set   */

    iio5ie = 0x01;              /*   Use the interrupt request for an interrupt     */
    iio6ie = 0x01;              /*   Use the interrupt request for an interrupt     */
    iio5ir = 0x00;
    iio6ir = 0x00;
    iio5ie = 0x11;              /*   Enable interrupt to gr1 sio receive    */
    iio6ie = 0x11;              /*   Enable interrupt to gr1 sio trans      */
    iio5ic = 0x03;              /*   Select interrupt priority level    */
    iio6ic = 0x03;              /*   Select interrupt priority level    */

    /*   port set   */
    psc = 0x01;
    psl1 = 0x00;
    psl0 = 0x10;
    ps1 = 0x01;
    ps0 = 0x10;
    psl0 = 0x10;
    ps0 = 0x10;
    /* interrupt enable     */
    _asm("fset      i");

    /*   sio initial setting   */
    g2bcr1 = 0x02;              /*   Start the base timer counting    */
    g2bcr0 = 0x7f;              /*   b0,b1: count source f1
                                      b2to b6: count source division ratio : No division */

    g2bcr1 = 0x12;              /*   Start the base timer counting    */
    g2cr = 0x11;                /*   transmit / receive     */

    g2tb = 0x0200;              /*   2Bit Write the transmit data    */

    while(1);
}
/*   iio   interrupt     */
void receive_int(void){
    iio5ir = 0x00;              /*   Clear interrupt request    */
    rec_buff = g2rb;            /*   Receive the transmit data    */
}

void trans_int(void){
    int wait;
    static char send_data;

    iio6ir = 0x00;              /*   Clear interrupt request    */
    send_data ++;

    /*   Change the transmit data length */
    if(send_bits == 0x600){
        send_bits = 0x200;
    }else{
        send_bits = 0x600;
    }

    /* Weight to measure with oscilloscope is usually unneeded.   */
    for(wait=0; wait < 2000; wait ++);

    g2tb = send_bits + send_data;     /*   Write the transmit data    */
}
/*------------------------------ end program */
```

5. Example Waveform and Result

The transmit clock is output from a pin ISCLK2 (P64) and the transmit data is output from a pin ISTxD2 (P70) by using the Intelligent I/O Group 2.

Conditions: Supply voltage = 5V,
Main clock (Xin) = 10MHz
Base Timer Count Source (fBT2) = 30MHz (f1 no division)

Transmission speed : 50kbps (10MHz / 200 : register G2P00 value = 98) → 20 μ / bit



Measurement result from oscilloscope

6. Reference

HADWARE MANUAL

Refer to the M32C/ 83 group HARDWARE MANUAL.

7. Web-site and contact for support

Renesas Web-site

http://www.renesas.com

Contact for Renesas technical support

Mail to : support_apl@renesas.com

REVISION HISTORY

Rev.	Issue date	Revised	
		Page	Point
1.00	Jan 30, 2004	-	First edition issued
1.01	Sep.16,2004	2, 4	Inverted waveform output mode → phase-delayed waveform mode

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