NEC

Application Note

V850ES/Jx3 and Jx3-L

32-Bit Single-Chip Microcontrollers

Software LCD Control

µPD70F3735 µPD70F3740 µPD70F3745
µPD70F3736 µPD70F3741 µPD70F3746
µPD70F3737 µPD70F3742
µPD70F3738 µPD70F3743
µPD70F3739 µPD70F3744

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Chapter 1 Introduction

This document is intended for users who understand the V850ES/Jx3 and V850ES/Jx3-L functions and who design application systems using these products.

Nowadays a lot of industrial applications include LCD displays, thanks to their low power consumption, particularly in measurement and metering applications.

This application note has been written to provide sample code and to give the users an idea of how to control by software a basic LCD module using NEC Electronics' 32-bit microcontroller V850ES/Jx3 and V850ES/Jx3-L.

The software has been developed to run on the V850ES/JJ3 target board, available under the order code QB-V850ESJJ3-TB, wherein the μPD70F3746GJ microcontroller is used. Any other Jx3 or Jx3-L microcontroller can be used, in that case, only the port used to interface the LCD and the pin numbers must be reconsidered.

This Application Note also includes an overview and an application example of sending data from a PC to the board using an RS232 serial communication (via the UART peripheral) and displaying those data on the LCD.

Moreover, V850ES/Jx3-L benefits from pin and functional compatibility to both previous generations of the V850 All Flash range such as V850ES/Jx2, enabling an easy upgrade path to power optimised designs, as well as sister devices from the current generation such as the new V850ES/Jx3 which offers even higher performance and Flash sizes up to 1MB on-chip.

Chapter 2 Hardware Realization

This chapter describes the hardware to interface the LCD module to the V850ES/JJ3 microcontroller, and also deals with serial communication using one of the on-chip UART peripherals.

2.1 LCD Module

In this example, a standard 16x4 Alphanumeric LCD module is connected to the V850ES/JJ3 microcontroller.

The picture below shows the internal block diagram of the LCD module used, which includes the LCD Controller/Driver, the 16x4 LCD display and the LED backlight.

Since the LCD interface is a parallel port, ideally, both the LCD and the MCU would operate on the same voltage level to meet the absolute maximum electrical ratings and provide equal logic levels on the data and control lines of the interface ($V_{LCD} = V_{DD}$, where $V_{SS} = 0V$). We will see afterwards that in this example, that condition is not fulfilled as $V_{LCD} = 5V$ and $V_{DD} = 3V$ (Where V_{DD} is the operating power supply voltage of the microcontroller).

Block diagram
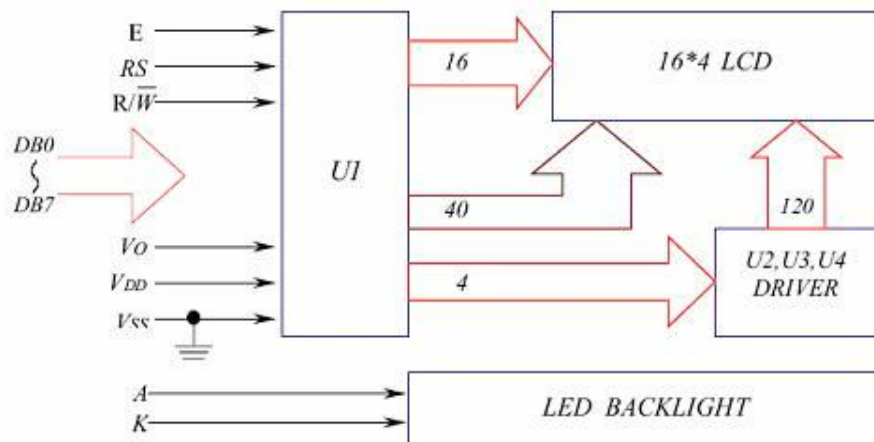
Display data address charts

Character	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
LINE 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
LINE 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
LINE 3	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
LINE 4	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F

Figure 2-1   LCD block diagram and address charts

2.2 Interface Between V850ES/JJ3 and the LCD Module

The operating power supply voltage (V_{DD}) range of V850ES/JJ3 is from 2.85 to 3.3V. For the realization of this application note, the circuit has been designed using the V850ES/JJ3 target board, where the operating supply voltage is strictly equal to 3.3V.

However the logic of the LCD module operates at 5V, as the majority of the standard LCD modules. Nevertheless, one of the benefits of the V850ES/JJ3 as well as all other NEC Electronics' V850ES based microcontrollers operating on up to 3.3V is the I/Os that are tolerant to 5V input. Moreover, the minimum input voltage (V_{IH}) of the LCD module used is 2.2V, therefore, no level shifter between the microcontroller and the LCD module is required to adapt the level of the voltages.

The schematic on Figure 2-3, showing the connections between the LCD and the microcontroller, consists of a connection between the 8 data pins of the LCD module and the 8-bit port PDH of V850ES/JJ3. The three command pins of the LCD module (RS, R/W and E) are connected to the pins 0 to 2 of the 4-bit port PCD.

Regarding the LCD module (Figure 2-2), we supply it with 5V between V_{DD} and V_{SS}, and we connect V_0 to a potentiometer in order to control the contrast of the display, as you can see on the schematic below. In our case, $V_{DD} - V_0$ is also the driving voltage of the LCD controller included in the LCD module.

In the case that the LCD module has got a backlight, a simple current limiting resistor is required to limit the LED current, I_{LED}, to 60mA.
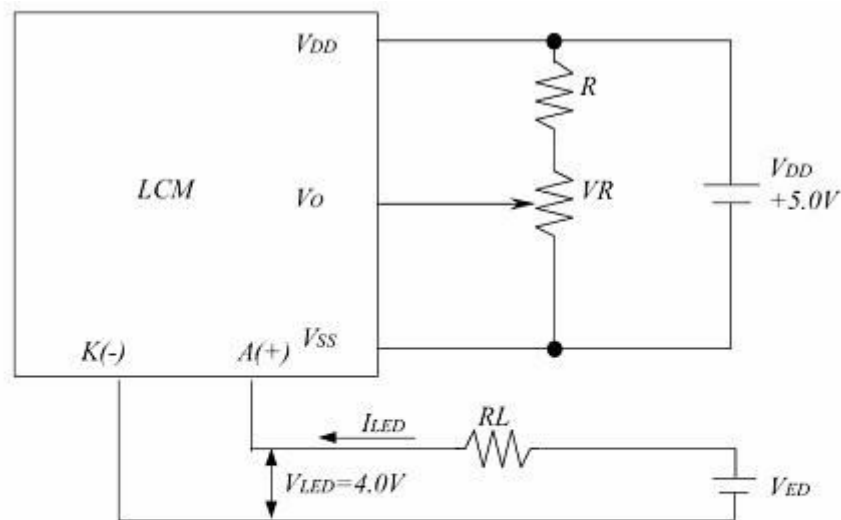
RECOMMENDED RESISTOR R: $V_{DD} - V_0 \geq 1.5V$
$RL \geq ((V_{ED} - 4.0V) / I_{LED})$, $I_{LED} \leq 60mA$
$V_{DD} - V_0$: LCD DRIVING VOLTAGE
VR: $10K\Omega \sim 20K\Omega$
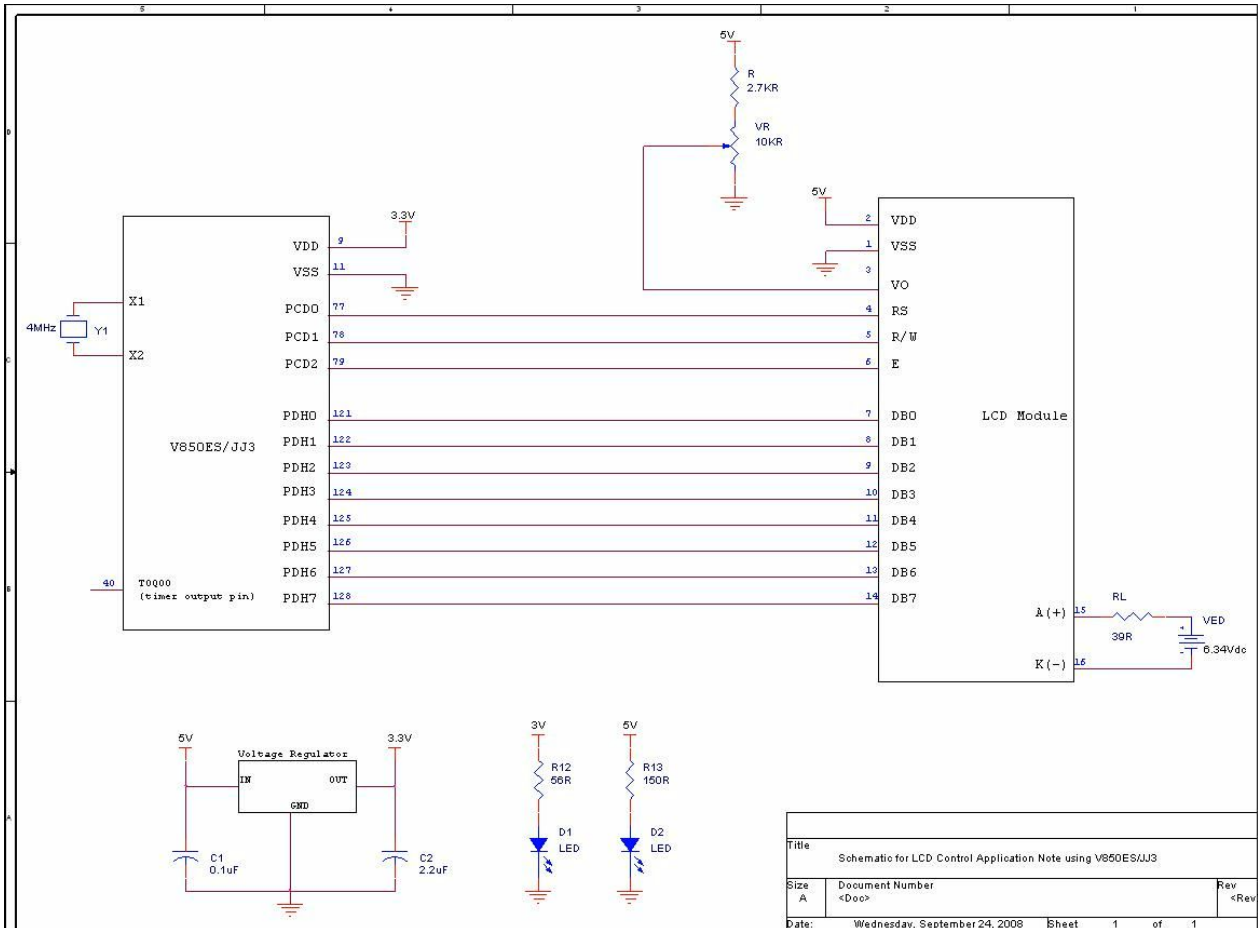
Figure 2-2   LCD circuit diagram

Figure 2-3   Gobal circuit diagram

2.3 Internal Peripheral Functions to be Used

The following internal peripheral hardware of the microcontroller shown below is used in this sample program:

- 16-bit timer Q: TMQ0 for the delay function
- Output port: PDH (8 pins needed) for LCD data signals
- Output port: PCD (3 pins needed) for LCD command signals
- Output port: PCM3 for LED01 on target board
- Asynchronous Serial Interface A: UARTA0

To summarize, we need 11 I/Os from 2 different ports for the LCD interface, TMQ0 16-bit timer which operates as interval timer for implementing system time. Finally, we utilize UARTA0 function to enable RS232 communication between the microcontroller and a PC.

2.4 UART Schematic

We also provide an example of how to implement RS232 communication between the microcontroller, still interfaced to the LCD module, and a PC serial port.

Basically, we need a MAX232 transceiver to make the conversion from an RS-232 serial port to signals suitable for use in TTL compatible digital logic circuits. This

device is design for RS-232 communication interface where ± 12V supplies are not available. It converts the + 5V input to the ± 10V (or 12V) required for RS-232 levels. The MAX232 has to be connected to only four 0.1µF capacitors to provide the required voltage level.

For RS232 communication, only pin 2, pin 3 and pin 5 of the DB-9 connectors are used. The board sends data using pin 3 and receives data using pin 2. That's why pins 2 and 3 of the two ends must be crossed. Pin 5 of the two nodes must be shorted as it represents the common ground. The remaining pins are not used in this project.

On the microcontroller side, the TXDA0 pin is connected to pin 3 of the DB-9 connector using to send data, while the RXDA0 pin is connected to pin 2 using to receive data.

Then, a RS232 serial cable with DB-9 connectors is used to provide the communication between a PC and the board with the microcontroller.
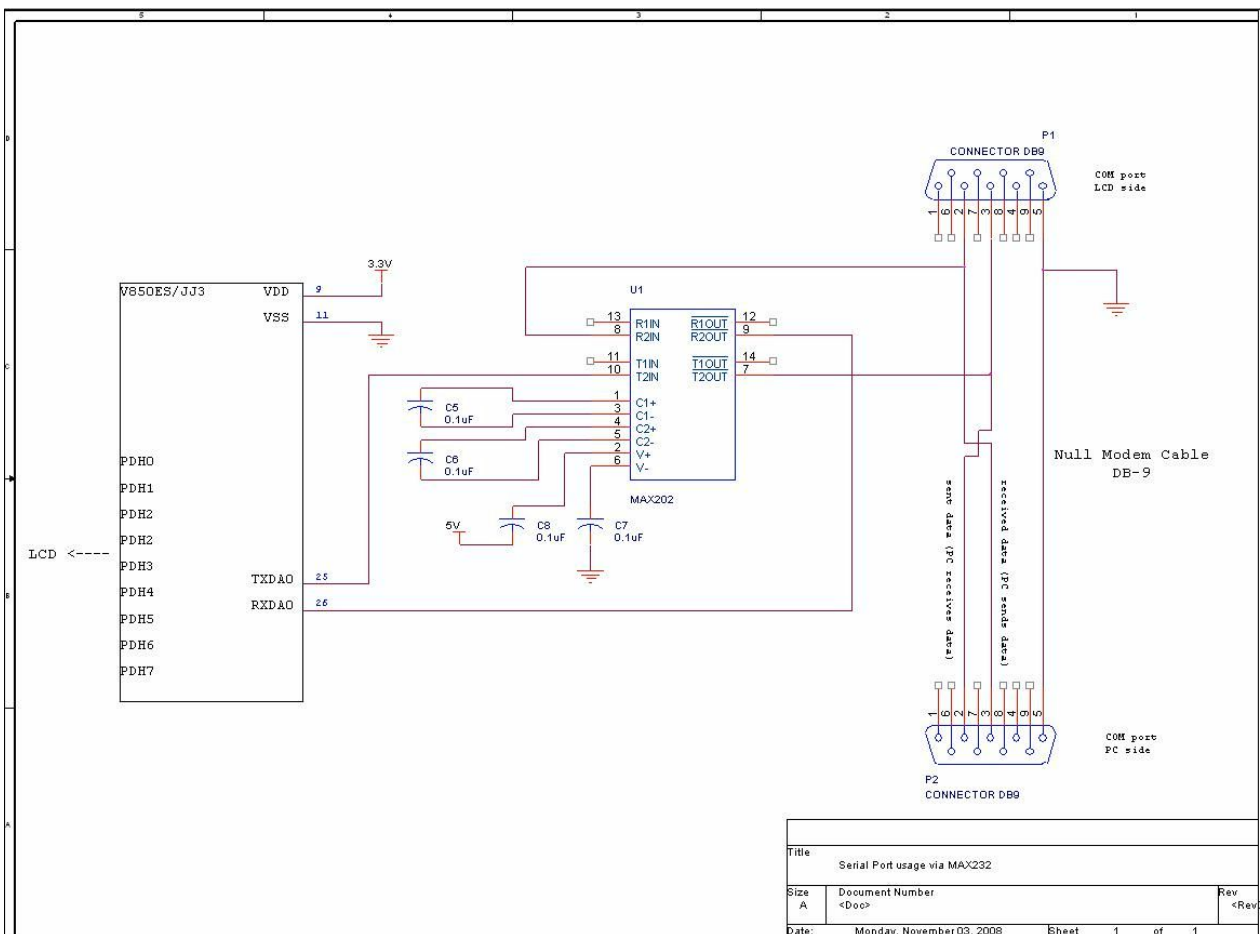
Figure 2-4   Circuit diagram for UART interface

Chapter 3 Software Realization

This chapter describes the software, including initial settings and operation overview of the sample program, and the related flowcharts.

3.1 Initial Contents

The main contents of the initial settings are as follows:

- Enabling the main clock oscillator
- Setting of the CPU clock frequency to fastest speed (f_{XX} = 4 MHz) (4 MHz crystal)
- Stopping watchdog timer operation
- Setting of the 16-bit timer Q (TMQ0)
- Setting of the count clock to $f_{XX}/8$ (500 KHz), setting the operation mode to the interval timer mode, enabling the timer output from TOQ00
- Setting of the UARTA channel 0 (including the setting of TXDA0 and RXDA0 pins)
- Enabling INTTQ0CC0 interrupt
- Setting of the I/O ports for LCD

PORT / PIN	LCD pin	Description
PDH.0 / Pin 121	DB0	Data
PDH.1 / Pin 122	DB1	Data
PDH.2 / Pin 123	DB2	Data
PDH.3 / Pin 124	DB3	Data
PDH.4 / Pin 125	DB4	Data
PDH.5 / Pin 126	DB5	Data
PDH.6 / Pin 127	DB6	Data
PDH.7 / Pin 128	DB7	Data
PCD.0 / Pin 77	RS	Register Select signal
PCD.1 / Pin 78	R/W	Read/Write signal
PCD.2 / Pin 79	E	Enable signal
PCM.3 / Pin 88	-	LED01 on target board

The delay is set using the 16-bit timer TMQ interrupt (INTTQ0CC0) that occurs every millisecond.

3.2 Program Description

The example code is split into three different levels. The first level consists of the low level routines handling the LCD interface that describe the communication between the LCD pins and the V850ES/JJ3 ports (lcd_interface.c).

Then, we have the medium level routines in which we are using a circular buffer to store data before sending it to the LCD module (DispDrv.c).

Finally, there is the high level part which is basically the main program. This main program consists of an endless loop that displays a scrolling string, this is just an example.

The circular buffer stores two types of information, either a command or data. There is also a flag which defines what type of data to be sent (0 for command - which is the address - or 1 for data).

The LCD display is updated by looking at the circular buffer's content. When the read pointer of the circular buffer is different to the write pointer, this means that some data are available to display and must be read.
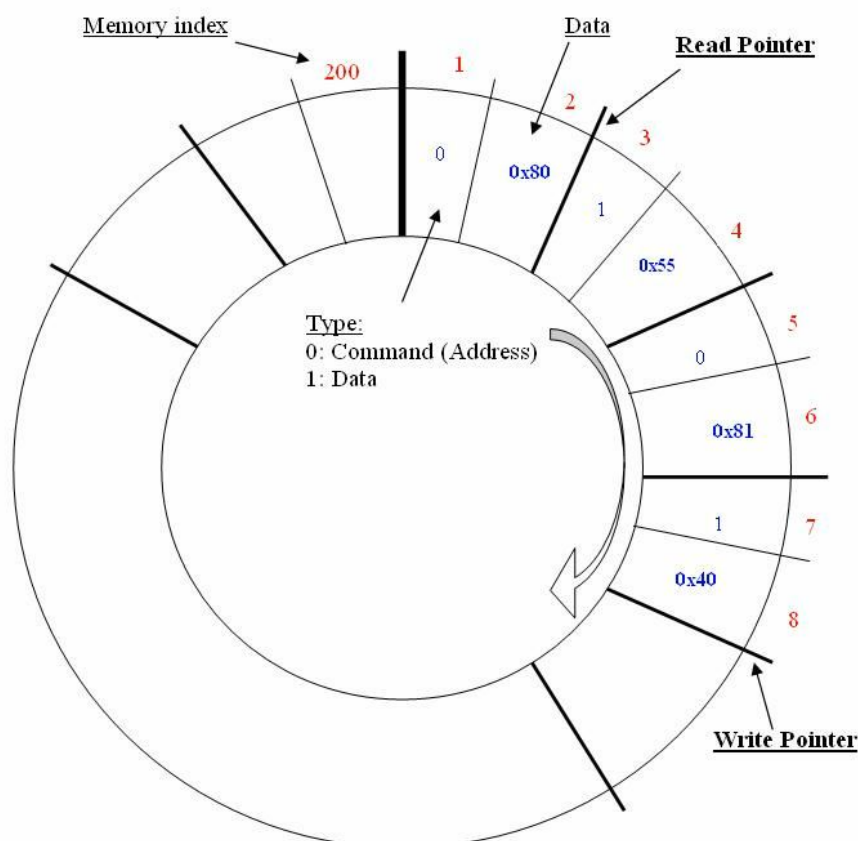
Figure 3-1   Circular buffer diagram

3.3 UART Implementation

The UART peripheral is configured for the baud rate of 9600 bits per second to transmit data with 1 start bit, 8 data bits, no parity, and 1 stop bit. The same sample program has also enabled reception.

By writing to the UARTA0 Control Register 0 (UA0CTL0), global UARTA0 operation is enabled, as well as transmission and reception operations with 1 start bit, 8 data bits, no parity, and 1 stop bit. The baud rate of 9600 is selected by writing to the UARTA0 Control Register 2 (UA0CTL2).

The multiplexed port 3.0 for transmitting data (P30/TXDA0) and port 3.1 for receiving data (P31/RXDA0) are set to UARTA0 mode by writing to the PMC3 and PFC3 registers.

With transmission enabled, writing an 8-bit value to the transmit data register (UA0TX) begins transmission of that value. Once the transmit data is written to the UA0TX register, it is transferred from the UA0TX register to the UARTA0 transmit shift register for serial transmission. The transmission enable interrupt request signal (INTUA0T) is then generated and the interrupt flag (UA0TIF) is set. The program detects when transmission is completed by polling this interrupt flag.

In the reception enabled status, receive data is transferred from the UARTA0 receive shift register to the receive data register (UA0RX) in synchronization with the completion of shift-in processing of 1 frame. Transfer to the UA0RX register also causes the reception complete interrupt request signal (INTUA0R) to be output, and the interrupt flag (UA0RIF) to be set. The program detects when reception is completed by polling this interrupt flag.

To transmit data, the sample code is using a temporary transmission buffer to store data before transmitting to the transmit data register, UA0TX.

The main program continuously transmits the string "V850ES/JJ3 \n\r" at intervals of 200 ms.

3.4 Software Flowcharts

This section describes some key program flowcharts like the main function and peripheral initialisations.
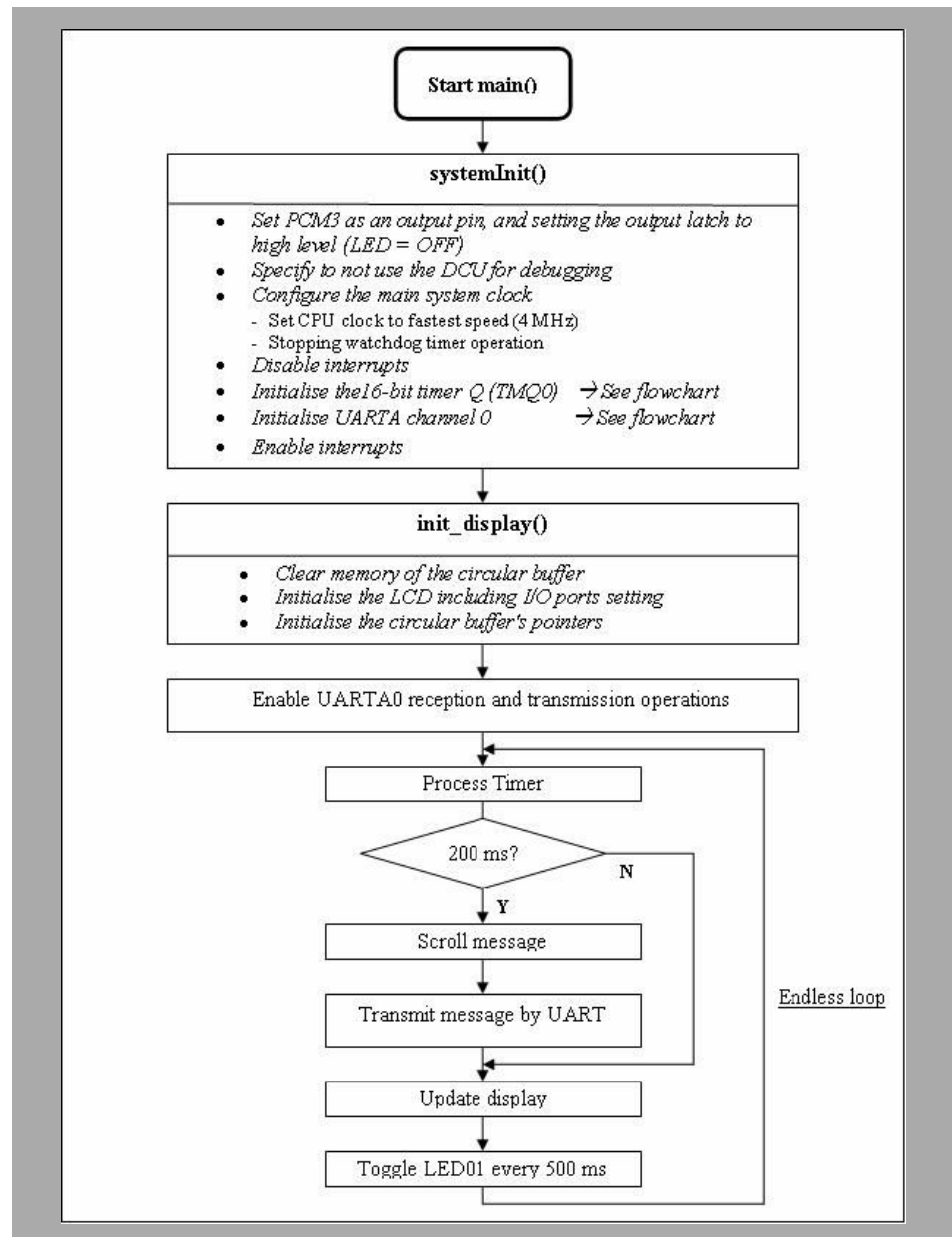
3.4.1 Main Program

Figure 3-2   Flowchart of the main function
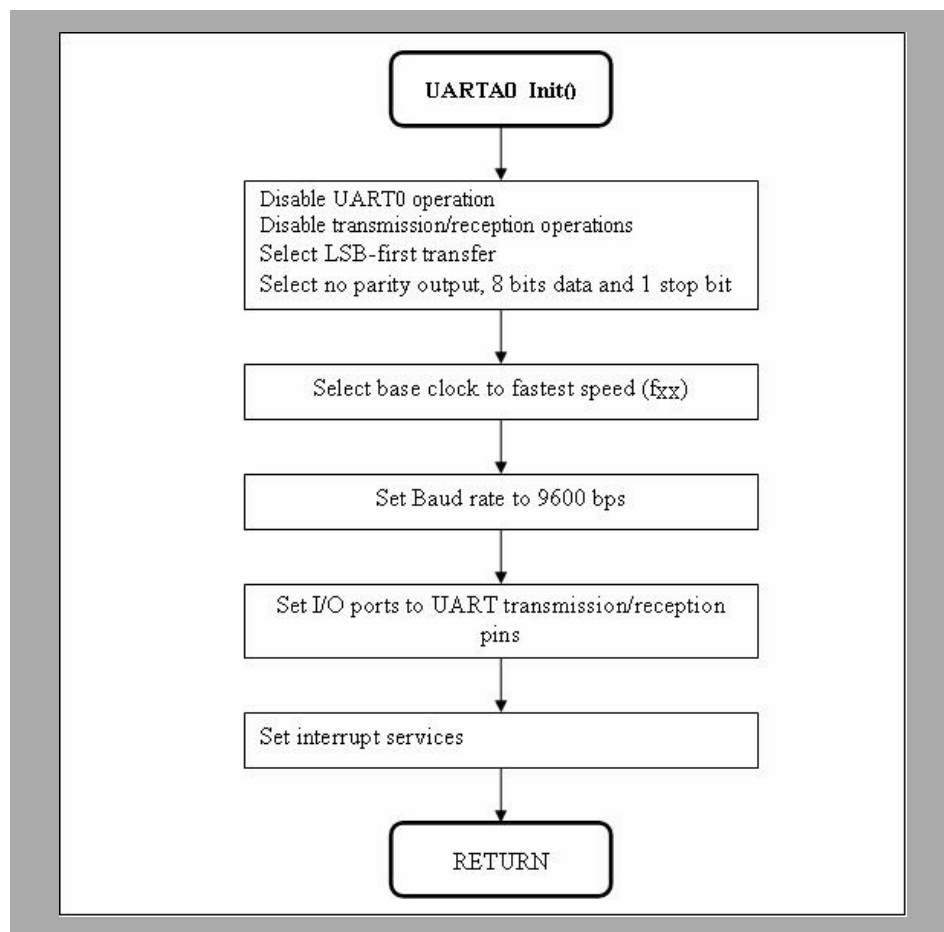
3.4.2 UARTA0 Initialisation

Figure 3-3   Flowchart of the UARTA0 initialisation function
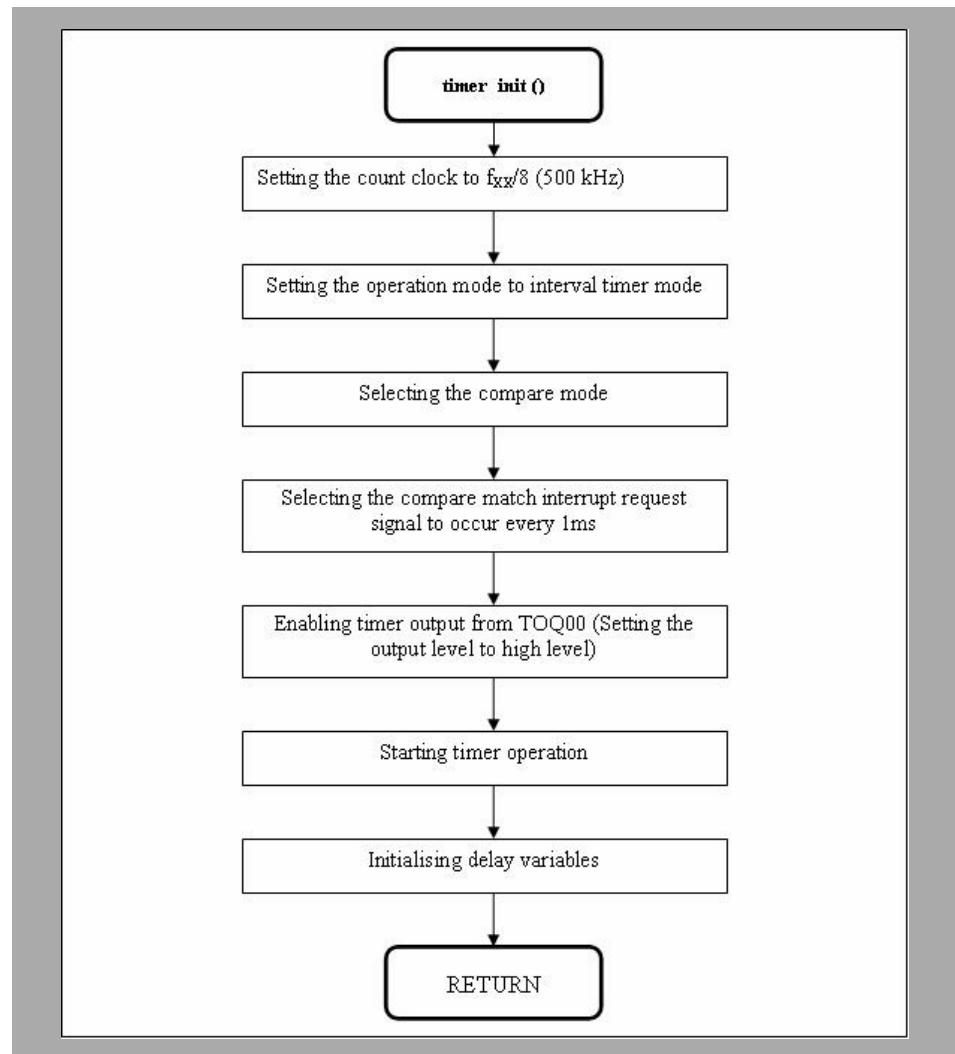
3.4.3   Timer Q Initialisation

Figure 3-4   Flowchart of the Timer Q initialisation function
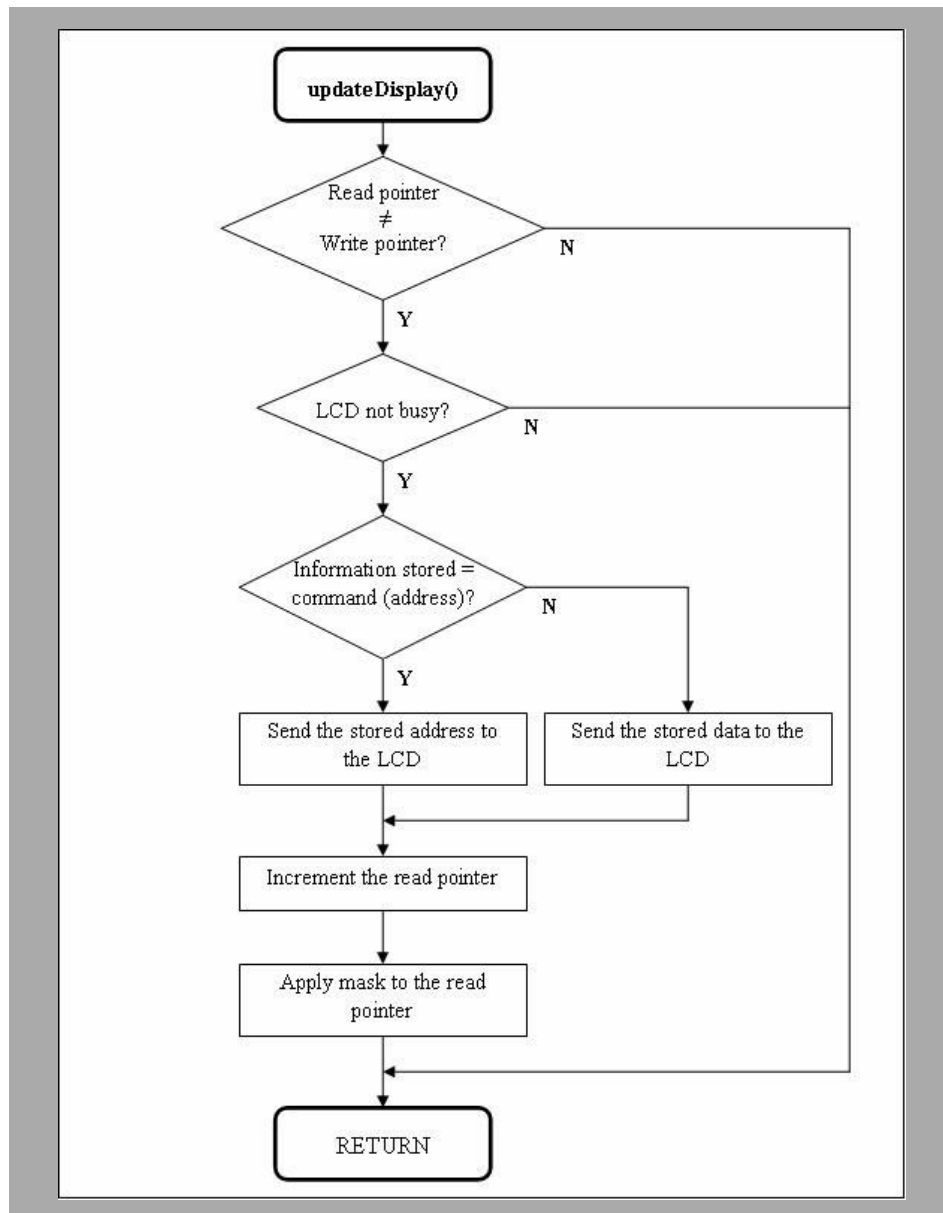
3.4.4 Update Display Function

Figure 3-5   Flowchart of the update display function

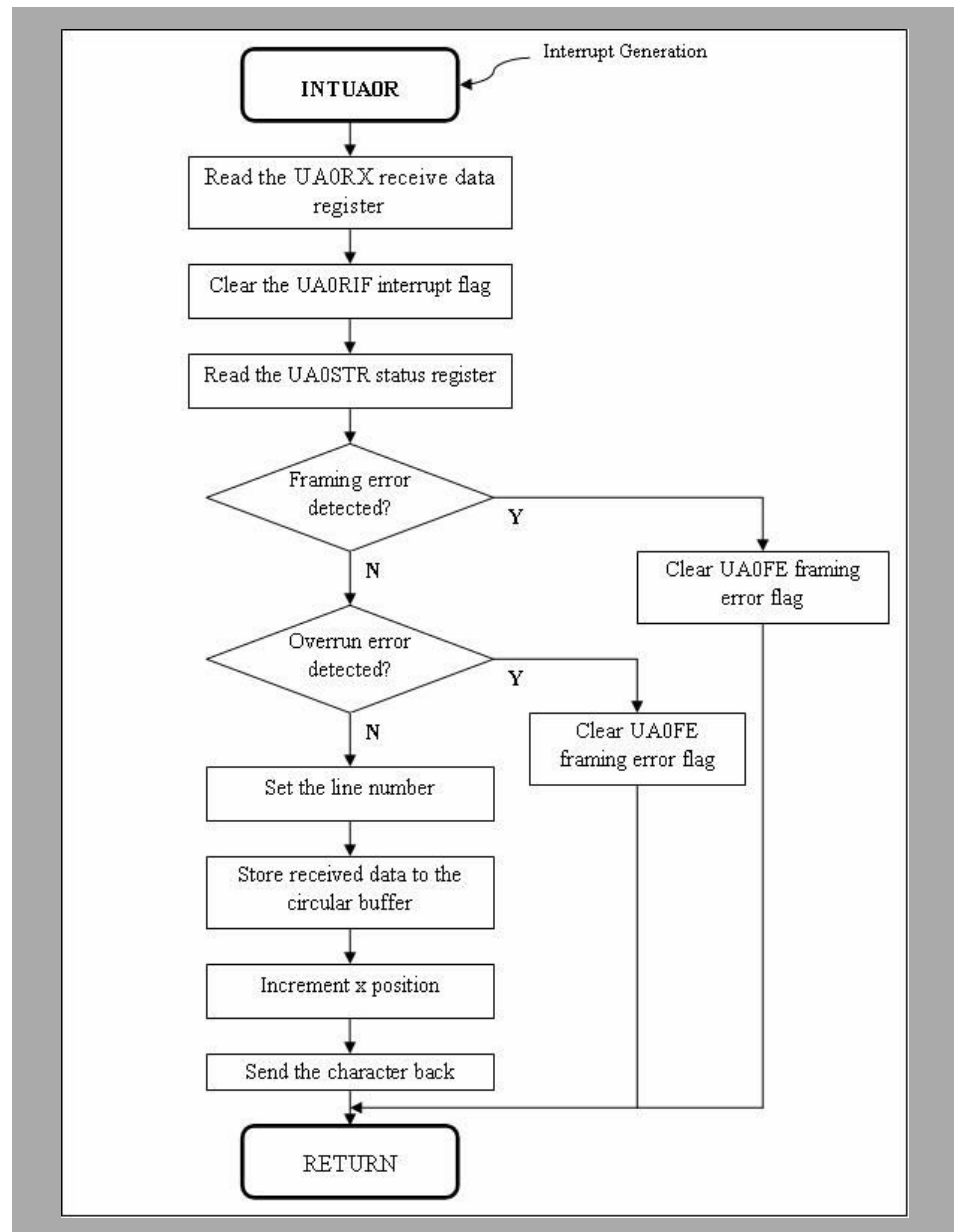### 3.4.5   Interrupt Service Routine for UARTA0 Reception

Figure 3-6   Flowchart of the interrupt service routine for UARTA0 reception

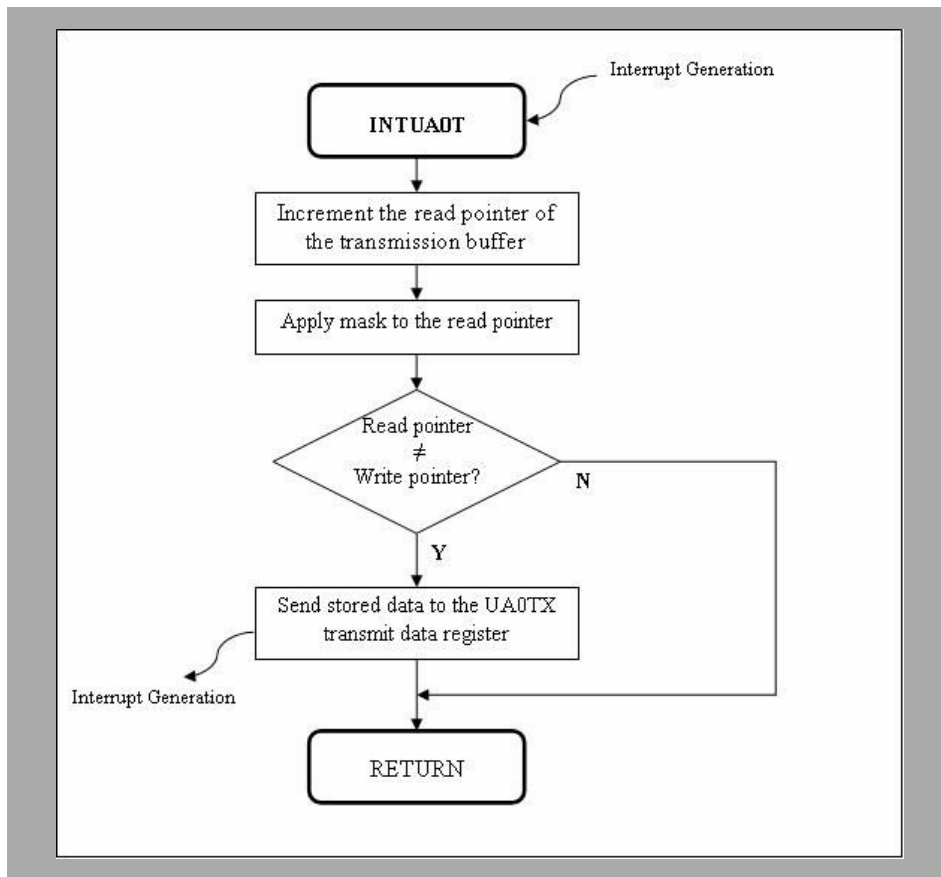### 3.4.6 Interrupt Service Routine for UARTA0 Transmission

Figure 3-7   Flowchart of the interrupt service routine for UARTA0 transmission