To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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Application Note

V850ES/Hx3
32-bit Single-Chip Microcontrollers
Flash Memory Programming (Programmer)

μPD70F3747
μPD70F3750
μPD70F3752
μPD70F3755
μPD70F3757
**NOTES FOR CMOS DEVICES**

1. **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

2. **HANDLING OF UNUSED INPUT PINS**
   Unconnected CMOS device inputs can be a cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

3. **PRECAUTION AGAINST ESD**
   A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

4. **STATUS BEFORE INITIALIZATION**
   Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

5. **POWER ON/OFF SEQUENCE**
   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

6. **INPUT OF SIGNAL DURING POWER OFF STATE**
   Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.
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INTRODUCTION

Target Readers This application note is intended for users who understand the functions of the V850ES/Hx3 and who will use this product to design application systems.

Purpose The purpose of this application note is to help users understand how to develop dedicated flash memory programmers for rewriting the internal flash memory of the V850ES/Hx3.

The sample programs and circuit diagrams shown in this document are for reference only and are not intended for use in actual design-ins. Therefore, these sample programs must be used at the user’s own risk. Correct operation is not guaranteed if these sample programs are used.

Organization This manual consists of the following main sections.
• Flash memory programming
• Programmer operating environment
• Basic programmer operation
• Command/data frame format
• Description of command processing
• UART communication mode
• 3-wire serial I/O communication mode with handshake supported (CSI + HS)
• 3-wire serial I/O communication mode (CSI)
• Flash memory programming parameter characteristics

How to Read This Manual It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

To learn more about the V850ES/Hx3’s hardware functions:
→ See the user’s manual of each V850ES/Hx3 product.

Conventions

Data significance: Higher digits on the left and lower digits on the right
Active low representation: xxx (overscore over pin or signal name)
Note: Footnote for item marked with Note in the text
Caution: Information requiring particular attention
Remark: Supplementary information
Numerical representation: Binary .................xxxx or xxxxB
Decimal .................xxxx
Hexadecimal .........xxxxH
Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Device-related documents

<table>
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CHAPTER 7 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS ............243
CHAPTER 1  FLASH MEMORY PROGRAMMING

To rewrite the contents of the internal flash memory of the V850ES/Hx3, a dedicated flash memory programmer (hereafter referred to as the “programmer”) is usually used.

This Application Note explains how to develop a dedicated programmer.

1.1 Overview

The V850ES/Hx3 incorporates firmware that controls flash memory programming. The programming to the internal flash memory is performed by transmitting/receiving commands between the programmer and the V850ES/Hx3 via serial communication.

Figure 1-1. System Outline of Flash Memory Programming in V850ES/Hx3
1.2 System Configuration

Examples of the system configuration for programming the flash memory are illustrated in Figure 1-2.
These figures illustrate how to program the flash memory with the programmer, under control of a host machine.
Depending on how the programmer is connected, the programmer can be used in a standalone mode without using
the host machine, if a user program has been downloaded to the programmer in advance.
For example, NEC Electronics’ flash memory programmer PG-FP5 can execute programming either by using the
GUI software with a host machine connected or by itself (standalone).

Figure 1-2. System Configuration Example

(1) UART communication mode (LSB-first transfer)

(2) 3-wire serial I/O communication mode with handshake supported (CSI + HS) (MSB-first transfer)

(3) 3-wire serial I/O communication mode (CSI) (MSB-first transfer)
Remark  For the pins used by flash memory programming and the recommended connections of unused pins, see the user’s manual of each product.

1.3  Flash Memory Configuration

The programmer must manage product-specific information (such as a device name and memory information). Table 1-1 shows the flash memory size of the V850ES/Hx3 and Figure 1-3 shows the configuration of the flash memory.

Table 1-1. Flash Memory Size of V850ES/Hx3

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>μPD70F3747</td>
<td>128 KB</td>
</tr>
<tr>
<td>μPD70F3750</td>
<td>256 KB</td>
</tr>
<tr>
<td>μPD70F3752</td>
<td>256 KB</td>
</tr>
<tr>
<td>μPD70F3755</td>
<td>256 KB</td>
</tr>
<tr>
<td>μPD70F3757</td>
<td>512 KB</td>
</tr>
</tbody>
</table>
Figure 1-3. Flash Memory Configuration
1.4 Command List and Status List

The flash memory incorporated in the V850ES/Hx3 has functions to manipulate the flash memory, as listed in Table 1-2. The programmer transmits commands to control these functions to the V850ES/Hx3, and checks the response status sent from the V850ES/Hx3, to manipulate the flash memory.

1.4.1 Command List

The commands used by the programmer and their functions are listed below.

Table 1-2. List of Commands Transmitted from Programmer to V850ES/Hx3

<table>
<thead>
<tr>
<th>Command Number</th>
<th>Command Name</th>
<th>Function Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>20H</td>
<td>Chip Erase</td>
<td>Erase</td>
<td>Erases the entire flash memory area.</td>
</tr>
<tr>
<td>22H</td>
<td>Block Erase</td>
<td></td>
<td>Erases a specified area in the flash memory.</td>
</tr>
<tr>
<td>40H</td>
<td>Programming</td>
<td>Write</td>
<td>Writes data to a specified area in the flash memory.</td>
</tr>
<tr>
<td>13H</td>
<td>Verify</td>
<td>Verify</td>
<td>Compares the contents in a specified area in the flash memory with data transmitted from the programmer.</td>
</tr>
<tr>
<td>32H</td>
<td>Block Blank Check</td>
<td>Blank check</td>
<td>Checks the erase status of a specified block in the flash memory.</td>
</tr>
<tr>
<td>50H</td>
<td>Read</td>
<td>Read</td>
<td>Reads data in the specified flash memory area.</td>
</tr>
<tr>
<td>70H</td>
<td>Status</td>
<td>Information acquisition</td>
<td>Acquires the current operating status (status data).</td>
</tr>
<tr>
<td>C0H</td>
<td>Silicon Signature</td>
<td></td>
<td>Acquires V850ES/Hx3 information (write protocol information).</td>
</tr>
<tr>
<td>C5H</td>
<td>Version Get</td>
<td></td>
<td>Acquires version information of the V850ES/Hx3 and firmware.</td>
</tr>
<tr>
<td>B0H</td>
<td>Checksum</td>
<td></td>
<td>Acquires checksum data of a specified area.</td>
</tr>
<tr>
<td>A0H</td>
<td>Security Set</td>
<td>Security</td>
<td>Sets security information.</td>
</tr>
<tr>
<td>00H</td>
<td>Reset</td>
<td>Others</td>
<td>Detects synchronization in communication.</td>
</tr>
<tr>
<td>90H</td>
<td>Oscillating Frequency Set</td>
<td></td>
<td>Specifies the oscillation frequency of the V850ES/Hx3.</td>
</tr>
<tr>
<td>9AH</td>
<td>Baud Rate Set</td>
<td></td>
<td>Sets baud rate when UART communication mode is selected.</td>
</tr>
</tbody>
</table>
1.4.2 Status list

The following table lists the status codes the programmer receives from the V850ES/Hx3.

<table>
<thead>
<tr>
<th>Status Code</th>
<th>Status Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>04H</td>
<td>Command number error. Error returned if a command not supported is received.</td>
</tr>
<tr>
<td>05H</td>
<td>Parameter error. Error returned if command information (parameter) is invalid.</td>
</tr>
<tr>
<td>06H</td>
<td>Normal acknowledgment (ACK). Normal acknowledgment.</td>
</tr>
<tr>
<td>07H</td>
<td>Checksum error. Error returned if data in a frame transmitted from the programmer is abnormal.</td>
</tr>
<tr>
<td>0F10H</td>
<td>Verify error. A verify error has occurred for the data of the frame transmitted from the programmer.</td>
</tr>
<tr>
<td>10H</td>
<td>Protect error. Error returned if an attempt is made to execute processing that is prohibited by the Security Set command.</td>
</tr>
<tr>
<td>15H</td>
<td>Negative acknowledgment (NACK). Negative acknowledgment.</td>
</tr>
<tr>
<td>1AH</td>
<td>MRG10 error. Erase error.</td>
</tr>
<tr>
<td>1BH</td>
<td>MRG11 error. Internal verify error or blank check error in writing data.</td>
</tr>
<tr>
<td>1CH</td>
<td>Write error. Write error.</td>
</tr>
<tr>
<td>FFH</td>
<td>Processing in progress (BUSY). Busy response.</td>
</tr>
</tbody>
</table>

**Note** During CSI communication, 1-byte “FFH” may be transmitted, as well as “FFH” as the data frame format.

Reception of a checksum error or NACK is treated as an immediate abnormal end in this manual. When a dedicated programmer is developed, however, the processing may be retried without problem from the wait immediately before transmission of the command that results a checksum error or NACK. In this event, limiting the retry count is recommended for preventing infinite repetition of the retry operation.

Although not listed in the above table, if a time-out error (BUSY time-out or time-out in data frame reception during UART communication) occurs, it is recommended to shutdown the power supply to the V850ES/Hx3 (refer to 1.6 Shutting Down Target Power Supply) and then connect the power supply again.
1.5 Power Application and Setting Flash Memory Programming Mode

To rewrite the contents of the flash memory with the programmer, the V850ES/Hx3 must first be set to the flash memory programming mode by supplying a specific voltage to the flash memory programming mode setting pin (FLMD0, FLMD1) in the V850ES/Hx3, then releasing a reset.

To select a communication mode for flash memory programming, input pulses to FLMD0 pin in the flash memory programming mode.

The following illustrates a timing chart for setting the flash memory programming mode and selecting the communication mode.

**Figure 1-4. Setting Flash Memory Programming Mode and Selecting Communication Mode**

The relationship between the settings of the FLMD0 and FLMD1 pins after reset release and the operating mode is shown below.

**Table 1-4. Relationship Between FLMD0 and FLMD1 Pins Setting After Reset Release and Operating Mode**

<table>
<thead>
<tr>
<th>FLMD0</th>
<th>FLMD1</th>
<th>Operating Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low (GND)</td>
<td>Any</td>
<td>Normal operating mode</td>
</tr>
<tr>
<td>High (Vcc)</td>
<td>Low (GND)</td>
<td>Flash memory programming mode</td>
</tr>
<tr>
<td>High (Vcc)</td>
<td>High (Vcc)</td>
<td>Setting prohibited</td>
</tr>
</tbody>
</table>

The following table shows the relationship between the number of FLMD0 pulses (pulse counts) and communication modes that can be selected with the V850ES/Hx3.
### Table 1-5. Relationship Between FLMD0 Pulse Counts and Communication Modes

<table>
<thead>
<tr>
<th>Communication Mode</th>
<th>FLMD0 Pulse Counts</th>
<th>Port Used for Communication</th>
</tr>
</thead>
<tbody>
<tr>
<td>UART (UARTD0)</td>
<td>0</td>
<td>TXDD0 (P30), RXDD0 (P31)</td>
</tr>
<tr>
<td>3-wire serial I/O (CSIB0)</td>
<td>8</td>
<td>SOB0 (P41), SIB0 (P40), SCKB0 (P42)</td>
</tr>
<tr>
<td>3-wire serial I/O with</td>
<td>11</td>
<td>SOB0 (P41), SIB0 (P40), SCKB0 (P42), HS</td>
</tr>
<tr>
<td>handshake supported (CSIB0 + HS)</td>
<td></td>
<td>(PCM0)</td>
</tr>
</tbody>
</table>

- **UART Communication Mode**
  The RxD and TxD pins are used for UART communication. The communication conditions are as shown below.

#### Table 1-6. UART Communication Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud rate</td>
<td>Selectable from 9,600, 19,200, 31,250, 38,400, 57,600, 76,800, 115,200, 128,000, and 153,600 bps (default: 9,600 bps)</td>
</tr>
<tr>
<td>Parity bit</td>
<td>None</td>
</tr>
<tr>
<td>Data length</td>
<td>8 bits (LSB first)</td>
</tr>
<tr>
<td>Stop bit</td>
<td>1 bit</td>
</tr>
</tbody>
</table>

The programmer always operates as the master device during CSI communication, so the programmer must check whether the processing by the V850ES/Hx3, such as writing or erasing, is normally completed. On the other hand, the status of the master and slave is occasionally exchanged during UART communication, so communication at the optimum timing is possible without assigning one pin like CSI + HS communication.

**Caution** Set the same baud rate to the master and slave devices when performing UART communication.

- **3-Wire Serial I/O Communication Mode with Handshake Supported (CSI + HS)**
  In the CSI + HS communication mode, the timing for communication of commands or data is optimized. In addition to the SI, SO and SCK pins, the HS (handshake) pin is used for implementing effective communication. The level of the HS pin signal falls (low level) when the V850ES/Hx3 is ready for transmitting or receiving data. The programmer must check the falling edge of the HS pin signal (low level) before starting transmission/reception of commands or data to the V850ES/Hx3. The communication data format is MSB-first, in 8-bit units.

**Figure 1-5. Timing Chart of CSI + HS Communication**

---

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3-Wire Serial I/O Communication Mode (CSI)

The SCK, SO and SI pins are used for CSI communication. The programmer always operates as the master device, so communication may not be performed normally if data is transmitted via the SCK pin while the V850ES/Hx3 is not ready for transmission/reception.

The communication data format is MSB-first, in 8-bit units.
1.5.1 Mode Setting Flowchart

- Processing to set programming mode
  - **RESET pin = low output**
  - **FLMD0 pin = low output**
  - **FLMD1 pin = low output**
  - **VDD pin = high output**
    (Target power supply on)
  - **Wait**
    **tDP (MIN.)**
  - **FLMD0 pin = high output**
  - **Wait**
  - **RESET pin = high output**
  - Start measurement of time until the Reset command processing starts

- UARTA0 communication (FLMD0 pulse = 0)?
  - Yes
  - **(tRP (MIN.) + trPE (MAX.))/2**
  - **Initialization of serial I/O hardware in accordance with communication mode**
  - Outputs the number of pulses corresponding to communication mode

- Time until Reset command processing starts elapsed?
  - Yes
  - End
  - No

- No
  - **Wait**
  - **Initialization of serial I/O hardware in accordance with communication mode**

- UART communication: **tR1** elapsed?
  - No
  - CSI communication: **tRC** elapsed?
  - Yes
  - CSI + HS communication: HS pin READY?
  - After this flow, execute Reset command processing of the respective communication mode.
1.5.2 Sample program

The following shows a sample program for mode setting processing.

```c
/**
 * connect to Flash device
 */

void fl_con_dev(void) {
    extern void init_fl_uart(void);
    extern void init_fl_csi(void);

    int n;
    int pulse;

    SRMK0 = true;
    UARTE0 = false;

    switch (fl_if) {
        default:
            case FLIF_UART: pulse = PULSE_UART; break;
            case FLIF_CSI: pulse = PULSE_CSI; break;
            case FLIF_CSI_HS: pulse = PULSE_CSIHS; break;
    }
    pFL_RES  = low;  // RESET/FLMD0 = low
    pmFL_FLMD0 = PM_OUT;  // FLMD0 = Low output
    pFL_FLMD0 = low;
    pmFL_FLMD1 = PM_OUT;  // FLMD1 = Low output
    pFL_FLMD1 = low;
    FL_VDD_HI();    // VDD = high
    fl_wait(tDP);    // wait
    pFL_FLMD0 = hi;   // FLMD0 = high
    fl_wait(tPR);    // wait
    pFL_RES  = hi;   // RESET = high
    start_flto(tRC);   // start "tRC" wait timer
    fl_wait((tRP+tRPE)/2);   // wait
    if (fl_if == FLIF_UART){
        init_fl_uart();  // Initialize UART h.w.(for Flash device control)
        UARTE0 = true;
        SRIF0 = false;
        SRMK0 = false;
    } else{
        init_fl_csi();  // Initialize CSI h.w.
    }
    for (n = 0; n < pulse; n++) { // pulse output
        pFL_FLMD0 = low;
    }
}
```
fl_wait(tPW);
pFL_FLMD0 = hi;
fl_wait(tPW);
}

while(!check_flto())  // timeout tRC ?
    ;  // no

    // start RESET command proc.
    }
1.6 Shutting Down Target Power Supply

After each command execution is completed, shut down the power supply to the target after setting the RESET pin to low level, as shown below.

Set other pins to Hi-Z when shutting down the power supply to the target.

Caution Shutting down the power supply and inputting a reset during command processing are prohibited.

![Figure 1-6. Timing for Terminating Flash Memory Programming Mode](image)

1.7 Command Execution Flow at Flash Memory Rewriting

Figure 1-6 illustrates the basic flowchart when flash memory rewriting is performed with the programmer. Other than commands shown in the Figure 1-6, the Verify command and Checksum command are also be supported.
Figure 1-7. Basic Flowchart for Flash Memory Rewrite Processing

Remark  The example of each command execution is shown in the Figure 1-8.
Figure 1-8. General Command Execution Flow at Flash Memory Rewriting

- General command flow
- Block Blank Check command (See 3.9)
- Block Erase command execution (See 3.6)
- Programming command execution (See 3.7)
- Verify command execution (See 3.8)
- Security Set command execution (See 3.13)
- End

This command is used to check whether data communication between programmer and target device was normally completed.
CHAPTER 2 COMMAND/DATA FRAME FORMAT

The programmer uses the command frame to transmit commands to the V850ES/Hx3. The V850ES/Hx3 uses the data frame to transmit write data or verify data from the programmer to the V850ES/Hx3. A header, footer, data length information, and checksum are appended to each frame to enhance the reliability of the transferred data. The following shows the format of a command frame and data frame.

Figure 2-1. Command Frame Format

SOH  (1 byte) LEN  (1 byte) COM  (1 byte) Command information (variable length) (Max. 255 bytes) SUM  (1 byte) ETX  (1 byte)

Figure 2-2. Data Frame Format

STX  (1 byte) LEN  (1 byte) Data (variable length) (Max. 256 bytes) SUM  (1 byte) ETX or ETB  (1 byte)

Table 2-1. Description of Symbols in Each Frame

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOH</td>
<td>01H</td>
<td>Command frame header</td>
</tr>
<tr>
<td>STX</td>
<td>02H</td>
<td>Data frame header</td>
</tr>
<tr>
<td>LEN</td>
<td></td>
<td>Data length information (00H indicates 256).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Command frame: COM + command information length</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Data frame: Data field length</td>
</tr>
<tr>
<td>COM</td>
<td></td>
<td>Command number</td>
</tr>
<tr>
<td>SUM</td>
<td></td>
<td>Checksum data for a frame</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Obtained by sequentially subtracting all of calculation target data from the</td>
</tr>
<tr>
<td></td>
<td></td>
<td>initial value (00H) in 1-byte units (borrow is ignored). The calculation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>targets are as follows.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Command frame: LEN + COM + all of command information</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Data frame: LEN + all of data</td>
</tr>
<tr>
<td>ETB</td>
<td>17H</td>
<td>Footer of data frame other than the last frame</td>
</tr>
<tr>
<td>ETX</td>
<td>03H</td>
<td>Command frame footer, or footer of last data frame</td>
</tr>
</tbody>
</table>

The following shows examples of calculating the checksum (SUM) for a frame.
CHAPTER 2 COMMAND/DATA FRAME FORMAT

[Command frame]
No command information is included in the following example of a Status command frame, so LEN and COM are targets of checksum calculation.

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>70H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Checksum calculation targets

For this command frame, checksum data is obtained as follows.

00H (initial value) − 01H (LEN) − 70H (COM) = 8FH (Borrow ignored. Lower 8 bits only.)

The command frame finally transmitted is as follows.

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>70H</td>
<td>8FH</td>
<td>03H</td>
</tr>
</tbody>
</table>

[Data frame]
To transmit a data frame as shown below, LEN to D4 are targets of checksum calculation.

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>04H</td>
<td>FFH</td>
<td>80H</td>
<td>40H</td>
<td>22H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Checksum calculation targets

For this data frame, checksum data is obtained as follows.

00H (initial value) − 04H (LEN) − FFH (D1) − 80H (D2) − 40H (D3) − 22H (D4) = 1BH (Borrow ignored. Lower 8 bits only.)

The data frame finally transmitted is as follows.

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>04H</td>
<td>FFH</td>
<td>80H</td>
<td>40H</td>
<td>22H</td>
<td>1BH</td>
<td>03H</td>
</tr>
</tbody>
</table>

When a data frame is received, the checksum data is calculated in the same manner, and the obtained value is used to detect a checksum error by judging whether the value is the same as that stored in the SUM field of the receive data. When a data frame as shown below is received, for example, a checksum error is detected.

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>04H</td>
<td>FFH</td>
<td>80H</td>
<td>40H</td>
<td>22H</td>
<td>1AH</td>
<td>03H</td>
</tr>
</tbody>
</table>

↑ Should be 1BH, if normal
2.1 Command Frame Transmission Processing

Read the following chapters for details on flowcharts of command processing to transmit command frames, for each communication mode.

- For the UART communication mode, read 4.1 Flowchart of Command Frame Transmission Processing.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 5.1 Flowchart of Command Frame Transmission Processing.
- For the 3-wire serial I/O communication mode (CSI), read 6.1 Flowchart of Command Frame Transmission Processing.

2.2 Data Frame Transmission Processing

The write data frame (user program), verify data frame (user program), and security data frame (security flag) are transmitted as a data frame.

Read the following chapters for details on flowcharts of command processing to transmit data frames, for each communication mode.

- For the UART communication mode, read 4.2 Flowchart of Data Frame Transmission Processing.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 5.2 Flowchart of Data Frame Transmission Processing.
- For the 3-wire serial I/O communication mode (CSI), read 6.2 Flowchart of Data Frame Transmission Processing.

2.3 Data Frame Reception Processing

The status frame, silicon signature data frame, version data frame, checksum data frame, and read data frame are received as a data frame.

Read the following chapters for details on flowcharts of command processing to receive data frames, for each communication mode.

- For the UART communication mode, read 4.3 Flowchart of Data Frame Reception Processing.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 5.3 Flowchart of Data Frame Reception Processing.
- For the 3-wire serial I/O communication mode (CSI), read 6.3 Flowchart of Data Frame Reception Processing.
CHAPTER 3 DESCRIPTION OF COMMAND PROCESSING

3.1 Status Command

3.1.1 Description

This command is used to check the operation status of the V850ES/Hx3 after issuance of each command such as write or erase.

After the Status command is issued, if the Status command frame cannot be received normally in the V850ES/Hx3 due to problems based on communication or the like, the status setting will not performed in the V850ES/Hx3. As a result, a busy response (FFH), not the status frame, may be received. In such a case, retry the Status command.

3.1.2 Command frame and status frame

Figure 3-1 shows the format of a command frame for the Status command, and Figure 3-2 shows the status frame for the command.

![Figure 3-1. Status Command Frame (from Programmer to V850ES/Hx3)](image)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>70H (Status)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

![Figure 3-2. Status Frame for Status Command (from V850ES/Hx3 to Programmer)](image)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>n</td>
<td>ST1</td>
<td>STn</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

Remarks 1. ST1 to STn: Status #1 to Status #n

2. The length of a status frame varies according to each command (such as write or erase) to be transmitted to the V850ES/Hx3.

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850ES/Hx3, flowcharts of command processing, and sample programs for each communication mode.

- The Status command is not used in the UART communication mode.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 5.4 Status Command.
- For the 3-wire serial I/O communication mode (CSI), read 6.4 Status Command.

Caution After each command such as write or erase is transmitted in UART communication, the V850ES/Hx3 automatically returns the status frame within a specified time. The Status command is therefore not used. If the Status command is transmitted in UART communication, the Command Number Error is returned.
3.2 Reset Command

3.2.1 Description
This command is used to check the establishment of communication between the programmer and the V850ES/Hx3 after the communication mode is set.

When UART is selected as the mode for communication with the V850ES/Hx3, the same baud rate must be set in the programmer and V850ES/Hx3. However, the V850ES/Hx3 cannot detect its own operating frequency so the baud rate cannot be set. It makes detection of the operating frequency in the V850ES/Hx3 possible by sending “00H” twice at 9,600 bps from the programmer, measuring the low-level width of “00H”, and then calculating the average of two sent signals. The baud rate can consequently be set, which enables synchronous detection in communication.

3.2.2 Command frame and status frame
Figure 3-3 shows the format of a command frame for the Reset command, and Figure 3-4 shows the status frame for the command.

Figure 3-3. Reset Command Frame (from Programmer to V850ES/Hx3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>00H (Reset)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Figure 3-4. Status Frame for Reset Command (from V850ES/Hx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>1</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark ST1: Synchronization detection result

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850ES/Hx3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 4.4 Reset Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 5.5 Reset Command.
- For the 3-wire serial I/O communication mode (CSI), read 6.5 Reset Command.
### 3.3 Baud Rate Set Command

#### 3.3.1 Description

This command is used to change the baud rate for UART (default value: 9,600 bps).

After the Baud Rate Set command is executed, the Reset command must be executed to confirm synchronization at the new baud rate.

The Baud Rate Set command is valid only in the UART communication mode. Data for setting the baud rate is represented as a 1-byte numeric value.

The V850ES/Hx3 ignores the Baud Rate Set command if it is transmitted in modes other than the UART communication mode.

#### 3.3.2 Command frame and status frame

Figure 3-5 shows the format of a command frame for the Baud Rate Set command, and Figure 3-6 shows the status frame for the command.

**Figure 3-5. Baud Rate Set Command Frame (from Programmer to V850ES/Hx3)**

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>02H</td>
<td>9AH</td>
<td>(Baud Rate Set)</td>
<td>D01</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

**Remark**  
D01: Baud rate selection value

<table>
<thead>
<tr>
<th>D01 Value</th>
<th>03H</th>
<th>04H</th>
<th>05H</th>
<th>06H</th>
<th>07H</th>
<th>08H</th>
<th>09H</th>
<th>0AH</th>
<th>0BH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud rate (bps)</td>
<td>9,600</td>
<td>19,200</td>
<td>31,250</td>
<td>38,400</td>
<td>76,800</td>
<td>153,600</td>
<td>57,600</td>
<td>115,200</td>
<td>128,000</td>
</tr>
</tbody>
</table>

**Figure 3-6. Status Frame for Baud Rate Set Command (from V850ES/Hx3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**  
ST1: Synchronization detection result

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850ES/Hx3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read **4.5 Baud Rate Set Command**.
- The Baud Rate Set command is not used in the 3-wire serial I/O communication mode with handshake supported (CSI + HS).
- The Baud Rate Set command is not used in 3-wire serial I/O communication mode (CSI).
3.4 Oscillating Frequency Set Command

3.4.1 Description
This command is used to set oscillation frequency data in the V850ES/Hx3.
Specify the frequency of the clock that is actually input to the X1 pin of the V850ES/Hx3.
The V850ES/Hx3 automatically sets the multiply rate of the CPU operation clock, based on the clock frequency
specified with this command. Therefore, note that the reference clock for wait calculation varies before and after
execution of this command.

3.4.2 Command frame and status frame
Figure 3-7 shows the format of a command frame for the Oscillating Frequency Set command, and Figure 3-8
shows the status frame for the command.

Figure 3-7. Oscillating Frequency Set Command Frame (from Programmer to V850ES/Hx3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>05H</td>
<td>90H</td>
<td>(Oscillating Frequency Set)</td>
<td>D01</td>
<td>D02</td>
</tr>
</tbody>
</table>

Remark  D01 to D04: Oscillation frequency = (D01 × 0.1 + D02 × 0.01 + D03 × 0.001) × 10³⁴ (Unit: kHz)
Settings can be made from 10 kHz to 100 MHz, but set the value according to the
specifications of each device when actually transmitting the command. D01 to D03 hold unpacked BCDs, and D04 holds a signed integer.

Setting example:  To set 6 MHz
D01 = 06H
D02 = 00H
D03 = 00H
D04 = 04H
Oscillation frequency = 6 × 0.1 × 10³⁴ = 6,000 kHz = 6 MHz

Setting example:  To set 10 MHz
D01 = 01H
D02 = 00H
D03 = 00H
D04 = 05H
Oscillation frequency = 1 × 0.1 × 10³⁴ = 10,000 kHz = 10 MHz

Figure 3-8. Status Frame for Oscillating Frequency Set Command (from V850ES/Hx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  ST1: Oscillation frequency setting result
Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850ES/Hx3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 4.6 Oscillating Frequency Set Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 5.6 Oscillating Frequency Set Command.
- For the 3-wire serial I/O communication mode (CSI), read 6.6 Oscillating Frequency Set Command.
3.5 Chip Erase Command

3.5.1 Description
This command is used to erase the entire contents of the flash memory. In addition, all of the information that is set by security setting processing can be initialized by Chip Erase processing, as long as execution of the Chip Erase command is not prohibited by the security setting (see 3.13 Security Set Command).

3.5.2 Command frame and status frame
Figure 3-9 shows the format of a command frame for the Chip Erase command, and Figure 3-10 shows the status frame for the command.

![Figure 3-9. Chip Erase Command Frame (from Programmer to V850ES/Hx3)](image)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>20H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

(Chip Erase)

![Figure 3-10. Status Frame for Chip Erase Command (from V850ES/Hx3 to Programmer)](image)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark** ST1: Chip erase result

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850ES/Hx3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 4.7 Chip Erase Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 5.7 Chip Erase Command.
- For the 3-wire serial I/O communication mode (CSI), read 6.7 Chip Erase Command.
3.6  Block Erase Command

3.6.1  Description

This command is used to erase the contents of blocks with the specified number in the flash memory, as long as erasure is not prohibited by the security setting (see 3.13 Security Set Command).

3.6.2  Command frame and status frame

Figure 3-11 shows the format of a command frame for the Block Erase command, and Figure 3-12 shows the status frame for the command.

Figure 3-11.  Block Erase Command Frame (from Programmer to V850ES/Hx3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>02H</td>
<td>22H</td>
<td>SAH</td>
<td>SAM</td>
<td>SAL</td>
</tr>
</tbody>
</table>

Remark  
SAH to SAL: Block erase start address (start address of arbitrary block)  
SAH: Start address, high (bits 23 to 16)  
SAM: Start address, middle (bits 15 to 8)  
SAL: Start address, low (bits 7 to 0)  
EAH to EAL: Block erase end addresses (start address of arbitrary block)  
EAH: End address, high (bits 23 to 16)  
EAM: End address, middle (bits 15 to 8)  
EAL: End address, low (bits 7 to 0)

Figure 3-12.  Status Frame for Block Erase Command (from V850ES/Hx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  
ST1: Block erase result

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850ES/Hx3, flowcharts of command processing, and sample programs for each communication mode.

• For the UART communication mode, read 4.8 Block Erase Command.
• For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 5.8 Block Erase Command.
• For the 3-wire serial I/O communication mode (CSI), read 6.8 Block Erase Command.
3.7 Programming Command

3.7.1 Description

This command is used to transmit data by the number of written bytes after the write start address and the write end address are transmitted. This command then writes the user program to the flash memory and verifies it internally.

The write start/end address can be set only in the block start/end address units.

If both of the status frames (ST1 and ST2) after the last data transmission indicate ACK, the V850ES/Hx3 firmware automatically executes internal verify. Therefore, the Status command for this internal verify must be transmitted.

3.7.2 Command frame and status frame

Figure 3-13 shows the format of a command frame for the Programming command, and Figure 3-14 shows the status frame for the command.

![Figure 3-13. Programming Command Frame (from Programmer to V850ES/Hx3)](image)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>40H</td>
<td>SAH</td>
<td>SAM</td>
<td>SAL</td>
</tr>
</tbody>
</table>

**Remark** SAH, SAM, SAL: Write start addresses
EAH, EAM, EAL: Write end addresses

![Figure 3-14. Status Frame for Programming Command (from V850ES/Hx3 to Programmer)](image)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (a)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark** ST1 (a): Command reception result

3.7.3 Data frame and status frame

Figure 3-15 shows the format of a frame that includes data to be written, and Figure 3-16 shows the status frame for the data.

![Figure 3-15. Data Frame to Be Written (from Programmer to V850ES/Hx3)](image)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX/ETB</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>00H to FFH (00H = 256)</td>
<td>Write Data</td>
<td>Checksum</td>
<td>03H/17H</td>
</tr>
</tbody>
</table>

**Remark** Write Data: User program to be written

![Figure 3-16. Status Frame for Data Frame (from V850ES/Hx3 to Programmer)](image)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>02H</td>
<td>ST1 (b)</td>
<td>ST2 (b)</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

**Remark** ST1 (b): Data reception check result
ST2 (b): Write result
3.7.4 Completion of transferring all data and status frame

Figure 3-17 shows the status frame after transfer of all data is completed.

**Figure 3-17. Status Frame After Completion of Transferring All Data (from V850ES/Hx3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (c)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**  ST1 (c): Internal verify result

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850ES/Hx3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read **4.9 Programming Command**.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read **5.9 Programming Command**.
- For the 3-wire serial I/O communication mode (CSI), read **6.9 Programming Command**.
3.8 Verify Command

3.8.1 Description
This command is used to compare the data transmitted from the programmer with the data read from the V850ES/Hx3 (read level) in the specified address range, and check whether they match.
The verify start/end address can be set only in the block start/end address units.

3.8.2 Command frame and status frame
Figure 3-18 shows the format of a command frame for the Verify command, and Figure 3-19 shows the status frame for the command.

Figure 3-18. Verify Command Frame (from Programmer to V850ES/Hx3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>13H (Verify)</td>
<td>SAH</td>
<td>SAM</td>
<td>SAL</td>
</tr>
</tbody>
</table>

Remark
SAH, SAM, SAL: Verify start addresses
EAH, EAM, EAL: Verify end addresses

Figure 3-19. Status Frame for Verify Command (from V850ES/Hx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (a)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark
ST1 (a): Command reception result

3.8.3 Data frame and status frame
Figure 3-20 shows the format of a frame that includes data to be verified, and Figure 3-21 shows the status frame for the data.

Figure 3-20. Data Frame of Data to Be Verified (from Programmer to V850ES/Hx3)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX/ETB</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>00H to FFH (00H = 256)</td>
<td>ST1 (Verify)</td>
<td>Checksum</td>
<td>03H/17H</td>
</tr>
</tbody>
</table>

Remark
Verify Data: User program to be verified
Figure 3-21. Status Frame for Data Frame (from V850ES/Hx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>02H</td>
<td>ST1 (b)</td>
<td>ST2 (b)</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

**Remark**  ST1 (b): Data reception check result  
ST2 (b): Verify result

**Note**  Even if a verify error occurs in the specified address range, ACK is always returned as the verify result. The status of all verify errors are reflected in the verify result for the last data. Therefore, the occurrence of verify errors can be checked only when all the verify processing for the specified address range is completed.

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850ES/Hx3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 4.10 Verify Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 5.10 Verify Command.
- For the 3-wire serial I/O communication mode (CSI), read 6.10 Verify Command.
3.9 Block Blank Check Command

3.9.1 Description
This command is used to check if data in the flash memory of the specified block is blank (erased state).

3.9.2 Command frame and status frame
Figure 3-22 shows the format of a command frame for the Block Blank Check command, and Figure 3-23 shows the status frame for the command.

**Figure 3-22. Block Blank Check Command Frame (from Programmer to V850ES/Hx3)**

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>32H (Block Blank Check)</td>
<td>SAH</td>
<td>SAM</td>
<td>SAL</td>
</tr>
</tbody>
</table>

**Remark**
SAH to SAL: Block blank check start address (start address of arbitrary block)
SAH: Start address, high (bits 23 to 16)
SAM: Start address, middle (bits 15 to 8)
SAL: Start address, low (bits 7 to 0)
EAH to EAL: Block blank check end address (end address of arbitrary block)
EAH: End address, high (bits 23 to 16)
EAM: End address, middle (bits 15 to 8)
EAL: End address, low (bits 7 to 0)

**Figure 3-23. Status Frame for Block Blank Check Command (from V850ES/Hx3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**
ST1: Block blank check result

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850ES/Hx3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 4.11 Block Blank Check Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 5.11 Block Blank Check Command.
- For the 3-wire serial I/O communication mode (CSI), read 6.11 Block Blank Check Command.
3.10 Silicon Signature Command

3.10.1 Description

This command is used to read the write protocol information (silicon signature) of the device.

If the programmer supports a programming protocol that is not supported in the V850ES/Hx3, for example, execute this command to select an appropriate protocol in accordance with the values of the second and third bytes.

3.10.2 Command frame and status frame

Figure 3-24 shows the format of a command frame for the Silicon Signature command, and Figure 3-25 shows the status frame for the command.

Figure 3-24. Silicon Signature Command Frame (from Programmer to V850ES/Hx3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>C0H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

(Silicon Signature)

Figure 3-25. Status Frame for Silicon Signature Command (from V850ES/Hx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  ST1: Command reception result

3.10.3 Silicon signature data frame

Figure 3-26 shows the format of a frame that includes silicon signature data.

Figure 3-26. Silicon Signature Data Frame (from V850ES/Hx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>VEN</th>
<th>MET</th>
<th>MSC</th>
<th>DEC1</th>
<th>DEC2</th>
<th>END</th>
<th>INVALID DATA</th>
<th>SCF</th>
<th>BOT</th>
<th>RVAL</th>
<th>RVAM</th>
<th>RVAH</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>20H</td>
<td>VEN</td>
<td>MET</td>
<td>MSC</td>
<td>DEC1</td>
<td>DEC2</td>
<td>END</td>
<td>INVALID DATA</td>
<td>SCF</td>
<td>BOT</td>
<td>RVAL</td>
<td>RVAM</td>
<td>RVAH</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remarks 1. VEN: Vendor code (NEC: 10H)
MET: Macro extension code
MSC: Macro function code
DEC1: Device extension code 1
DEC2: Device extension code 2
END: Internal flash ROM last address
INVALID DATA: Invalid data of 18-byte length
SCF: Security flag information
BOT: Boot block number
RVAL: Reset vector address L (bits 7 to 0)
RVAM: Reset vector address M (bits 15 to 8)
RVAH: Reset vector address H (bits 23 to 16)

2. Of the fields other than BOT (boot block number) and RVAL, RVAM and RVAH (reset vector addresses), the lower 7 bits are used as a data entity, and the highest 1 bit is used as the odd parity.
### Table 3-1. Example of Silicon Signature Data

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Description</th>
<th>Length (Bytes)</th>
<th>Signature Data&lt;sup&gt;max&lt;/sup&gt;</th>
<th>Actual Value</th>
<th>Parity</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEN</td>
<td>Vendor code (NEC)</td>
<td>1</td>
<td>10H (00010000B)</td>
<td>10H</td>
<td>Added</td>
</tr>
<tr>
<td>MET</td>
<td>Macro extension code (fixed value)</td>
<td>1</td>
<td>7FH (01111111B)</td>
<td>7FH</td>
<td>Added</td>
</tr>
<tr>
<td>MSC</td>
<td>Macro function (fixed value)</td>
<td>1</td>
<td>04H (00000100B)</td>
<td>04H</td>
<td>Added</td>
</tr>
<tr>
<td>DEC1</td>
<td>Device extension code 1 (fixed value)</td>
<td>1</td>
<td>ECH (1110100B)</td>
<td>ECH</td>
<td>Added</td>
</tr>
<tr>
<td>DEC2</td>
<td>Device extension code 2 (fixed value)</td>
<td>1</td>
<td>7FH (1111111B)</td>
<td>7FH</td>
<td>Added</td>
</tr>
<tr>
<td>END</td>
<td>END Internal flash memory last address (extracted from the lower bytes)</td>
<td>4</td>
<td>7FH(1111111B) 07H(00000111B) 80H(10000000B)</td>
<td>0001FFFFH Added&lt;sup&gt;max&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>INVALID DATA</td>
<td>Invalid data</td>
<td>18</td>
<td>−</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>SCF</td>
<td>Security flag information</td>
<td>1</td>
<td>Any</td>
<td>Any</td>
<td>Added</td>
</tr>
<tr>
<td>BOT</td>
<td>Boot block cluster last block number</td>
<td>1</td>
<td>Any</td>
<td>Any</td>
<td>None</td>
</tr>
<tr>
<td>RVAL</td>
<td>Reset vector address L (bits 7 to 0)</td>
<td>1</td>
<td>Any</td>
<td>Any</td>
<td>None</td>
</tr>
<tr>
<td>RVAM</td>
<td>Reset vector address M (bits 15 to 8)</td>
<td>1</td>
<td>Any</td>
<td>Any</td>
<td>None</td>
</tr>
<tr>
<td>RVAH</td>
<td>Reset vector address H (bits 23 to 16)</td>
<td>1</td>
<td>Any</td>
<td>Any</td>
<td>None</td>
</tr>
</tbody>
</table>

**Notes**

1. 0 and 1 are odd parities (the values to adjust the number of “1” to be the odd number in a byte)

2. The parity calculation for the END field is performed as follows (when the last address is 0001FFFFH)

<1> The END field is divided in 7-bit units from the lower digit (the higher 4 bits are discarded).

```
0 0 0 0 1 F F F F
00000000 00000001 11111111 11111111
↓
0000 000000 0001111 11111111 11111111
```

<2> The odd parity bit is appended to the highest bit.

```
\[\begin{array}{c}
00000000 \\
00000011 \\
01111111 \\
01111111 (p = odd parity bit) \\
\end{array}\]
```

```
= \[\begin{array}{c}
00000000 \\
00000011 \\
01111111 \\
01111111 \\
\end{array}\]
```

```
= 80 07 7F 7F
```

<3> The order of the higher, middle, and lower bytes is reversed, as follows.

```
7F 7F 07 80
```
The following shows the procedure to translate the values in the END field that has been sent from the microcontroller to the actual address.

<1> The order of the higher, middle, and lower bytes is reversed, as follows.

```
7F 7F 07 80
↓
80 07 7F 7F
```

<2> Checks that the number of “1” is odd in each byte (this can be performed at another timing).

<3> The parity bit is removed and a 3-bit 0 is added to the highest bit.

```
80 07 7F 7F
↓
10000000 00000111 01111111 01111111
↓
0000000 0000111 1111111 11111111
↓
0000 0000000 0000111 1111111 1111111
```

<4> The values are translated into groups in 8-bit units.

```
00000000000000000000000000001111111111111111111111111111111111111111111
↓
00000000 00000000 11111111 11111111
↓
00 00 1 F F F F
```

If “7F 7F 07 80” is given to the END field, the actual last address is consequently \[0001FFFF\]H.

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850ES/Hx3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 4.12 Silicon Signature Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 5.12 Silicon Signature Command.
- For the 3-wire serial I/O communication mode (CSI), read 6.12 Silicon Signature Command.
3.11 Version Get Command

3.11.1 Description
This command is used to acquire information on the V850ES/Hx3 device version and firmware version.
Use this command when the programming parameters must be changed in accordance with the V850ES/Hx3 firmware version.

Caution The firmware version may be updated during firmware update that does not affect the change of flash programming parameters (at this time, update of the firmware version is not reported).

Example Firmware version and reprogramming parameters

<table>
<thead>
<tr>
<th>Firmware version</th>
<th>Programming parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1.00</td>
<td>Parameter A</td>
</tr>
<tr>
<td>V2.00</td>
<td>Parameter B</td>
</tr>
<tr>
<td>V3.00</td>
<td></td>
</tr>
</tbody>
</table>

3.11.2 Command frame and status frame
Figure 3-28 shows the format of a command frame for the Version Get command, and Figure 3-29 shows the status frame for the command.

Figure 3-28. Version Get Command Frame (from Programmer to V850ES/Hx3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>C5H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Figure 3-29. Status Frame for Version Get Command (from V850ES/Hx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark ST1: Command reception result
3.11.3 Version data frame

Figure 3-30 shows the data frame of version data.

Figure 3-30. Version Data Frame (from V850ES/Hx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>06H</td>
<td>DV1</td>
<td>DV2</td>
<td>DV3</td>
</tr>
</tbody>
</table>

Remark
DV1: Integer of device version
DV2: First decimal place of device version
DV3: Second decimal place of device version
FV1: Integer of firmware version
FV2: First decimal place of firmware version
FV3: Second decimal place of firmware version

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850ES/Hx3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 4.13 Version Get Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 5.13 Version Get Command.
- For the 3-wire serial I/O communication mode (CSI), read 6.13 Version Get Command.
3.12 Checksum Command

3.12.1 Description
This command is used to acquire the checksum data in the specified area.
For the checksum calculation start/end address, specify a fixed address in block units starting from the top of the flash memory.
Checksum data is obtained by sequentially subtracting data in the specified address range from the initial value (00H) in 1-byte units.

3.12.2 Command frame and status frame
Figure 3-31 shows the format of a command frame for the Checksum command, and Figure 3-32 shows the status frame for the command.

Figure 3-31. Checksum Command Frame (from Programmer to V850ES/Hx3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>B0H (Checksum)</td>
<td>SAH</td>
<td>SAM</td>
<td>SAL</td>
</tr>
</tbody>
</table>

Remark  SAH, SAM, SAL: Checksum calculation start addresses
EAH, EAM, EAL: Checksum calculation end addresses

Figure 3-32. Status Frame for Checksum Command (from V850ES/Hx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  ST1: Command reception result

3.12.3 Checksum data frame
Figure 3-33 shows the format of a frame that includes checksum data.

Figure 3-33. Checksum Data Frame (from V850ES/Hx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>02H</td>
<td>CK1</td>
<td>CK2</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

Remark  CK1: Higher 8 bits of checksum data
CK2: Lower 8 bits of checksum data

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850ES/Hx3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 4.14 Checksum Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 5.14 Checksum Command.
- For the 3-wire serial I/O communication mode (CSI), read 6.14 Checksum Command.
3.13 Security Set Command

3.13.1 Description
This command is used to perform security settings (enable or disable of write, block erase, and chip erase). By performing these settings with this command, rewriting of the flash memory by an unauthorized party can be restricted.

Caution Once the security setting is performed, changing of the setting from disable to enable will no longer be possible. To re-set the security flag, all the security flags must be initialized by executing the Chip Erase command (the Block Erase command cannot be used to initialize the security flags). If chip erase has been disabled, however, chip erase itself will be impossible and so the settings cannot be erased from the programmer. Re-confirmation of security setting execution is therefore recommended before disabling chip erase, due to this programmer specification.

3.13.2 Command frame and status frame
Figure 3-34 shows the format of a command frame for the Security Set command, and Figure 3-35 shows the status frame for the command.

The Security Set command frame includes the block number field and page number field but these fields do not have any particular usage, so set these fields to 00H.

Figure 3-34. Security Set Command Frame (from Programmer to V850ES/Hx3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>03H</td>
<td>A0H (Security Set)</td>
<td>00H (fixed)</td>
<td>00H (fixed)</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

Figure 3-35. Status Frame for Security Set Command (from V850ES/Hx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (a)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark ST1 (a): Command reception result
3.13.3 Data frame and status frame

Figure 3-36 shows the format of a security data frame, and Figure 3-37 shows the status frame for the data.

**Figure 3-36 Security Data Frame (from Programmer to V850ES/Hx3)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>05H</td>
<td>FLG</td>
<td>BOT</td>
<td>ADH</td>
</tr>
</tbody>
</table>

**Remark**
- **FLG**: Security flag
- **BOT**: Boot block cluster last block number (00H to 7FH)*note
- **ADH**: Reset vector handler address (bits 23 to 16)
- **ADM**: Reset vector handler address (bits 15 to 8)
- **ADL**: Reset vector handler address (bits 7 to 0)

**Note** Set it within the ROM size of V850ES/Hx3.

**Figure 3-37. Status Frame for Security Data Writing (from V850ES/Hx3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (b)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark** ST1 (b): Security data write result

3.13.4 Internal verify check and status frame

Figure 3-38 shows the status frame for internal verify check.

**Figure 3-38. Status Frame for Internal Verify Check (from V850ES/Hx3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (c)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark** ST1 (c): Internal verify result

The following table shows the contents in the security flag field.

**Table 3-2. Contents of Security Flag Field**

<table>
<thead>
<tr>
<th>Item</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>Fixed to 1</td>
</tr>
<tr>
<td>Bit 6</td>
<td></td>
</tr>
<tr>
<td>Bit 5</td>
<td></td>
</tr>
<tr>
<td>Bit 4</td>
<td>Boot block cluster rewrite disable flag (1: enable, 0: disable)</td>
</tr>
<tr>
<td>Bit 3</td>
<td>Read disable flag (1: enable, 0: disable)</td>
</tr>
<tr>
<td>Bit 2</td>
<td>Write disable flag (1: enable, 0: disable)</td>
</tr>
<tr>
<td>Bit 1</td>
<td>Block erase disable flag (1: enable, 0: disable)</td>
</tr>
<tr>
<td>Bit 0</td>
<td>Chip erase disable flag (1: enable, 0: disable)</td>
</tr>
</tbody>
</table>
The following table shows the relationship between the security flag field settings and the enable/disable status of each operation.

### Table 3-3. Security Flag Field and Enable/Disable Status of Each Operation

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>Command</th>
<th>Flash Memory Programming Mode</th>
<th>Self-Programming Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Command Operation After Security Setting</td>
<td>All commands can be executed regardless of the security setting values</td>
</tr>
<tr>
<td>Security Setting Item</td>
<td></td>
<td>√: Execution possible, ×: Execution impossible</td>
<td>Only retention of security setting values is possible</td>
</tr>
<tr>
<td></td>
<td></td>
<td>△: Writing other than for boot specification or block erase is possible</td>
<td></td>
</tr>
<tr>
<td>Disable writing</td>
<td>×</td>
<td>√</td>
<td>×</td>
</tr>
<tr>
<td>Disable chip erase</td>
<td>√</td>
<td>×</td>
<td>×</td>
</tr>
<tr>
<td>Disable block erase</td>
<td>√</td>
<td>√</td>
<td>×</td>
</tr>
<tr>
<td>Disable read</td>
<td>√</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>Disable boot block rewriting</td>
<td>△</td>
<td>×</td>
<td>△</td>
</tr>
</tbody>
</table>

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850ES/Hx3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read **4.15 Security Set Command**.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read **5.15 Security Set Command**.
- For the 3-wire serial I/O communication mode (CSI), read **6.15 Security Set Command**.
3.14 Read Command

3.14.1 Description
This command is used to read data from the flash memory of the V850ES/Hx3. The write start/end address can be set only in the block start/end address units.

3.14.2 Command frame and status frame
Figure 3-39 shows the format of a command frame for the Read command, and Figure 3-40 shows the status frame for the command.

Figure 3-39. Read Command Frame (from Programmer to V850ES/Hx3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>50H (Read)</td>
<td>SAH</td>
<td>SAM</td>
<td>SAL</td>
</tr>
</tbody>
</table>

Remark: SAH, SAM, SAL: Read start address (start address of the block)
EAH, EAM, EAL: Read end address (end address of the block)

Figure 3-40. Status Frame for Read Command (from V850ES/Hx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (a)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark: ST1 (a): Command reception result

3.14.3 Data frame and status frame
Figure 3-41 shows the format of a frame that includes data to be read, and Figure 3-42 shows the status frame for the data.

Figure 3-41. Data Frame of Data to Be Read (from V850ES/Hx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX/ETB</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>00H to FFH (00H = 256)</td>
<td>Read Data</td>
<td>Checksum</td>
<td>03H/17H</td>
</tr>
</tbody>
</table>

Remark: Read Data: Data read from V850ES/Hx3

Figure 3-42. Status Frame for Read Data (from Programmer to V850ES/Hx3)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (b)</td>
<td>Checksum</td>
<td>03H/17H</td>
</tr>
</tbody>
</table>

Remark: ST1 (b): ACK (06H) or NACK (15H) sent from the programmer for read data
Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850ES/Hx3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 4.16 Read Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 5.16 Read Command.
- For the 3-wire serial I/O communication mode (CSI), read 6.16 Read Command.
4.1 Command Frame Transmission Processing Flowchart

- Command frame transmission processing
- Command frame header (SOH = 01H) transmission
- Wait between data transmissions
- Data length (LEN) transmission
- Wait between data transmissions
- Command number (COM) transmission
- If (LEN - 1) bytes transmitted? Yes
  - No
  - Wait between data transmissions
  - Transmits 1-byte command information
  - Wait between data transmissions
  - Checksum data (SUM) transmission
  - Wait between data transmissions
  - Command frame footer (ETX = 03H) transmission
  - Wait between data transmissions
  - End of command frame transmission
4.2 Data Frame Transmission Processing Flowchart

Data frame transmission processing

Data frame header (STX = 02H) transmission

Wait between data transmissions

Data length (LEN) transmission

LEN bytes transmitted? Yes

No

Wait between data transmissions

Transmits 1-byte data

Wait between data transmissions

Checksum data (SUM) transmission

Wait between data transmissions

Last data frame? No

Yes

Transmission of last data frame footer (ETX = 03H)

Transmission of footer other than those of last data frame (ETB = 17H)

End of data frame transmission
4.3 Data Frame Reception Processing Flowchart
4.4 Reset Command

4.4.1 Processing sequence chart

Reset command processing sequence

Note  Do not exceed the retry count for the reset command transmission (up to 16 times).
4.4.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command processing starts (wait time $t_{com}$).
<2> The low level is output (data 00H is transmitted at 9,600 bps).
<3> Wait state (wait time $t_{12}$).
<4> The low level is output (data 00H is transmitted at 9,600 bps).
<5> Wait state (wait time $t_{2c}$).
<6> The Reset command is transmitted by command frame transmission processing.
<7> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT0}$).
<8> The status code is checked.

When ST1 = ACK: Normal completion [A]
When ST1 $\neq$ ACK: The retry count ($t_{RS}$) is checked.
   The sequence is re-executed from <5> if the retry count is not over.
   If the retry count is over, the processing ends abnormally [B].

4.4.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|                                | Negative acknowledgment (NACK) | 15H         | • A command other than the Status command was received during processing.  
                        |                                               |             | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]             | –           | The status frame was not received within the specified time. |
4.4.4 Flowchart

Reset command processing

Wait from previous frame reception until next command transmission

Transmits '00' at 9,600 bps

Wait

Transmits '00' at 9,600 bps

Wait

Command frame transmission processing (Reset)

Status frame received?

Yes

Timed out?

Yes

Time-out error [C]

No

Status = ACK?

Yes

Retry count over?

Yes

Abnormal termination [B]

No

Normal completion [A]

No

Retry count over?

No
4.4.5 Sample program

The following shows a sample program for Reset command processing.

```c
u16 fl_ua_reset(void)
{
    u16 rc;
    u32 retry;

    set_uart0_br(BR_9600); // change to 9600bps

    fl_wait(tCOM); // wait
    putc_ua(0x00); // send 0x00 @ 9600bps

    fl_wait(t12); // wait
    putc_ua(0x00); // send 0x00 @ 9600bps

    for (retry = 0; retry < tRS; retry++)
    {
        fl_wait(t2C); // wait

        put_cmd_ua(FL_COM_RESET, 1, fl_cmd_prm); // send RESET command

        rc = get_sfrm_ua(fl_ua_sfrm, tWT0_MAX);
        if (rc == FLC_DFTO_ERR) // t.o. ?
            break; // yes // case [C]

        if (rc == FLC_ACK){ // ACK ?
            break; // yes // case [A]
        }
        else{
            NOP();
        }
        //continue; // case [B] (if exit from loop)
    }

    // switch(rc) {
    //   //
    //   case FLC_NO_ERR: return rc; break; // case [A]
    //   case FLC_DFTO_ERR: return rc; break; // case [C]
    //   default: return rc; break; // case [B]
    // }
    return rc;
}
```
4.5 Baud Rate Set Command

4.5.1 Processing sequence chart

Baud Rate Set command processing sequence

Note  Do not exceed the retry count for the reset command transmission (up to 16 times).
4.5.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{\text{COM}}$).
<2> The Baud Rate Set command is transmitted by command frame transmission processing.
<3> Waits from command transmission until Reset command transmission (wait time $t_{\text{WT10}}$).
<4> The Reset command is transmitted by command frame transmission processing.
<5> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{\text{WT0}}$).
<6> Since the status code should be ACK, the processing ends normally [A].

4.5.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H The command was executed normally and the synchronization of the UART communication speed has been established between the programmer and the V850ES/Hx3.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Data frame reception was timed out. With the V850ES/Hx3, this command also results in errors in the following cases.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Command information (parameter) is invalid</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The command frame includes the checksum error</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The data length of the command frame (LEN) is invalid</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The footer of the command frame (ETX) is missing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The Reset command was not detected after setting the baud rate and receiving command frame data for 16 times.</td>
</tr>
</tbody>
</table>
4.5.4 Flowchart

![Flowchart Image]

- Baud Rate Set command processing
- Wait from previous frame reception until next command transmission
- Command frame transmission processing (Baud Rate Set)
- Wait from command frame transmission until Reset command transmission
- Command frame transmission processing (Reset)
- Status frame received?
  - No
  - Timed out?
    - No
    - Yes
    - twT1o (MAX.)
  - Yes
    - twT0 (MAX.)
  - Normal completion [A]
- Yes
  - Time-out error [C]
4.5.5 Sample program
The following shows a sample program for Baud Rate Set command processing.

```
/**************************
/* Set baudrate command */
**************************
/* [i]  u8 brid ... baudrate ID */
/* [r]  u16  ... error code */
/**************************
ul6  fl_ua_setbaud(u8 brid)
{
    ul6  rc;
    u8  br;
    ul32 retry;

    switch(brid){
        default:
            case BR_9600:  br = 0x03;  break;
            case BR_19200: br = 0x04;  break;
            case BR_38400: br = 0x05;  break;
            case BR_76800: br = 0x06;  break;
            case BR_153600: br = 0x08; break;
            case BR_57600:  br = 0x09;  break;
            case BR_115200: br = 0x0a; break;
            case BR_128000: br = 0x0b; break;
    }
    fl_cmdprm[0] = br;  // "D01"

    fl_wait(tCOM);       // wait before sending command
    put_cmd_ua(FL_COM_SET_BAUDRATE, 2, fl_cmdprm);  // send "Baudrate Set" command

    set_flbaud(brid);    // change baud-rate
    set_uart0_br(brid);  // change baud-rate (h.w.)

    retry = tRS;
    while(1){
        fl_wait(tWT10);

        put_cmd_ua(FL_COM_RESET, 1, fl_cmdprm);   // send RESET command

        rc = get_sfrm_ua(fl_ua_sfrm, tWT0_MAX);  // get status frame
        if (rc){
            if (retry--)
                continue;
```
else
    return rc;
}
break;  // got ACK !!

// switch(rc) {
//        case FLC_NO_ERR: return rc; break; // case [A]
//        case FLC_DFTO_ERR: return rc; break; // case [C]
//        default: return rc; break; // case [B]
//    }

return rc;
}
4.6 Oscillating Frequency Set Command

4.6.1 Processing sequence chart

Oscillating Frequency Set command processing sequence

1. Wait from previous frame reception until next command transmission
2. Oscillating Frequency Set command frame transmission
3. Time-out check for status frame reception
4. Status frame reception

- Normal completion [A]
- Abnormal termination [B]
- Time-out error [C]
- Other than ACK
- ACK
- Reception status [ACK/other than ACK]
4.6.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{com}$).

<2> The Oscillating Frequency Set command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.

   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{wa}$).

<4> The status code is checked.

   When ST1 = ACK: Normal completion [A]
   When ST1 ≠ ACK: Abnormal termination [B]

4.6.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
| Negative acknowledgment (NACK)  | 15H | • A command other than the Status command was received during processing.  
   • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]              | – | The status frame was not received within the specified time. |
4.6.4 Flowchart

Oscillating Frequency Set command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Oscillating Frequency Set)

Status frame received?

Yes

Timed out?

No

Yes

Time-out error [C]

No

Status = ACK?

Yes

Normal completion [A]

No

Abnormal termination [B]
4.6.5 Sample program

The following shows a sample program for Oscillating Frequency Set command processing.

```c
u16  fl_ua_setclk(u8 clk[])  
{  
   u16 rc;
   
   fl_cmd_prm[0] = clk[0]; // "D01"
   fl_cmd_prm[1] = clk[1]; // "D02"
   fl_cmd_prm[2] = clk[2]; // "D03"
   fl_cmd_prm[3] = clk[3]; // "D04"

   fl_wait(tCOM);          // wait before sending command
   put_cmd_ua(FL_COM_SET_OSC_FREQ, 5, fl_cmd_prm);

   rc = get_sfrm_ua(fl_ua_sfrm, tWT9_MAX); // get status frame
   // switch(rc) {
   //      //
   //      // case FLC_NO_ERR: return rc; break; // case [A]
   //      // case FLC_DFTO_ERR: return rc; break; // case [C]
   //      // default: return rc; break; // case [B]
   //   // }

   return rc;
}
```
4.7 Chip Erase Command

4.7.1 Processing sequence chart

Chip Erase command processing sequence

1. Wait from previous frame reception until next command transmission
2. Chip Erase command frame transmission
3. Time-out check for status frame reception
4. Status frame reception
4.7.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{com}$).

<2> The Chip Erase command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{wT1}$).

<4> The status code is checked.

   When ST1 = ACK: Normal completion [A]
   When ST1 $\neq$ ACK: Abnormal termination [B]

4.7.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
</tbody>
</table>
|                                | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
|                                | WRITE error | 1CH | An erase error has occurred. |
|                                | MRG10 error | 1AH | – |
|                                | MRG11 error | 1BH | – |
| Time-out error [C]             | –           | The status frame was not received within the specified time. |
4.7.4 Flowchart

Chip Erase command processing

Waits from previous frame reception until next command transmission \( t_{com} \)

Command frame transmission processing (Chip Erase)

Status frame received? No

Timed out? Yes

Time-out error [C]

Status = ACK? No

Yes

Normal completion [A]

Abnormal termination [B]
4.7.5 Sample program

The following shows a sample program for Chip Erase command processing.

```c
u16 fl ua_erase_all(void)
{
    u16 rc;

    fl_wait(tCOM);  // wait before sending command

    put_cmd_ua(FL_COM_ERASE_CHIP, 1, fl_cmd_prm); // send ERASE CHIP command

    rc = get_sfrm_ua(fl ua_sfrm, tWT1_MAX); // get status frame
// switch(rc) {
//   // case FLC_NO_ERR: return rc; break; // case [A]
//   // case FLC_DFTO_ERR: return rc; break; // case [C]
//   // default: return rc; break; // case [B]
// }
    return rc;
}
```
4.8 Block Erase Command

4.8.1 Processing sequence chart

Block Erase command processing sequence

Programmer

V850ES/Hx3

<1> Wait from previous frame reception until next command transmission

<2> Block Erase command frame transmission

<3> Time-out check for status frame reception

<4> Status frame reception

- Time-out error [C]
- Abnormal termination [B]
- Normal completion [A]

- Reception status [ACK/other than ACK]

- Erasure of specified blocks completed? [Yes/No]

- Yes
  - Go to <1>

- No
  - Time-out occurs
  - Status frame received within specified time

- ACK
  - Other than ACK

Application Note U19304EJ1V0AN
4.8.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{\text{COM}}$).

<2> The Block Erase command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception. If a time-out occurs, a time-out error [C] is returned (time-out time $t_{\text{WT2}}$).

<4> The status code is checked.

When ST1 = ACK: When the block erase for all of the specified blocks is not yet completed, processing changes the block number and re-executes the sequence from <1>.

When the block erase for all of the specified blocks is completed, the processing ends normally [A].

When ST1 ≠ ACK: Abnormal termination [B]

4.8.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
</tbody>
</table>
|                                | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
• Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
|                                | MRG10 error   | 1AH | An erase error has occurred. |
| Time-out error [C]             | –            | – | The status frame was not received within the specified time. |
4.8.4 Flowchart

Block Erase command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Block Erase)

Status frame received?

- Yes
  - Status = ACK?
    - Yes: Abnormal termination [B]
    - No: Erasure of specified blocks completed?
      - Yes: Normal completion [A]
      - No: Timed out?
        - Yes: Time-out error [C]
        - No: Status frame received?

- No: Timed out? 
  - Yes: Time-out error [C]
  - No: Status = ACK?
    - Yes: Abnormal termination [B]
    - No: Erasure of specified blocks completed?
      - Yes: Normal completion [A]
      - No: Timed out?
        - Yes: Time-out error [C]
        - No: Status frame received?
4.8.5 Sample program

The following shows a sample program for Block Erase command processing for one block.

```c
/****************************************************************/
/*                */
/* Erase block command */
/*                */
/****************************************************************/
/* [i] u16 sblk ... start block number */
/* [i] u16 eblk ... end block number */
/* [r] u16 ... error code */
/****************************************************************/

u16 fl_ua_erase_blk(u16 sblk, u16 eblk)
{
    u16 rc;
    u32 wt2_max;
    u32 top, bottom;

top = get_top_addr(sblk);  // get start address of start block
bottom = get_bottom_addr(eblk); // get end address of end block

set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

wt2_max = make_wt2_max(sblk, eblk);  // get tWT2(Max)

fl_wait(tCOM);  // wait before sending command

put_cmd_ua(FL_COM_ERASE_BLOCK, 7, fl_cmd_prm); // send ERASE CHIP command

rc = get_sfrm_ua(fl_ua_sfrm, wt2_max); // get status frame

    // switch(rc) {
    //     //
    //     //     case FLC_NO_ERR: return rc; break; // case [A]
    //     //     case FLC_DFTO_ERR: return rc; break; // case [C]
    //     //     default:        return rc; break; // case [B]
    //     // }

    return rc;
}
```
4.9 Programming Command

4.9.1 Processing sequence chart

Programmer V850ES/Hx3

Programming command processing sequence

- <1> Wait from previous frame reception until next command transmission
- <2> Programming command frame transmission
- <3> Time-out check for status frame reception
- <4> Status frame reception
- <5> Wait from previous frame reception until next data frame transmission
- <6> Data frame (user data) transmission
- <7> Time-out check for status frame reception
- <8> Status frame reception
- <9> Time-out check for status frame reception
- <10> Status frame reception

- Reception status [ACK/other than ACK]
- Reception status [ST1]
- Reception status [ST2]
- All data frames transmitted? [Yes/No]
- Abnormal termination [B]
- Abnormal termination [E]
- Abnormal termination [D]
- Normal completion [A]

- Time-out occurs
- Time-out error [C]
- Time-out error [C]
- Time-out error [C]

- Normal completion [A]
- Time-out error [C]
- Time-out error [C]
- Time-out error [C]
4.9.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{COM}$).

<2> The Programming command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT3}$).

<4> The status code is checked.
   - When ST1 = ACK: Proceeds to <5>.
   - When ST1 ≠ ACK: Abnormal termination [B]

<5> Waits from the previous frame reception until the next data frame transmission (wait time $t_{FDS}$).

<6> User data is transmitted by data frame transmission processing.

<7> A time-out check is performed from user data transmission until data frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT4}$).

<8> The status code (ST1/ST2) is checked (also refer to the processing sequence chart and flowchart).
   - When ST1 ≠ ACK: Abnormal termination [B]
   - When ST1 = ACK: The following processing is performed according to the ST2 value.
     - When ST2 = ACK: Proceeds to <9> when transmission of all data frames is completed.
       If there still remain data frames to be transmitted, the processing re-executes the
       sequence from <5>.
     - When ST2 ≠ ACK: Abnormal termination [D]

<9> A time-out check is performed until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT5}$).

<10> The status code is checked.
   - When ST1 = ACK: Normal completion [A]
   - When ST1 ≠ ACK: Abnormal termination [E]
### 4.9.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>The command was executed normally and the user data was written normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>05H</td>
<td>The specified start/end address is not the start/end address of the block.</td>
</tr>
<tr>
<td>Parameter error</td>
<td>07H</td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td>Checksum error</td>
<td>10H</td>
<td>Programming command is prohibited by the security setting.</td>
</tr>
<tr>
<td>Protect error</td>
<td></td>
<td>A command other than the Status command was received during processing.</td>
</tr>
<tr>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
<td>Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td></td>
<td>The status frame was not received within the specified time.</td>
</tr>
<tr>
<td>Abnormal termination [D]</td>
<td>1CH</td>
<td>A write error has occurred.</td>
</tr>
<tr>
<td>Abnormal termination [E]</td>
<td>1BH</td>
<td>An internal verify error has occurred.</td>
</tr>
</tbody>
</table>
4.9.4 Flowchart

[Flowchart diagram showing the UART communication mode process with decision points for status frame reception, command frame transmission, and data frame transmission, along with possible outcomes for normal completion and abnormal termination.

- Programming command processing
- Command frame transmission (Programming)
- Status frame received?
  - Yes -> Status = ACK? (Normal completion [A])
  - No -> Timed out? (Time-out error [C])
- All data frames transmitted?
  - Yes -> Status = ACK? (Normal completion [A])
  - No -> Data frame transmission (User program)
- Status frame received?
  - Yes -> ST1 = ACK? (Normal completion [A])
  - No -> Timed out? (Time-out error [C])
- ST2 = ACK?
  - Yes -> Abnormal termination [B]
  - No -> Abnormal termination [B]
- Status frame received?
  - Yes -> Status = ACK? (Normal completion [A])
  - No -> Timed out? (Time-out error [C])
- Timed out?
  - Yes -> Abnormal termination [B]
  - No -> Abnormal termination [B]
4.9.5 Sample program

The following shows a sample program for Programming command processing.

```c
#define fl_st2_ua (fl_ua_sfrm[OFS_STA_PLD+1])

u16 fl_ua_write(u32 top, u32 bottom)
{
    u16 rc;
    u32 send_head, send_size;
    bool is_end;
    u32 wt5_max;

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL
    wt5_max = make_wt5_max(get_block_num(top, bottom));

    // set params
    put_cmd_ua(FL_COM_WRITE, 7, fl_cmd_prm); // send "Programming" command
    rc = get_sfrm_ua(fl_ua_sfrm, tWT3_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

    // send user data
    while(1)
    {
        // make send data frame
        if ((bottom - send_head) > 256) { // rest size > 256 ?
            // make send data frame
            if ((bottom - send_head) > 256) { // rest size > 256 ?
```

```c
    Application Note U19304EJ1V0AN

83
```
is_end = false;  // yes, not is_end frame
send_size  = 256;  // transmit size = 256 byte

} else{
  is_end = true;
  send_size = bottom - send_head + 1;
  // transmit size = (bottom - send_head)+1 byte
}

memcpy(fl_txdata_frm, rom_buf+send_head, send_size);
// set data frame payload
send_head += send_size;

fl_wait(tFD3);  // wait before sending data frame

put_dfrm_ua(send_size, fl_txdata_frm, is_end); // send user data

rc = get_sfrm_ua(fl_ua_sfrm, tWT4_MAX);  // get status frame
switch(rc) {
  case FLC_NO_ERR:   break; // continue
  case FLC_DFTO_ERR: return rc; break; // case [C]
  default:  return rc; break; // case [B]
}

if (fl_st2_ua != FLST_ACK){  // ST2 = ACK ?
  rc = decode_status(fl_st2_ua); // No
  return rc;    // case [D]
}

if (is_end)
  break;

/************************************************/
/* Check internally verify                         */
/************************************************/
rc = get_sfrm_ua(fl_ua_sfrm, wt5_max); // get status frame again
switch(rc) {
  // case FLC_NO_ERR: return rc; break; // case [A]
  // case FLC_DFTO_ERR: return rc; break; // case [C]
  // default: return rc; break; // case [E]
}
return rc;
}
4.10 Verify Command

4.10.1 Processing sequence chart

Verify command processing sequence

Programmer

V850ES/Hx3

<1> Wait from previous frame reception until next command transmission (COM)

<2> Verify command frame transmission

<3> Time-out check for status frame reception

<4> Status frame reception

<5> Wait from previous frame reception until next data frame transmission (Xf63)

<6> Data frame (user data for verify) transmission

<7> Time-out check for status frame reception

<8> Status frame reception (ST1/ST2)

Status frame received within specified time

Reception status (ST1) [ACK/other than ACK]

ACK

Abnormal termination [B]

Other than ACK

Reception status (ST2) [ACK/other than ACK]

ACK

Abnormal termination [D]

No

Go to <5>

Yes

All data frames transmitted? [Yes/No]

Yes

Normal completion [A]

No

Time-out occurs

Time-out error [C]

Other than ACK

Abnormal termination [B]

Time-out occurs

Time-out error [C]

Other than ACK

Abnormal termination [B]
4.10.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{com}$).

<2> The Verify command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT}$).

<4> The status code is checked.

   - When ST1 = ACK: Proceeds to <5>.
   - When ST1 ≠ ACK: Abnormal termination [B]

<5> Waits from the previous frame reception until the next data frame transmission (wait time $t_{DFD}$).

<6> User data for verifying is transmitted by data frame transmission processing.

<7> A time-out check is performed from user data transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT}$).

<8> The status code (ST1/ST2) is checked (also refer to the processing sequence chart and flowchart).

   - When ST1 ≠ ACK: Abnormal termination [B]
   - When ST1 = ACK: The following processing is performed according to the ST2 value.
     * When ST2 = ACK: If transmission of all data frames is completed, the processing ends normally [A].
       If there still remain data frames to be transmitted, the processing re-executes the sequence from <5>.
     * When ST2 ≠ ACK: Abnormal termination [D]

4.10.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|                                 | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
   • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]              | –            | The status frame was not received within the specified time. |
| Abnormal termination [D]        | Verify error | 0FH | The verify has failed, or another error has occurred. |
4.10.4 Flowchart

Verify command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Verify)

Status frame received?

No

Wait from previous frame reception until next data frame transmission

Data frame transmission processing (User program)

Status frame received?

No

Timed out?

Yes

Time-out error [C]

No

ST1 = ACK?

Yes

Abnormal termination [B]

No

ST1 = ACK?

Yes

Abnormal termination [B]

No

ST2 = ACK?

Yes

Abnormal termination [D]

No

All data frames transmitted?

No

Yes

Normal completion [A]
4.10.5 Sample program
The following shows a sample program for Verify command processing.

```c
u16  fl ua verify(u32 top, u32 bottom, u8 *buf)
{
    u16  rc;
    u32  send_head, send_size;
    bool  is_end;

    // set params
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    // send command & check status
    fl_wait(tCOM);  // wait before sending command
    put_cmd_ua(FL_COM_VERIFY, 7, fl_cmd_prm);  // send VERIFY command
    rc = get_sfrm_ua(fl ua_sfrm, tWT6_MAX);  // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        case FLC_DFTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }

    // send user data
    send_head = top;
    while(1){
        if ((bottom - send_head) > 256){  // rest size > 256 ?
            is_end = false;  // yes, not is_end frame
            send_size = 256;  // transmit size = 256 byte
        }
```
else{
    is_end = true;
    send_size = bottom - send_head + 1;  // transmit size = (bottom - send_head)+1 byte
}
memcpy(fl_txdata_frm, buf+send_head, send_size);// set data frame payload
send_head += send_size);

fl_wait(tFD3);
put_dfrm_ua(send_size, fl_txdata_frm, is_end);  // send user data

rc = get_sfrm_ua(fl_uA_sfrm, tWT7_MAX);  // get status frame
switch(rc) {
    case FLC_NO_ERR: break; // continue
    // case FLC_DFTO_ERR: return rc; break; // case [C]
    default:  return rc; break; // case [B]
}
if (fl_st2_ua != FLST_ACK){ // ST2 = ACK ?
    rc = decode_status(fl_st2_ua); // No
    return rc; // case [D]
}
if (is_end) // send all user data ?
    break; // yes
//continue;
}
return FLC_NO_ERR;  // case [A]
4.11 Block Blank Check Command

4.11.1 Processing sequence chart

Block Blank Check command processing sequence
4.11.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time t_com).

<2> The Block Blank Check command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
    If a time-out occurs, a time-out error [C] is returned (time-out time t_wt8).

<4> The status code is checked.

    When ST1 = ACK: If the blank check for all of the specified blocks is not yet completed, processing
    changes the block number and re-executes the sequence from <1>.
    If the blank check for all of the specified blocks is completed, the processing ends
    normally [A].

    When ST1 ≠ ACK: Abnormal termination [B]

4.11.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
| Negative acknowledgment (NACK)  | 15H | • A command other than the Status command was received during processing.  
                                 |              | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| MRG11 error                     | 1BH | The specified block in the flash memory is not blank. |
| Time-out error [C]              | – | The status frame was not received within the specified time. |
4.11.4 Flowchart

- **Block Blank Check command processing**
  - Wait from previous frame reception until next command transmission
  - Command frame transmission processing (Block Blank Check)
  - Status frame received?
    - No
    - Status = ACK?
      - No
      - Blank check for all of specified blocks completed?
        - No
        - Yes
          - Normal completion [A]
      - Yes
    - Yes
      - Timed out?
        - No
        - Time-out error [C]
      - Yes
        - Abnormal termination [B]

4.11.5 Sample program

The following shows a sample program for Block Blank Check command processing for one block.

```c
/* *******************************************************
/* Block blank check command                             */
/* *******************************************************
/* [i] u16 sblk ... start block number                  */
/* [i] u16 eblk ... end block number                    */
/* [r] u16  ... error code                              */
/* *******************************************************
*/

u16  fl_ua_blk_blank_chk(u16 sblk, u16 eblk)
{
    u16  rc;
    u32  wt8_max;
    u32  top, bottom;

    top = get_top_addr(sblk);  // get start address of start block
    bottom = get_bottom_addr(eblk); // get end address of end block

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    wt8_max = make_wt8_max(sblk, eblk);  // get tWT8(Max)

    fl_wait(tCOM);  // wait before sending command

    put_cmd_ua(FL_COM_BLOCK_BLANK_CHK, 7, fl_cmd_prm);
    rc = get_sfrm_ua(fl_ua_sfrm, wt8_max+6*1000); // get status frame
    // switch(rc) {
    //     case FLC_NO_ERR: return rc; break; // case [A]
    //     case FLC_DFTO_ERR: return rc; break; // case [C]
    //     default: return rc; break; // case [B]
    // }
    return rc;
}
```
4.12 Silicon Signature Command

4.12.1 Processing sequence chart
4.12.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{com}$).
<2> The Silicon Signature command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception. If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT1}$).
<4> The status code is checked.

When ST1 = ACK: Proceeds to <5>.
When ST1 $\neq$ ACK: Abnormal termination [B]

<5> A time-out check is performed until data frame (silicon signature data) reception. If a time-out occurs, a time-out error [C] is returned (time-out time $t_{FD2}$).
<6> The received data frame (silicon signature data) is checked.

If data frame is normal: Normal completion [A]
If data frame is abnormal: Data frame error [D]

4.12.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|                               | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
|                               |                           |   | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]            | –                        | – | The status frame or data frame was not received within the specified time. |
| Data frame error [D]          | –                        | – | The checksum of the data frame received as silicon signature data does not match. |
4.12.4 Flowchart

Silicon Signature command processing

Wait from previous frame reception until next command transmission $t_{com}$

Command frame transmission processing (Silicon Signature)

Status frame received? No

Status = ACK? Yes

Abnormal termination [B]

Status = ACK? Yes

Data frame (silicon signature) received? No

Normal data frame? No

Data frame error [D]

Normal data frame? Yes

Time-out error [C]

Data frame error [D]

Normal completion [A]

Timed out? Yes

Time-out error [C]

Timed out? No

Timed out? Yes

Time-out error [C]

Timed out? No
4.12.5 Sample program

The following shows a sample program for Silicon Signature command processing.

```c
u16 fl_ua_getsig(u8 *sig)
{
    u16 rc;

    fl_wait(tCOM); // wait before sending command

    put_cmd_ua(FL_COM_GET_SIGNATURE, 1, fl_cmd_prm); // send GET SIGNATURE command

    rc = get_sfrm_ua(fl_ua_sfrm, tWT11_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        default: return rc; break; // case [B]
    }

    rc = get_dfrm_ua(fl_rxdata_frm, tFD2_MAX); // get status frame
    if (rc){ // if error
        return rc; // case [D]
    }

    memcpy(sig, fl_rxdata_frm+OFS_STA_PLD, fl_rxdata_frm[OFS_LEN]); // copy Signature data
    return rc; // case [A]
}
```
4.13 Version Get Command

4.13.1 Processing sequence chart

Version Get command processing sequence
4.13.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \(t_{com}\)).

<2> The Version Get command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error \([C]\) is returned (time-out time \(t_{WT1}\)).

<4> The status code is checked.
   
   When \(ST1 = \text{ACK}\): Proceeds to <5>.
   When \(ST1 \neq \text{ACK}\): Abnormal termination \([B]\)

<5> A time-out check is performed until data frame (version data) reception.
   If a time-out occurs, a time-out error \([C]\) is returned (time-out time \(t_{FD2}\)).

<6> The received data frame (version data) is checked.
   
   If data frame is normal: Normal completion \([A]\)
   If data frame is abnormal: Data frame error \([D]\)

4.13.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion ([A])</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination ([B])</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
| | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
| | | | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error \([C]\) | – | The status frame or data frame was not received within the specified time. |
| Data frame error \([D]\) | – | The checksum of the data frame received as version data does not match. |
4.13.4 Flowchart

Wait from previous frame reception until next command transmission

Command frame transmission processing (Version Get)

Status frame received?

Yes

Status = ACK?

Yes

Abnormal termination [B]

No

Status = ACK?

Yes

Data frame (version data) received?

No

No

Normal data frame?

Yes

Normal completion [A]

No

Data frame error [D]

Yes

Timed out? [tFD2]

No

Yes

Time-out error [C]

No

Timed out? [tWT12]

Yes

Time-out error [C]

No

Timed out? [tCOM]

Yes

Time-out error [C]
4.13.5 Sample program
The following shows a sample program for Version Get command processing.

```c
u16  fl_ua_getver(u8 *buf)
{
  u16  rc;

  fl_wait(tCOM);   // wait before sending command

  put_cmd_ua(FL_COM_GET_VERSION, 1, fl_cmd_prm); // send GET VERSION command

  rc = get_sfrm_ua(fl_ua_sfrm, tWT12_MAX);   // get status frame
  switch(rc) {
    case FLC_NO_ERR:    break;  // continue
    // case FLC_DFTO_ERR:  return rc; break;  // case [C]
    default:   return rc; break;  // case [B]
  }

  rc = get_dfrm_ua(fl_rxdata_frm, tFD2_MAX); // get data frame
  if (rc){
    return rc;   // case [D]
  }

  memcpy(buf, fl_rxdata_frm+OFS_STA_PLD, DFV_LEN); // copy version data
  return rc;    // case [A]
}```
4.14 Checksum Command

4.14.1 Processing sequence chart

Checksum command processing sequence

Programmer V850ES/Hx3

1. Wait from previous frame reception until next command transmission.
2. Checksum command frame transmission.
3. Time-out check for status frame reception.
5. Time-out check for status frame reception.
6. Data frame (checksum data) reception.
7. Data frame received within specified time.
8. Normal completion [A].
9. Data frame error [D].
10. Normal data frame? [Yes/No].
11. Yes.
12. Normal completion [A].
13. No.
14. Data frame error [D].
15. Abnormal termination [B].
16. Other than ACK.
17. ACK.
18. Reception status [ACK/other than ACK].
19. Time-out occurs.
20. Status frame received within specified time.
22. Normal completion [A].
23. Time-out error [C].
24. Time-out error [C].
25. Time-out error [C].
4.14.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{com}} \)).

<2> The Checksum command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT16}} \)).

<4> The status code is checked.
   
   When ST1 = ACK: Proceeds to <5>.
   When ST1 \( \neq \) ACK: Abnormal termination [B]

<5> A time-out check is performed until data frame (checksum data) reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{FD1}} \)).

<6> The received data frame (checksum data) is checked.
   
   If data frame is normal: Normal completion [A]
   If data frame is abnormal: Data frame error [D]

4.14.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK) 06H</td>
<td>The command was executed normally and checksum data was acquired normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error 05H</td>
<td>The specified start/end address is not the start/end address of the block.</td>
</tr>
<tr>
<td></td>
<td>Checksum error 07H</td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
</tbody>
</table>
|                                 | Negative acknowledgment (NACK) 15H | • A command other than the Status command was received during processing.  
                                          • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]              | – | The status frame or data frame was not received within the specified time. |
| Data frame error [D]            | – | The checksum of the data frame received as version data does not match. |
4.14.4 Flowchart

- Checksum command processing
- Wait from previous frame reception until next command transmission
- Command frame transmission processing (Checksum)
- Status frame received?
  - Yes: Status = ACK?
    - Yes: Abnormal termination [B]
    - No: Data frame (checksum data) received?
      - Yes: Normal data frame?
        - Yes: Normal completion [A]
        - No: Data frame error [D]
      - No: Time-out error [C]
  - No: Timed out? (t_FDI)
    - Yes: Time-out error [C]
    - No: Wait from previous frame reception until next command transmission [t_COM]
4.14.5 Sample program

The following shows a sample program for Checksum command processing.

```c
u16  fl_ua_getsum(u16 *sum, u32 top, u32 bottom)
{
    u16  rc;
    u32  fd1_max;

    // set params
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL
    fd1_max = get_fd1_max(get_block_num(top, bottom)); // get tFD1(MAX)

    // send command
    fl_wait(tCOM); // wait before sending command
    put_cmd_ua(FL_COM_GET_CHECK_SUM, 7, fl_cmd_prm); // send GET VERSION command

    rc = get_sfrm_ua(fl_rxdata_frm, tWT16_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        default:  return rc; break; // case [B]
    }

    // get data frame (Checksum data)
    rc = get_dfrm_ua(fl_rxdata_frm, fd1_max); // get status frame
    if (rc){
        return rc; // case [D]
    }

    *sum = (fl_rxdata_frm[OFS_STA_PLD] << 8) + fl_rxdata_frm[OFS_STA_PLD+1]; // set SUM data
    return rc; // case [A]
}
```
4.15 Security Set Command

4.15.1 Processing sequence chart

Security Set command processing sequence

Programmer V850ES/Hx3

1. Wait from previous frame reception until next command transmission

2. Security Set command frame transmission

3. Time-out check for status frame reception

4. Status frame reception

5. Wait from previous frame reception until data frame transmission

6. Data frame (security data) transmission

7. Time-out check for status frame reception

8. Status frame reception

9. Time-out check for status frame reception

10. Status frame reception

Reception status

ACK

Other than ACK

Abnormal termination [B]

Abnormal termination [A]

Time-out error [C]

Time-out error [D]

Time-out error [E]

Other than ACK

ACK

Status frame received within specified time

Status frame received within specified time
4.15.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{com}$).

<2> The Security Set command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT13}$).

<4> The status code is checked.

   When ST1 = ACK:  Proceeds to <5>.
   When ST1 $\neq$ ACK:  Abnormal termination [B]

<5> Waits from the previous frame reception until the next data frame transmission (wait time $t_{FD3}$).

<6> The data frame (security setting data) is transmitted by data frame transmission processing.

<7> A time-out check is performed until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT14}$).

<8> The status code is checked.

   When ST1 = ACK:  Proceeds to <9>.
   When ST1 $\neq$ ACK:  Abnormal termination [D]

<9> A time-out check is performed until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT15}$).

<10> The status code is checked.

   When ST1 = ACK:  Normal completion [A]
   When ST1 $\neq$ ACK:  Abnormal termination [E]
### 4.15.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
| Abnormal termination [B]        | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
• Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]              | –            | 15H | The status frame was not received within the specified time. |
| Abnormal termination [D]        | Negative acknowledgment (NACK) | 15H | The security data frame is abnormal. |
| Abnormal termination [D]        | Checksum error | 07H | The checksum of the transmitted security data frame does not match. |
| Abnormal termination [D]        | Protect error | 10H | When security data is in the following statuses  
• The security is changed from disabled to enabled.  
• The value of the last block number in the boot block cluster is changed when boot block cluster rewriting is disabled. |
| Abnormal termination [D]        | Parameter error | 05H | When security data is in the following statuses  
• The last block number of the boot block cluster is larger than the last block number of the device.  
• The value of the reset vector handler address is not 00000000H. |
| Abnormal termination [E]        | MRG10 error | 1AH | A write error has occurred. |
| Abnormal termination [E]        | MRG11 error | 1BH |
| Abnormal termination [E]        | WRITE error | 1CH |
4.15.4 Flowchart

Wait from previous frame reception until next command transmission

Command frame transmission processing (Security Set)

Status frame received?

Yes

Timed out?

No

Time-out error [C]

No

Abnormal termination [B]

No

Status = ACK?

Yes

Abnormal termination [E]

No

Wait from previous frame reception until next data frame transmission

Data frame transmission processing (Security data)

Status frame received?

Yes

Timed out?

No

Time-out error [C]

No

Status = ACK?

Yes

Abnormal termination [D]

No

Status = ACK?

Yes

Normal completion [A]

No

Abnormal termination [E]
4.15.5 Sample program

The following shows a sample program for Security Set command processing.

```c
u16  fl_ua_setscf(u8 scf, u8 bot, u32 vect)
{
  u16  rc;

  /*******************************************************************************/
  /*! set params */
  /*******************************************************************************/
  fl_cmd_prm[0] = 0x00;   // "BLK" (must be 0x00)
  fl_cmd_prm[1] = 0x00;   // "PAG" (must be 0x00)

  fl_txdata_frm[0] = scf|= 0b11100000; // "FLG" (bit 7,6,5 must be '1')
  fl_txdata_frm[1] = bot;   // "BOT"
  fl_txdata_frm[2] = (u8)(vect >> 16); // "ADH"
  fl_txdata_frm[3] = (u8)(vect >>  8); // "ADM"
  fl_txdata_frm[4] = (u8) vect;  // "ADL"

  /*******************************************************************************/
  /*! send command */
  /*******************************************************************************/
  put_cmd_ua(FL_COM_SET_SECURITY, 3, fl_cmd_prm);

  rc = get_sfrm_ua(fl_ua_sfrm, tWT13_MAX);  // get status frame
  switch(rc) {
    case FLC_NO_ERR:   break; // continue
    // case FLC_DFTO_ERR: return rc; break; // case [C]
    default:  return rc; break; // case [B]
  }

  /*******************************************************************************/
  /*! send data frame (security setting data) */
  /*******************************************************************************/

  fl_wait(tFD3);
  put_dfrm_ua(5, fl_txdata_frm, true);  // send security setting data

  rc = get_sfrm_ua(fl_ua_sfrm, tWT14_MAX);  // get status frame
  switch(rc) {
```
case FLC_NO_ERR: break; // continue
    // case FLC_DFTO_ERR: return rc; break; // case [C]
    default: return rc; break; // case [B]
}

/************************************************/
/* Check internally verify */
/************************************************/
rc = get_sfrm_ua(fl_ua_sfrm, tWT15_MAX); // get status frame
    // switch(rc) {
    //  case FLC_NO_ERR: return rc; break; // case [A]
    //  case FLC_DFTO_ERR: return rc; break; // case [C]
    //  default: return rc; break; // case [B]
    // }

return rc;
}
4.16 Read Command

4.16.1 Processing sequence chart

Read command processing sequence
4.16.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{com}$).
<2> The Read command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT17}$).
<4> The status code is checked.

   When ST1 = ACK: Proceeds to <5>.
   When ST1 ≠ ACK: Abnormal termination [B]

<5> A time-out check is performed until reception of the data frame reception result (user data).
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT19}$).
<6> The received data frame (user data) is checked.

   If data frame is normal: Proceeds to <9>.
   If data frame is abnormal: Proceeds to <7>.

<7> Waits from the previous frame reception until the next status (NACK) frame transmission (wait time $t_{WT19}$).
<8> The NACK frame is transmitted by data frame transmission processing.
   → A data frame error [D] is returned.
<9> Waits from the previous frame reception until the next status (ACK) frame transmission (wait time $t_{WT19}$).
<10> The ACK frame is transmitted by data frame transmission processing.

   When reception of all data frames is completed, normal completion [A] is returned.
   If there still remain data frames to be received, the processing re-executes the sequence from <5>.

4.16.3 Status at processing completion

<table>
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<th>Description</th>
</tr>
</thead>
<tbody>
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<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame or data frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as read data does not match.</td>
</tr>
</tbody>
</table>
4.16.4 Flowchart

Read command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Read)

Wait from previous frame reception until next status frame transmission

Status frame received?

Yes

ST1 = ACK?

Yes

Abnormal termination [B]

No

Timed out?

No

Data frame (user program) reception processing

Data frame received?

Yes

Data frame reception error?

No

Data frame received?

Yes

Data frame reception error?

No

Status frame received?

Yes

Timed out?

Yes

Time-out error [C]

No

Wait from previous frame reception until next status frame transmission

Status (NACK) frame transmission

Data frame error [D]

Wait from previous frame reception until next data frame transmission

Status (NACK) frame transmission

No

All data frames received?

Yes

Normal completion [A]

No
4.16.5 Sample program

The following shows a sample program for Read command processing.

```c
u16 fl_ua_read(u32 top, u32 bottom)
{
    u16 rc;
    u32 read_head;
    u16 len;
    u8 hooter;

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    fl_wait(tCOM); // wait before sending command
    put_cmd_ua(FL_COM_READ, 7, fl_cmd_prm);
    rc = get_sfrm_ua(fl_ua_sfrm, tWT17_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break;
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }

    read_head = top;
    while(1) {
        rc = get_dfrm_ua(fl_rxdata_frm, tWT18_MAX); // get ROM data from FLASH
        switch(rc) {
            case FLC_NO_ERR: break; // continue
            case FLC_DFTO_ERR: return rc; break; // case [C]
            // case FLC_RX_DFSUM_ERR:
            default:  // case [B]
                fl_wait(tWT19);
                put_sfrm_ua(FLST_NACK); // send status(NACK) frame
        }
    }
}
```
return rc;
break;
}
fl_wait(tWT19);
put_sfrm_us(FLST_ACK);
/**************************************************************************
/* save ROM data
/**************************************************************************/
if ((len = fl_rxdata_frm[OFS_LEN]) == 0) // get length
    len = 256;
memcpy(read_buf+read_head, fl_rxdata_frm+2, len); // save to external RAM
read_head += len;
/**************************************************************************
/* end check
/**************************************************************************/
hooter = fl_rxdata_frm[len + 3];
if (hooter == FL_ETB) // end frame ?
    continue; // no
break; // yes
return FLC_NO_ERR;
CHAPTER 5  3-WIRE SERIAL I/O COMMUNICATION MODE WITH HANDSHAKE SUPPORTED  
(CSI + HS)

5.1 Command Frame Transmission Processing Flowchart
5.2 Data Frame Transmission Processing Flowchart

[Flowchart diagram]

Data frame transmission processing

Data frame header (STX = 02H) transmission

HS pin = BUSY?

Yes
No

Timed out?

Yes
No

Data length (LEN) transmission

HS pin = BUSY?

Yes
No

Timed out?

Yes
No

LEN bytes transmitted?

Yes
No

Transmit 1-byte data

HS pin = BUSY?

Yes
No

Timed out?

Yes
No

Checksum data (SUM) transmission

HS pin = BUSY?

Yes
No

Timed out?

Yes
No

Last data frame?

Yes
No

Transmission of last data frame footer (ETX = 03H)

Transmission of footer other than those of last data frame (ETB = 17H)

End of data frame transmission
5.3 Data Frame Reception Processing Flowchart
5.4 Status Command

5.4.1 Processing sequence chart

Status command processing sequence

Programmer → V850ES/Hx3

1. Status command frame transmission

2. BUSY time-out check using HS pin

3. Status frame reception

- Reception status [ACK/other than ACK]
- Other than ACK
  - Abnormal termination [B]
  - Normal completion [A]

- ACK

- Time-out error [C]

- Time-out occurs

- BUSY release

- BUSY time-out check using HS pin

- Status command frame transmission
5.4.2 Description of processing sequence

<1> The Status command is transmitted by command frame transmission processing.

<2> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{SF}$).

<3> The status code is checked.

   When $ST1 = ACK$: Normal completion [A]
   When $ST1 \neq ACK$: Abnormal termination [B]

5.4.3 Status at processing completion

<table>
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<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Command error</td>
<td>04H</td>
</tr>
<tr>
<td></td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Write error</td>
<td>1CH</td>
</tr>
<tr>
<td></td>
<td>MRG10 error</td>
<td>1AH</td>
</tr>
<tr>
<td></td>
<td>MRG11 error</td>
<td>1BH</td>
</tr>
<tr>
<td></td>
<td>Verify error</td>
<td>0FH</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
</tbody>
</table>
5.4.4 Flowchart

Status command processing

Command frame transmission processing (Status)

HS pin = BUSY?

Yes

HS timed out?

Yes

Time-out error [C]

No

Status = ACK?

No

Abnormal termination [B]

Yes

Normal completion [A]

Status frame reception processing

No
5.4.5 Sample program
The following shows a sample program for Status command processing.

```c
static u16 fl_hs_getstatus(void)
{
    u16    rc;
    u32   retry = 0;

    rc = put_cmd_hs(FL_COM_GET_STA, 1, fl_cmd_prm); // send "Status" command
    if (rc)
        return rc; // case [C]

    if (hs_busy_to(tSF_MAX)) // HS-Busy t.o. ?
        return FLC_HSTO_ERR; // t.o. detected : case [C]

    if (rc = get_sfrm_hs(fl_rxdata_frm))
        return rc; // case [C] or [B(checksum error)]

    rc = decode_status(fl_st1); // decode return code
    return rc; // case [A] or [B]
}
```
5.5 Reset Command

5.5.1 Processing sequence chart

Note  Do not exceed the retry count for the reset command transmission (up to 16 times).
CHAPTER 5  3-WIRE SERIAL I/O COMMUNICATION MODE WITH HANDSHAKE SUPPORTED (CSI + HS)

5.5.2 Description of processing sequence

<1> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time tcom).

<2> The Reset command is transmitted by command frame transmission processing.

<3> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time tswt).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

   When the processing ends normally:  Normal completion [A]
   When the processing ends abnormally:  The sequence is re-executed from <1> if the retry count is not over.
   If the retry count is over, the processing ends abnormally [B].
   When a time-out error occurs:  A time-out error [C] is returned.

5.5.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H  The command was executed normally and synchronization between the programmer and the V850ES/Hx3 has been established.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H  The checksum of the transmitted command frame does not match.</td>
</tr>
</tbody>
</table>
|                                      | Negative acknowledgment (NACK) | 15H  • A command other than the Status command was received during processing.  
                                      |                                      | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]                   | –                        | Status check processing timed out. Processing timed out due to the busy status at the HS pin. |
5.5.4 Flowchart

- Reset command processing
  - HS pin = BUSY?
    - Yes
      - HS timed out?
        - Yes
          - Time-out error [C]
        - No
          - \( t_{\text{com}} \)
    - No
      - Command frame transmission processing (Reset)
  - \( t_{\text{com}} \)

- Status check processing
  - Result of status check processing = Abnormal termination?
    - Yes
      - Retry count over?
        - Yes
          - Abnormal termination [B]
        - No
          - \( t_{\text{wro}} \)
    - No
      - Result of status check processing = Time-out error?
        - Yes
          - \( t_{\text{com}} \)
        - No
          - No (normal completion)

- Normal completion [A]
5.5.5 Sample program
The following shows a sample program for Reset command processing.

```c
/******************* Reset command (CSI-HS) *******************/
/*                                                        */
/* Reset command (CSI-HS)                                */
/*                                                        */
/******************* Reset command (CSI-HS) *******************/
/* [r] u16     ... error code                            */
/******************* Reset command (CSI-HS) *******************/

u16 fl_hs_reset(void)
{
    u16 rc;
    u32 retry;

    for (retry = 0; retry < tRS; retry++){

        if (hs_busy_to(tCOM_MAX))
            return FLC_HSTO_ERR;   // t.o. detected :case [C]

        rc = put_cmd_hs(FL_COM_RESET, 1, fl_cmd_prm); // send "Reset" command
        if (rc)
            return rc;  // case [C]

        if (hs_busy_to(tWT0_MAX))
            return FLC_HSTO_ERR;   // t.o. detected :case [C]

        rc = fl_hs_getstatus(); // get status frame
        if (rc == FLC_ACK)  // ST1 = ACK ?
            break;   // case [A]
        //continue;   // case [B] (if exit from loop)

    }

    // switch(rc) {
    //     case FLC_NO_ERR: return rc; break; // case [A]
    //     case FLC_HSTO_ERR: return rc; break; // case [C]
    //     default:          return rc; break; // case [B]
    // }

    return rc;
}
```
5.6 Oscillating Frequency Set Command

5.6.1 Processing sequence chart

Oscillating Frequency Set command processing sequence
5.6.2 Description of processing sequence

<1> A V850ES/Hx3 BUSY status is checked using the HS pin. If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{com}$).

<2> The Oscillating Frequency Set command is transmitted by command frame transmission processing.

<3> A V850ES/Hx3 BUSY status is checked using the HS pin. If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{w79}$).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

When the processing ends normally: Normal completion [A]
When the processing ends abnormally: Abnormal termination [B]
When a time-out error occurs: A time-out error [C] is returned.

5.6.3 Status at processing completion

<table>
<thead>
<tr>
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</thead>
<tbody>
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<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|                                 | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
• Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]              | –             | Processing timed out due to the busy status at the HS pin. |
5.6.4 Flowchart

```
Oscillating Frequency Set command processing

HS pin = BUSY?
 No

Command frame transmission processing (Oscillating Frequency Set)

HS pin = BUSY?
 No

Status check processing

Timed out?
 Yes  t_CWS

Time-out error [C]

Time-out error?
 Yes  t_CWS

Time-out error [C]

Normal completion?
 No

Time-out error [C]

Yes

Normal completion [A]  Abnormal termination [B]
```
5.6.5 Sample program

The following shows a sample program for Oscillating Frequency Set command processing.

```c
/* *******************************************************/
/* */
/* Set Flash device clock value command (CSI-HS) */
/* */
/* *******************************************************/
/* [i] u8 clk[4] ... frequency data(D1-D4) */
/* [r] u16 ... error code */
/* *******************************************************/
/* *******************************************************/
u16 fl_hs_setclk(u8 clk[])
{
    u16 rc;

    fl_cmd_prm[0] = clk[0]; // "D01"
    fl_cmd_prm[1] = clk[1]; // "D02"
    fl_cmd_prm[2] = clk[2]; // "D03"
    fl_cmd_prm[3] = clk[3]; // "D04"

    if (hs_busy_to(tCOM_MAX))
        return FLC_HSTO_ERR; // t.o. detected :case [C]

    if (rc = put_cmd_hs(FL_COM_SET_OSC_FREQ, 5, fl_cmd_prm))
        // send "Oscillating Frequency Set" command
        return rc; // case [C]

    if (hs_busy_to(tWT9_MAX))
        return FLC_HSTO_ERR; // t.o. detected :case [C]

    rc = fl_hs_getstatus(); // get status frame
    // switch(rc) { 
    //     case FLC_NO_ERR: return rc; break; // case [A]
    //     case FLC_HSTO_ERR: return rc; break; // case [C]
    //     default: return rc; break; // case [B]
    // } }
    return rc;
}
```
5.7 Chip Erase Command

5.7.1 Processing sequence chart

Chip Erase command processing sequence

Programmer V850ES/Hx3

<1> BUSY time-out check using HS pin

<2> Chip Erase command frame transmission

<3> BUSY time-out check using HS pin

<4> Status check processing

<5> Result of status check processing

Result
[Normal completion/
Abnormal termination/
Time-out error]

Time-out error

Normal completion

Abnormal termination

Time-out error [C]

Normal completion [A]

Abnormal termination [B]

Time-out error [C]
5.7.2 Description of processing sequence

<1> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{cw} \)).
<2> The Chip Erase command is transmitted by command frame transmission processing.
<3> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{sm} \)).
<4> The status frame is acquired by status check processing.
<5> The following processing is performed according to the result of status check processing.

When the processing ends normally: Normal completion [A]
When the processing ends abnormally: Abnormal termination [B]
When a time-out error occurs: A time-out error [C] is returned.

5.7.3 Status at processing completion

<table>
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<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
</tbody>
</table>
|                                | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
                     |              |     | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
|                                | WRITE error  | 1CH | An erase error has occurred. |
|                                | MRG10 error  | 1AH | |
|                                | MRG11 error  | 18H | |
| Time-out error [C]             | –            | Processing timed out due to the busy status at the HS pin. |
5.7.4 Flowchart

- Chip Erase command processing

  - HS pin = BUSY?
    - Yes
      - Timed out?
        - Yes
          - Time-out error [C]
        - No
          - Command frame transmission processing (Chip Erase)
          - HS pin = BUSY?
            - Yes
              - Timed out?
                - Yes
                  - Time-out error [C]
                - No
                  - Status check processing
            - No
              - Normal completion?
                - Yes
                  - Abnormal termination [B]
                - No
                  - Time-out error [C]

Time-out error [C]
5.7.5 Sample program

The following shows a sample program for Chip Erase command processing.

```c
/******************************************************************
/*  
/* Erase all(chip) command (CSI-HS)  
/*  
/******************************************************************/
/* [r] u16 ... error code  */
*************************************************************************

u16 fl_hs_erase_all(void)
{
  u16 rc;

  if (hs_busy_to(tCOM_MAX))
    return FLC_HSTO_ERR;   // t.o. detected

  if (rc = put_cmd_hs(FL_COM_ERASE_CHIP, 1, fl_cmd_prm))
    return rc;    // case [C]

  if (hs_busy_to(tWT1_MAX))
    return FLC_HSTO_ERR;   // case [C]

  rc = fl_hs_getstatus();   // get status frame
  // switch(rc) {
  //   case FLC_NO_ERR: return rc; break; // case [A]
  //   case FLC_HSTO_ERR: return rc; break; // case [C]
  //   default: return rc; break; // case [B]
  // }
  return rc;
}
```
5.8 Block Erase Command

5.8.1 Processing sequence chart

Block Erase command processing sequence
5.8.2 Description of processing sequence

<1> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{\text{com}}$).

<2> The Block Erase command is transmitted by command frame transmission processing.

<3> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{\text{wt2}}$).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

   When the processing ends normally:  When the block erase for all of the specified blocks is not yet
       completed, processing changes the block number and re-executes
       the sequence from <1>.
   When the block erase for all of the specified blocks is completed,
       the processing ends normally [A].

   When the processing ends abnormally: Abnormal termination [B]

   When a time-out error occurs:  A time-out error [C] is returned.

5.8.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>The command was executed normally and block erase was performed normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>05H</td>
<td>The specified start/end address is not the start/end address of the block.</td>
</tr>
<tr>
<td></td>
<td>07H</td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td></td>
<td>10H</td>
<td>Block Erase command is prohibited by the security setting.</td>
</tr>
<tr>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
<td>• A command other than the Status command was received during processing.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td></td>
<td>1AH</td>
<td>An erase error has occurred.</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
</tbody>
</table>
5.8.4 Flowchart

Block Erase command processing

HS pin = BUSY?

Yes

Time out?

No

Command frame transmission processing (Block Erase)

HS pin = BUSY?

Yes

Timed out?

No

Status check processing

Timed out?

Yes

Time-out error [C]

No

Time-out error [C]

Erasure of specified blocks completed?

No

Abnormal termination [B]

Normal completion?

Yes

Normal completion [A]

No
5.8.5 Sample program

The following shows a sample program for Block Erase command processing for one block.

```c
u16  fl_hs_erase_blk(u16 sblk, u16 eblk)
{
    u16  rc;
    u32  wt2_max;

    u32  top, bottom;
    top = get_top_addr(sblk);    // get start address of start block
    bottom = get_bottom_addr(eblk); // get end address of end block

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL
    wt2_max = make_wt2_max(sblk, eblk);    // get tWT2(Max)

    if (hs_busy_to(tCOM_MAX))
        return FLC_HSTO_ERR;   // t.o. detected :case [C]

    if (rc = put_cmd_hs(FL_COM_ERASE_BLOCK, 7, fl_cmd_prm))
        return rc;    // case [C]

    if (hs_busy_to(wt2_max))
        return FLC_HSTO_ERR;   // t.o. detected :case [C]

    rc = fl_hs_getstatus();   // get status frame
    // switch(rc) {
    //     case FLC_NO_ERR: return rc; break; // case [A]
    //     case FLC_HSTO_ERR: return rc; break; // case [C]
    //     default: return rc; break; // case [B]
    // }
    return rc;
}
```
5.9 Programming Command

5.9.1 Processing sequence chart

[Diagram showing the processing sequence chart for programming command]
5.9.2 Description of processing sequence

<1> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{com} \)).

<2> The Programming command is transmitted by command frame transmission processing.

<3> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{wt3} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing:

    When the processing ends normally: Proceeds to <6>.
    When the processing ends abnormally: Abnormal termination [B]
    When a time-out error occurs: A time-out error [C] is returned.

<6> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{fd3} \)).

<7> User data is transmitted by data frame transmission processing.

<8> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{wt4} \)).

<9> The status frame is acquired by status check processing.

<10> The following processing is performed according to the result of status check processing (status code (ST1/ST2)) (also refer to the processing sequence chart and flowchart):

    When ST1 = abnormal termination: Abnormal termination [B]
    When ST1 = time-out error: A time-out error [C] is returned.
    When ST1 = normal completion: The following processing is performed according to the ST2 value.
        • When ST2 \( \neq \) ACK: Abnormal termination [D]
        • When ST2 = ACK: Proceeds to <11> when transmission of all of the user data is completed.
          If there still remain user data to be transmitted, the processing re-executes the sequence from <6>.

<11> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{wt5} \)).

<12> The status frame is acquired by status check processing.

<13> The following processing is performed according to the result of status check processing:

    When the processing ends normally: Normal completion [A]
        (Indicating that the internal verify check has performed normally after completion of write)
    When the processing ends abnormally: Abnormal termination [E]
        (Indicating that the internal verify check has not performed normally after completion of write)
    When a time-out error occurs: A time-out error [C] is returned.
### 5.9.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
</tbody>
</table>
|                                | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
• Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]             | –            | Processing timed out due to the busy status at the HS pin. |
| Abnormal termination [D]       | WRITE error  | 1CH | A write error has occurred. |
| Abnormal termination [E]       | MRG11error  | 1BH | An internal verify error has occurred. |
5.9.4 Flowchart
5.9.5 Sample program

The following shows a sample program for Programming command processing.

```c
u16 fl_hs_write(u32 top, u32 bottom)
{
    u16   rc;
    u32   send_head, send_size;
    bool  is_end;
    u32   wt5_max;

    if (hs_busy_to(tCOM_MAX))
        return FLC_HSTO_ERR; // t.o. detected

    if (rc = put_cmd_hs(FL_COM_WRITE, 7, fl_cmd_prm))// send "Programming" command
        return rc;       // t.o. detected

    if (hs_busy_to(tWT3_MAX))
        return FLC_HSTO_ERR; // t.o. detected

    rc = fl_hs_getstatus();   // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break;  // continue
        // case FLC_HSTO_ERR: return rc; // case [C]
        default:  return rc; break;  // case [B]
    }

    send_head = top;

    while(1){
        // make send data frame
        if (((bottom - send_head) > 256){ // rest size > 256 ?
            is_end = false;  // yes, not end frame
            send_size = 256;  // transmit size = 256 byte
```
else{
    is_end = true;
    send_size = bottom - send_head + 1;
    // transmit size = (bottom - send_head)+1 byte
}
memcpy(fl_txdata_frm, rom_buf+send_head, send_size);
    // set data frame payload
send_head += send_size;

if (hs_busy_to(tFD3_MAX))  // t.o. check before sending data frame
    return FLC_HSTO_ERR;  // t.o. detected
if (rc = put_dfrm_hs(send_size, fl_txdata_frm, is_end))
    // send user data
    return rc;   // error detected
if (hs_busy_to(tWT4_MAX))
    return FLC_HSTO_ERR;  // t.o. detected

rc = fl hs_getstatus();  // get status frame
switch(rc) {
    case FLC_NO_ERR:   break; // continue
    // case FLC_HSTO_ERR: return rc; break; // case [C]
    default:  return rc; break; // case [B]
}
if (fl_st2 != FLST_ACK){   // ST2 = ACK ?
    rc = decode_status(fl_st2); // No
    return rc;    // case [D]
}
if (is_end)   // send all user data ?
    break;   // yes

}  //*********************************************************************************/
/* Check internally verify                                               */
/****************************************************************************/  
if (hs_busy_to(wt5_max))
    return FLC_HSTO_ERR;  // t.o. detected

rc = fl hs_getstatus();  // get status frame
switch(rc) {
    case FLC_NO_ERR:   return rc; break; // case [A]
    // case FLC_HSTO_ERR: return rc; break; // case [C]
    default:  return rc; break; // case [B]
}
return rc;
}
5.10 Verify Command

5.10.1 Processing sequence chart

Verify command processing sequence

Programmer

Verify command frame transmission

<2> Status check processing

<3> BUSY time-out check using HS pin

<4> Status check processing

<5> Result of status check processing

<6> BUSY time-out check using HS pin

<7> Data frame (user data for verify) transmission

<8> BUSY time-out check using HS pin

<9> Status check processing

<10> Result of status check processing (ST1/ST2)

V850ES/Hx3

Result

[Normal completion/
Abnormal termination/
Time-out error]

Abnormal termination

<1> BUSY time-out check using HS pin

Normal completion

<2> Verify command frame transmission

Abnormal termination

<3> BUSY time-out check using HS pin

<4> Status check processing

<5> Result of status check processing

<6> BUSY time-out check using HS pin

<7> Data frame (user data for verify) transmission

<8> BUSY time-out check using HS pin

<9> Status check processing

<10> Result of status check processing (ST1/ST2)

Reception status (ST1)

[Normal completion/
Abnormal termination/
Time-out error]

Normal completion

Reception status (ST2)

[ACK/other than ACK]

Abnormal termination

<1> BUSY time-out check using HS pin

Normal completion

<2> Verify command frame transmission

Abnormal termination

<3> BUSY time-out check using HS pin

<4> Status check processing

<5> Result of status check processing

<6> BUSY time-out check using HS pin

<7> Data frame (user data for verify) transmission

<8> BUSY time-out check using HS pin

<9> Status check processing

<10> Result of status check processing (ST1/ST2)

All data frames transmitted?
[Yes/No]

Yes

Normal completion [A]

No

Go to <6>

Abnormal termination [C]

Time-out [C]

Time-out occurs

Time-out error

Other than ACK

Abnormal termination [D]

ACK
5.10.2 Description of processing sequence

<1> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{com}$).
<2> The Verify command is transmitted by command frame transmission processing.
<3> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{wtr}$).
<4> The status frame is acquired by status check processing.
<5> The following processing is performed according to the result of status check processing.

    When the processing ends normally: Proceeds to <6>.
    When the processing ends abnormally: Abnormal termination [B]
    When a time-out error occurs: A time-out error [C] is returned.

<6> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{fda}$).
<7> User data for verifying is transmitted by data frame transmission processing.
<8> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{wtr}$).
<9> The status frame is acquired by status check processing.
<10> The following processing is performed according to the result of status check processing (status code (ST1/ST2)) (also refer to the processing sequence chart and flowchart).

    When ST1 = abnormal termination: Abnormal termination [B]
    When ST1 = time-out error: A time-out error [C] is returned.
    When ST1 = normal completion: The following processing is performed according to the ST2 value.
        • When ST2 = ACK: If transmission of all data frames is completed, the processing ends normally [A].
          If there still remain data frames to be transmitted, the processing re-executes the sequence from <6>.
        • When ST2 ≠ ACK: Abnormal termination [D]
### 5.10.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td>Checksum error</td>
<td>07H</td>
<td>The checksum of the transmitted command frame or data frame does not match.</td>
</tr>
</tbody>
</table>
|Negative acknowledgment (NACK)                  | 15H | • A command other than the Status command was received during processing.  
• Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]                              | – | Processing timed out due to the busy status at the HS pin.                                                                                   |
| Abnormal termination [D]                        | Verify error | 0FH | The verify has failed, or another error has occurred.                                                                                      |
5.10.4 Flowchart

Verify command processing

HS pin = BUSY?

No

Command frame transmission processing (Verify)

Timed out?

Yes

Time-out error [C]

No

Status check processing

Time-out error?

Yes

Normal completion?

No

Abnormal termination [B]

Yes

Abnormal termination [B]

HS pin = BUSY?

No

Data frame transmission processing (User program)

Timed out?

Yes

Time-out error [C]

No

Status check processing

Time-out error?

Yes

Normal completion?

No

Abnormal termination [B]

Yes

Abnormal termination [B]

ST2 = ACK?

Yes

Abnormal termination [D]

No

All data frames transmitted?

Yes

Normal completion [A]

No
5.10.5 Sample program

The following shows a sample program for Verify command processing.

```c
u16  fl_hs_verify(u32 top, u32 bottom, u8 *buf)
{
    u16  rc;
    u32  send_head, send_size;
    bool  is_end;

    /*****************************************************************
     /*               */
     /* Verify command (CSI-HS) */
     /*               */
     /*****************************************************************/
    u16  rc;
    u32  send_head, send_size;
    bool  is_end;

    /*****************************************************************
     /* set params */
     /*****************************************************************
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    /*****************************************************************
     /* send command & check status */
     /*****************************************************************
    if (hs_busy_to(tCOM_MAX))
        return FLC_HSTO_ERR; // t.o. detected

    if (rc = put_cmd_hs(FL_COM_VERIFY, 7, fl_cmd_prm)) // send "Verify" command
        return rc; // error detected

    if (hs_busy_to(tWT6_MAX))
        return FLC_HSTO_ERR; // t.o. detected

    rc = fl_hs_getstatus(); // get status frame
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        case FLC_HSTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

    /*****************************************************************
     /* send user data */
     /*****************************************************************
    send_head = top;

    while(1){
```

// make send data frame
if ((bottom - send_head) > 256) { // rest size > 256 ?
    is_end = false; // yes, not is_end frame
    send_size = 256; // transmit size = 256 byte
} else {
    is_end = true;
    send_size = bottom - send_head + 1;
    // transmit size = (bottom - send_head)+1 byte
}
memcpy(fl_txdata_frm, buf+send_head, send_size);// set data frame payload
send_head += send_size;

if (hs_busy_to(tFD3_MAX))
    return FLC_HSTO_ERR; // t.o. detected

if (rc = put_dfrm_hs(send_size, fl_txdata_frm, is_end))
    // send user data
    return rc; // error detected

if (hs_busy_to(tWT7_MAX))
    return FLC_HSTO_ERR; // t.o. detected

rc = f1_hs_getstatus(); // get status frame
switch(rc) {
    case FLC_NO_ERR: break; // continue
    // case FLC_HSTO_ERR: return rc; // case [C]
    default: return rc; break; // case [B]
}
if (fl_st2 != FLST_ACK) // ST2 = ACK ?
    rc = decode_status(fl_st2); // No
    return rc; // case [D]

if (is_end) // send all user data ?
    break; // yes

return FLC_NO_ERR; // case [A]
5.11 Block Blank Check Command

5.11.1 Processing sequence chart

Block Blank Check command processing sequence
5.11.2 Description of processing sequence

<1> A V850ES/Hx3 BUSY status is checked using the HS pin. If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{COM} \)).

<2> The Block Blank Check command is transmitted by command frame transmission processing.

<3> A V850ES/Hx3 BUSY status is checked using the HS pin. If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT8} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

When the processing ends abnormally: Abnormal termination [B]

When the processing ends normally: If the blank check for all of the specified blocks is completed, the processing ends normally [A]. If the blank check for all of the specified blocks is not yet completed, processing changes the block number and re-executes the sequence from <1>.

When a time-out error occurs: A time-out error [C] is returned.

5.11.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
<td>• A command other than the Status command was received during processing. • Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>MRG11 error</td>
<td>1BH</td>
<td>The specified block in the flash memory is not blank.</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td></td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
</tbody>
</table>
5.11.4 Flowchart

Block Blank Check command processing

HS pin = BUSY?

Yes

No

Command frame transmission processing (Block Blank Check)

HS pin = BUSY?

Yes

No

Status check processing

Timed out?

Yes

No

Time-out error [C]

Time-out error [C]

Time-out error [C]

Abnormal termination [B]

Normal completion?

Yes

No

Blank check for all of specified blocks completed?

Yes

No

Normal completion [A]
5.11.5 Sample program
The following shows a sample program for Block Blank Check command processing for one block.

```c
u16  fl_hs_blk_blank_chk(u16 sblk, u16 eblk)
{
    u16  rc;
    u32  wt8_max;
    u32  top, bottom;

    top = get_top_addr(sblk);  // get start address of start block
    bottom = get_bottom_addr(eblk); // get end address of end block
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    wt8_max = make_wt8_max(sblk, eblk);  // get tWT8(Max)

    if (hs_busy_to(tCOM_MAX))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]

    if (rc = put_cmd_hs(FL_COM_BLOCK_BLANK_CHK, 7, fl_cmd_prm))
        return rc;  // send "Block Blank Check" command

    if (hs_busy_to(wt8_max))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]

    rc = fl_hs_getstatus();  // get status frame
    switch(rc) {
    case FLC_NO_ERR:  return rc; break;  // case [A]
    case FLC_HSTO_ERR:  return rc; break;  // case [C]
    default:  return rc; break;  // case [B]
    }
    return rc;

```
5.12 Silicon Signature Command

5.12.1 Processing sequence chart

Silicon Signature command processing sequence

Programmer

1. BUSY time-out check using HS pin

2. Silicon Signature command frame transmission

3. BUSY time-out check using HS pin

4. Status check processing

5. Result of status check processing

V850ES/Hx3

6. BUSY time-out check using HS pin

7. Data frame (silicon signature) reception processing

Result

[Normal completion/Abnormal termination/Time-out error]

Abnormal termination [B]

Normal completion [A]

Abnormal termination [C]

Data frame error [D]

Normal completion [A]

Yes

No

Time-out error [C]

Time-out occurs
5.12.2 Description of processing sequence

<1> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{COM} \)).

<2> The Silicon Signature command is transmitted by command frame transmission processing.

<3> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT1} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

   When the processing ends normally: Proceeds to <6>.
   When the processing ends abnormally: Abnormal termination [B]
   When a time-out error occurs: A time-out error [C] is returned.

<6> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{FD2} \)).

<7> The received data frame (silicon signature data) is checked.

   If data frame is normal: Normal completion [A]
   If data frame is abnormal: Data frame error [D]

5.12.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>The command was executed normally and the silicon signature was acquired normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>07H</td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
</tbody>
</table>
|                                 | 15H         | • A command other than the Status command was received during processing.  
|                                 |             | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]              | –           | Processing timed out due to the busy status at the HS pin. |
| Data frame error [D]            | –           | The checksum of the data frame received as silicon signature data does not match. |
5.12.4 Flowchart

```
Silicon Signature command processing

HS pin = BUSY?
   Yes
   Timed out?
      Yes
      Time-out error [C]
      No
   No

Command frame transmission processing (Silicon Signature)

HS pin = BUSY?
   Yes
   Timed out?
      Yes
      Time-out error [C]
      No
   No

Status check processing

Time-out error?
   Yes
   No
   Normal completion?
      Yes
      Abnormal termination [B]
      No

Data frame reception processing

Normal data frame?
   Yes
   Normal completion [A]
   No

Abnormal termination [B]
```

Yes

Time-out error [C]

No

Time-out [C]

No

Time-out error [C]
5.12.5 Sample program
The following shows a sample program for Silicon Signature command processing.

```c
/**
 * Get silicon signature command (CSI-HS)
 */
*****************************************************************
/* [i] u8 *sig... pointer to signature save area */
/* [r] u16 ... error code */
*****************************************************************

u16 fl_hs_getsig(u8 *sig)
{
    u16 rc;
    if (hs_busy_to(tCOM_MAX))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]
    if (rc = put_cmd_hs(FL_COM_GET_SIGNATURE, 1, fl_cmd_prm))
        // send "Silicon Signature" command
        return rc;   // error detected :case [C]
    if (hsBusyTo(tWT11_MAX))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]
    rc = fl_hs_getstatus();  // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        // case FLC_HSTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }
    if (hs_busy_to(tFD2_MAX))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]
    rc = get_dfrm_hs(fl_rxdata_frm); // get signature data
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        // case FLC_HSTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [D]
    }
    memcpy(sig, fl_rxdata_frm+OFS_STA_PLD, fl_rxdata_frm[OFS_LEN]);
    // copy Signature data
    return rc;    // case [A]
}
```
5.13 Version Get Command

5.13.1 Processing sequence chart

Version Get command processing sequence

Diagram showing the processing sequence from the Programmer to V850ES/Hx3.

- Step 1: BUSY time-out check using HS pin (COM)
- Step 2: Version Get command frame transmission
- Step 3: BUSY time-out check using HS pin
- Step 4: Status check processing
- Step 5: Result of status check processing
- Step 6: BUSY time-out check using HS pin
- Step 7: Data frame (version data) reception processing

Flowchart includes decision points for normal completion, abnormal termination, time-out error, and data frame error.
5.13.2 Description of processing sequence

<1> A V850ES/Hx3 BUSY status is checked using the HS pin. If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{com} \)).

<2> The Version Get command is transmitted by command frame transmission processing.

<3> A V850ES/Hx3 BUSY status is checked using the HS pin. If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{wait} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

- When the processing ends normally: Proceeds to <6>.
- When the processing ends abnormally: Abnormal termination [B]
- When a time-out error occurs: A time-out error [C] is returned.

<6> A V850ES/Hx3 BUSY status is checked using the HS pin. If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{req} \)).

<7> The received data frame (version data) is checked.

- If data frame is normal: Normal completion [A]
- If data frame is abnormal: Data frame error [D]

5.13.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|                                 | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
|                                 |                           |     | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]              | –                       | Processing timed out due to the busy status at the HS pin. |
| Data frame error [D]            | –                       | The checksum of the data frame received as version data does not match. |
5.13.4 Flowchart

[Flowchart Diagram]

- Version Get command processing
- Command frame transmission processing (Version Get)
- Status check processing
- Data frame reception processing

Decision Points:
- HS pin = BUSY?
- Time-out?
- Normal completion?
- Normal data frame?

Errors:
- Time-out error
- Abnormal termination
- Data frame error

Steps:
- Yes
- No
5.13.5 Sample program

The following shows a sample program for Version Get command processing.

```c
/* *************************************************************************/
/* Get device/firmware version command (CSI-HS) */
/* *************************************************************************/
/* [i]  u8  *buf     ... pointer to version date save area */
/* [r]   u16       ... error code */
/* *************************************************************************/
u16  fl_hs_getver(u8 *buf)
{
    u16  rc;

    if (hs_busy_to(tCOM_MAX))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]

    if (rc = put_cmd_hs(FL_COM_GET_VERSION, 1, fl_cmd_prm))
        // send "Version Get" command
        return rc;   // error detected :case [C]

    if (hs_busy_to(tWT12_MAX))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]

    rc = fl_hs_getstatus();  // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        default:  return rc; break; // case [B]
    }

    if (hs_busy_to(tFD2_MAX))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]

    rc = get_dfrm_hs(fl_rxdata_frm);  // get signature data
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        default:  return rc; break; // case [D]
    }

    memcpy(buf, fl_rxdata_frm+OFS_STA_PLD, DFV_LEN); // copy version data
    return rc;    // case [A]
}
```
5.14 Checksum Command

5.14.1 Processing sequence chart

Checksum command processing sequence

Programmer

<1> BUSY time-out check using HS pin

<2> Checksum command frame transmission

<3> BUSY time-out check using HS pin

<4> Status check processing

<5> Result of status check processing

V850ES/Hx3

<6> BUSY time-out check using HS pin

<7> Data frame (checksum data) reception processing

Result [Normal completion/ Abnormal termination/ Time-out error]

Time-out error [C]

Abnormal termination [B]

Normal completion [A]

Data frame error [D]

Normal data frame? [Yes/No]

Abnormal termination

Time-out occurs

BUSY release

<1> BUSY time-out check using HS pin

<3> BUSY time-out check using HS pin

<6> BUSY time-out check using HS pin

Time-out occurs

Time-out occurs

Time-out occurs

<2> Checksum command frame transmission

<4> Status check processing
5.14.2 Description of processing sequence

<1> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{COM} \)).

<2> The Checksum command is transmitted by command frame transmission processing.

<3> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT16} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

   When the processing ends normally:  Proceeds to <6>.
   When the processing ends abnormally:  Abnormal termination [B]
   When a time-out error occurs:   A time-out error [C] is returned.

<6> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{FD1} \)).

<7> The received data frame (checksum data) is checked.

   If data frame is normal:   Normal completion [A]
   If data frame is abnormal:  Data frame error [D]

5.14.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|                                 | Negative acknowledgment (NACK) | 15H         | • A command other than the Status command was received during processing.
|                                 |              |             | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]             | –            | Processing timed out due to the busy status at the HS pin. |
| Data frame error [D]           | –            | The checksum of the data frame received as version data does not match. |
5.14.4 Flowchart

- **Checksum command processing**
  - HS pin = BUSY?
    - Yes: Timed out?
      - Yes: Time-out error [C]
      - No: Command frame transmission processing (Checksum)
    - No: Timed out?
      - Yes: Time-out [C]
      - No: Status check processing
  - No: Normal completion?
    - Yes: Abnormal termination [B]
    - No: HS pin = BUSY?
      - Yes: Timed out?
        - Yes: Time-out error [C]
        - No: Data frame reception processing
      - No: Normal data frame?
        - Yes: Normal completion [A]
        - No: Data frame error [D]

- Normal completion [A]
- Time-out error [C]
5.14.5 Sample program

The following shows a sample program for Checksum command processing.

```c
u16  fl_hs_getsum(u16 *sum, u32 top, u32 bottom)
{
    u16  rc;
    u32  fd1_max;
    
    set_range_prm(fl_cmd_prm, top, bottom);  // set SAH/SAM/SAL, EAH/EAM/EAL
    fd1_max = get_fd1_max(get_block_num(top, bottom));  // get tFD1(Max)

    if (hs_busy_to(tCOM_MAX))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]

    if (rc = put_cmd_hs(FL_COM_GET_CHECK_SUM, 7, fl_cmd_prm))// send "Checksum" command
        return rc;   // error detected :case [C]

    if (hs_busy_to(tWT16_MAX))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]

    rc = fl_hs_getstatus();  // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        // case FLC_HSTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }

    if (hs_busy_to(fd1_max))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]

    rc = get_dfrm_hs(fl_rxdata_frm); // get sum data
```
switch(rc) {
    case FLC_NO_ERR: break; // continue
    default: return rc; break; // case [D]
}

*sum = (fl_rxdata_frm[OFS_STA_PLD] << 8) + fl_rxdata_frm[OFS_STA_PLD+1];
        // set SUM data
return rc;  // case [A]
5.15 Security Set Command

5.15.1 Processing sequence chart

Security Set command processing sequence

Programmer V850ES/Hx3

1. BUSY time-out check using HS pin
2. Security Set command frame transmission
3. BUSY time-out check using HS pin
4. Status check processing
5. Result of status check processing
6. BUSY time-out check using HS pin
7. Data frame transmission (security data)
8. BUSY time-out check using HS pin
9. Status check processing
10. Result of status check processing
11. BUSY time-out check using HS pin
12. Status check processing
13. Result of status check processing
5.15.2 Description of processing sequence

<1> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{conn} \)).

<2> The Security Set command is transmitted by command frame transmission processing.

<3> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT13} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

    When the processing ends normally: Proceeds to <6>.
    When the processing ends abnormally: Abnormal termination [B]
    When a time-out error occurs: A time-out error [C] is returned.

<6> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{PDO} \)).

<7> The data frame (security setting data) is transmitted by data frame transmission processing.

<8> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT14} \)).

<9> The status frame is acquired by status check processing.

<10> The following processing is performed according to the result of status check processing.

    When the processing ends normally: Proceeds to <11>.
    When the processing ends abnormally: Abnormal termination [D]
    When a time-out error occurs: A time-out error [C] is returned.

<11> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT15} \)).

<12> The status frame is acquired by status check processing.

<13> The following processing is performed according to the result of status check processing.

    When the processing ends normally: Normal completion [A]
    When the processing ends abnormally: Abnormal termination [E]
    When a time-out error occurs: A time-out error [C] is returned.
5.15.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|  | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
• Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C] | – | The status frame was not received within the specified time. |
| Abnormal termination [D] | Negative acknowledgment (NACK) | 15H | The security data frame is abnormal. |
|  | Checksum error | 07H | The checksum of the transmitted security data frame does not match. |
|  | Protect error | 10H | When security data is in the following statuses  
• The security is changed from disabled to enabled.  
• The value of the last block number in the boot block cluster is changed when boot block cluster rewriting is disabled. |
|  | Parameter error | 05H | When security data is in the following statuses  
• The last block number of the boot block cluster is larger than the last block number of the device.  
• The value of the reset vector handler address is not 00000000H. |
| Abnormal termination [E] | MRG10 error | 1AH | A write error has occurred. |
|  | MRG11 error | 1BH | |
|  | WRITE error | 1CH | |
5.15.4 Flowchart

[Flowchart diagram]

- Security Set command processing
- HS pin = BUSY?
  - Yes: Time-out error
  - No: Command frame transmission processing (Security Set)
- Status check processing
  - Time-out error?
    - Yes: Time-out error
    - No: Normal completion?
- Abnormal termination
- Status check processing
  - HS pin = BUSY?
    - Yes: Time-out error
    - No: Data frame transmission processing (Security data)
- Status check processing
  - Status = ACK?
    - Yes: Normal completion
    - No: Time-out error
- Abnormal termination
- Status check processing
  - HS pin = BUSY?
    - Yes: Time-out error
    - No: Status check processing
- Normal completion?
5.15.5 Sample program
The following shows a sample program for Security Set command processing.

```c
u16 fl_hs_setscf(u8 scf, u8 bot, u32 vect)
{
    u16 rc;

    fl_cmd_prm[0] = 0x00;       // "BLK" (must be 0x00)
    fl_cmd_prm[1] = 0x00;       // "PAG" (must be 0x00)

    fl_txdata_frm[0] = scf|0b11100000;    // "FLG" (bit 7,6,5 must be '1')
    fl_txdata_frm[1] = bot;    // "BOT"
    fl_txdata_frm[2] = (u8)(vect >> 16);  // "ADH"
    fl_txdata_frm[3] = (u8)(vect >> 8);  // "ADM"
    fl_txdata_frm[4] = (u8) vect;  // "ADL"

    if (hs_busy_to(tCOM_MAX))
        return FLC_HSTO_ERR; // t.o. detected :case [C]

    if (rc = put_cmd_hs(FL_COM_SET_SECURITY, 3, fl_cmd_prm))
        return rc;   // error detected :case [C]

    if (hs_busy_to(tWT13_MAX))
        return FLC_HSTO_ERR; // t.o. detected :case [C]

    rc = fl_hs_getstatus();                // get status frame
    switch(rc) {
        case FLC_NO_ERR:  break;  // continue
        case FLC_HSTO_ERR: return rc;  break;  // case [C]
        default:  return rc; break;  // case [B]
    }
}
```
/*******************************/
/* send data frame (security setting data) */
/*******************************/
if (hs_busy_to(tFD3_MAX))
    return FLC_HSTO_ERR; // t.o. detected :case [C]

if (rc = put_dfrm_hs(5, fl_txdata_frm, true)) // send security setting data
    return rc; // error detected :case [C]

if (hs_busy_to(tWT14_MAX))
    return FLC_HSTO_ERR; // t.o. detected :case [C]

rc = fl_hs_getstatus(); // get status frame
switch(rc) {
    case FLC_NO_ERR:   break; // continue
    default:  return rc; break; // case [B]
}

/*******************************/
/* Check internally verify */
/*******************************/
if (hs_busy_to(tWT15_MAX))
    return FLC_HSTO_ERR; // t.o. detected

rc = fl_hs_getstatus(); // get status frame again
switch(rc) {
    case FLC_NO_ERR: return rc; break; // case [A]
    default:  return rc; break; // case [B]
}

return rc;
5.16 Read Command

5.16.1 Processing sequence chart

[Diagram showing the processing sequence for the read command]
5.16.2 Description of processing sequence

<1> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{COM}$).

<2> The Read command is transmitted by command frame transmission processing.

<3> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{CNT17}$).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

   When the processing ends normally: Proceeds to <6>.
   When the processing ends abnormally: Abnormal termination [B]
   When a time-out error occurs: A time-out error [C] is returned.

<6> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{CNT19}$).

<7> The data frame (user data) in the flash memory is received by data frame reception processing.

   When the processing ends normally: Proceeds to <10>.
   When an error such as checksum error occurs: Proceeds to <8>.
   When a time-out error occurs: A time-out error [C] is returned.

<8> A V850ES/Hx3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{CNT19}$).

<9> The NACK frame is transmitted by data frame transmission processing.
   A data frame error [D] is returned.

<10> A V850ES/Hx3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{CNT19}$).

<11> The ACK frame is transmitted by data frame transmission processing.
    When reception of all data frames is completed, the normal completion status [A] is returned.
    If there still remain data frames to be received, the sequence is re-executed from <6>. 
## 5.16.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>The command was executed normally and the read data was set normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>05H</td>
<td>The specified start/end address is not the start/end address of the block.</td>
</tr>
<tr>
<td>Checksum error</td>
<td>07H</td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td>Protect error</td>
<td>10H</td>
<td>Read is prohibited by the security setting.</td>
</tr>
<tr>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
<td>Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as read data does not match.</td>
</tr>
</tbody>
</table>
5.16.4 Flowchart

[Flowchart diagram showing the flow of operations and decision points based on various conditions such as HS pin status, command transmission processing, status check, time-out errors, and normal completions.]

Normal completion? Yes

Data frame (user program) reception processing

Timed out during data frame reception? Yes

Normal completion? No

Status check processing

Time-out error? Yes

Normal completion? Yes

Abnormal termination [B]

HS pin = BUSY? Yes

Command frame transmission processing (Read)

Timed out? Yes

Time-out error [C]

No

Status check processing

Time-out error? Yes

Normal completion? Yes

Abnormal termination [B]

Data frame (user program) reception processing

Timed out during data frame reception? Yes

Normal completion? No

HS pin = BUSY? Yes

Status (NACK) frame transmission

Timed out? Yes

Status (NACK) frame transmission

Yes

Normal completion [A]

All data frames received? No

No

Data frame error [D]

Time-out error [C]

Yes

Time-out error [C]

HS pin = BUSY? Yes

Status (ACK) frame transmission

Timed out? Yes

Time-out error [C]

No

Data frame error [D]

Time-out error [C]
5.16.5 Sample program

The following shows a sample program for Read command processing.

```c
u16 fl_hs_read(u32 top, u32 bottom)
{
    u16 rc;
    u32 read_head;
    u16 len;
    u8 hooter;

    // set params
    set_range_prm(fl_cmd_prm, top, bottom);
    // set SAH/SAM/SAL, EAH/EAM/EAL

    // send command & check status
    if (hs_busy_to(tCOM_MAX))
        return FLC_HSTO_ERR; // t.o. detected :case [C]

    if (rc = put_cmd_hs(FL_COM_READ, 7, fl_cmd_prm))
        return rc;

    if (hs_busy_to(tWT17_MAX))
        return FLC_HSTO_ERR; // t.o. detected :case [C]

    rc = fl_hs_getstatus(); // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        case FLC_HSTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }

    // receive user data
    read_head = top;
    while(1){
        if (hs_busy_to(tWT18_MAX))
            return FLC_HSTO_ERR; // t.o. detected :case [C]

        rc = get_dfrm_hs(fl_rxdata_frm); // get ROM data from FLASH
```

switch(rc) {
    case FLC_NO_ERR:       break; // continue
    case FLC_HSTO_ERR:     return rc; break; // case [C]

    // case FLC_RX_DFSUM_ERR:
    default:               // case [D]

        if (hs_busy_to(tWT19_MAX))
            return FLC_HSTO_ERR; // t.o. detected
        put_sfrm_hs(FLST_NACK);
        return rc;

    break;
}

if (hs_busy_to(tWT19_MAX))
    return FLC_HSTO_ERR; // t.o. detected

put_sfrm_hs(FLST_ACK);   // send status(ACK) frame

/************************************************/
/* save ROM data      *
/************************************************/
if ((len = fl_rxdata_frm[OFS_LEN]) == 0) // get length
    len = 256;

memcpy(read_buf+read_head, fl_rxdata_frm+2, len);
    // save to external RAM

read_head += len;

/************************************************/
/* end check     *
/************************************************/
    hooter = fl_rxdata_frm[len + 3];
    if (hooter == FL_ETB)   // end frame ?
        continue;          // no
    break;                // yes
}

return FLC_NO_ERR;
}
CHAPTER 6  3-WIRE SERIAL I/O COMMUNICATION MODE (CSI)

6.1 Command Frame Transmission Processing Flowchart

- Command frame transmission processing
  - Command frame header (SOH = 01H) transmission
    - Wait between data transmissions
      - Data length (LEN) transmission
        - Wait between data transmissions
          - Command number (COM) transmission
            - (LEN - 1) bytes transmitted?
              - Yes
                - Transmits 1-byte parameter
              - No
                - Wait between data transmissions
                  - Checksum data (SUM) transmission
                    - Wait between data transmissions
                      - Command frame footer (ETX = 03H) transmission
                        - End of command frame transmission
6.2 Data Frame Transmission Processing Flowchart

Data frame transmission processing

Data frame header (STX = 02H) transmission

Wait between data transmissions

Data length (LEN) transmission

LEN bytes transmitted?

Yes
No

Wait between data transmissions

Transmits 1-byte data

Wait between data transmissions

Checksum data (SUM) transmission

Wait between data transmissions

Last data frame?

No
Yes

Last data frame footer (ETX = 03H) transmission

Transmission of footer other than those of last data frame (ETB = 17H)

End of data frame transmission
6.3 Data Frame Reception Processing Flowchart

```
Data frame reception processing

Data frame header (STX = 02H) reception

Wait between data receptions

Data length (LEN) reception

Wait between data receptions

Receives 1-byte data

LEN bytes received? Yes

Wait between data receptions

Checksum data (SUM) reception

Wait between data receptions

Reception of last data frame footer (ETX = 03H) or footer other than those of last data frame (ETB = 17H)

Checksum error? Yes

End of data frame reception

Checksum error
```
6.4 Status Command

6.4.1 Processing sequence chart

Status command processing sequence

Note Applied specifications differ depending on the command executed.
6.4.2 Description of processing sequence

<1> The Status command is transmitted by command frame transmission processing.
<2> Waits from command transmission until status frame reception (wait time $t_{SF}$).
<3> The status code is checked.

When $ST1 = ACK$: Normal completion [A]
When $ST1 = BUSY$: A time-out check is performed. The time-out time ($t_{WTn}$) is given as a parameter for this processing.
If the processing is not timed out, the sequence is re-executed from <1>.
If a time-out occurs, a time-out error [C] is returned.
When $ST1 \neq ACK, BUSY$: Abnormal termination [B]

6.4.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Command error</td>
<td>04H</td>
</tr>
<tr>
<td></td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Write error</td>
<td>1CH</td>
</tr>
<tr>
<td></td>
<td>MRG10 error</td>
<td>1AH</td>
</tr>
<tr>
<td></td>
<td>MRG11 error</td>
<td>1BH</td>
</tr>
<tr>
<td></td>
<td>Verify error</td>
<td>0FH</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
</tbody>
</table>
6.4.4 Flowchart

Status command processing

Command frame transmission processing (Status)

Wait from command frame transmission until status frame reception $t_{sf}$

Status frame reception processing

Status = BUSY?

Yes

Timed out? $t_{wn}$

No

Status = ACK?

Yes

Normal completion [A]

No

Time-out error [C]

Status = ACK?

Yes

Abnormal termination [B]
6.4.5 Sample program

The following shows a sample program for Status command processing.

```c
static u16 fl_csi_getstatus(u32 limit)
{
    u16 rc;

    start_flto(limit);

    while(1){

        put_cmd_csi(FL_COM_GET_STA, 1, fl_cmd_prm);// send "Status" command frame
        fl_wait(tSF);  // wait

        rc = get_sfrm_csi(fl_rxdata_frm);    // get status frame

        switch(rc){
            case FLC_BUSY:
                if (check_flto())   // time out ?
                    return FLC_DFTO_ERR;  // Yes, time-out // case [C]
                continue;    // No, retry
            default:     // checksum error
                return rc;
            case FLC_NO_ERR:    // no error
                break;
        }

        if (fl_st1 == FLST_BUSY){   // ST1 = BUSY
            if (check_flto())       // time out ?
                return FLC_DFTO_ERR;  // Yes, time-out // case [C]
            continue;    // No, retry
        }

        if (fl_rxdata_frm[OFS_LEN]==2&&fl_st1==FLST_ACK&&fl_st2==FLST_BUSY){
            if (check_flto())       // time out ?
                return FLC_DFTO_ERR;  // Yes, time-out // case [C]
            continue;
        }

        break;    // ACK or other error (but BUSY)
    }

    rc = decode_status(fl_st1);  // decode status to return code
}
```

//
//  case FLC_NO_ERR: return rc; break; // case [A]
//  default: return rc; break; // case [B]
// }
return rc;
}
6.5 Reset Command

6.5.1 Processing sequence chart

Reset command processing sequence

Note: Do not exceed the retry count for the reset command transmission (up to 16 times).
6.5.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{COM} \)).

<2> The Reset command is transmitted by command frame transmission processing.

<3> Waits from command transmission until status check processing (wait time \( t_{WT0} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

   - When the processing ends normally: Normal completion [A]
   - When the processing ends abnormally: The sequence is re-executed from <1> if the retry count is not over. If the retry count is over, the processing ends abnormally [B].
   - When a time-out error occurs: A time-out error [C] is returned.

6.5.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>The command was executed normally and synchronization between the programmer and the V850ES/Hx3 has been established.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>07H</td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
<td>- A command other than the Status command was received during processing. - Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Status check processing timed out.</td>
</tr>
</tbody>
</table>
6.5.4 Flowchart

Reset command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Reset)

Wait from command frame transmission until status check

Status check processing

Result of status check processing = Abnormal termination?

Yes

Retry count over?

Yes

Abnormal termination [B]

No

No (normal completion)

Result of status check processing = Time-out error?

Yes

Normal completion [A]

Time-out error [C]

No
6.5.5 Sample program

The following shows a sample program for Reset command processing.

```c
/* Reset command (CSI) */

u16  fl_csi_reset(void)
{
    u16 rc;
    u32 retry;

    for (retry = 0; retry < tRS; retry++){

        fl_wait(tCOM);   // wait before sending command frame

        put_cmd_csi(FL_COM_RESET, 1, fl_cmd_prm);   // send "Reset" command frame

        fl_wait(tWT0);

        rc = fl_csi_getstatus(tWT0_MAX);  // get status

        if (rc == FLC_DFTO_ERR)  // timeout error ?
            break;    // yes // case [C]

        if (rc == FLC_ACK)   // Ack ?
            break;    // yes // case [A]

        //continue;     // case [B] (if exit from loop)
    }

    // switch(rc) {
    //
    //    case FLC_NO_ERR: return rc; break; // case [A]
    //    case FLC_DFTO_ERR: return rc; break; // case [C]
    //    default:          return rc; break; // case [B]
    // }

    return rc;
}
```
6.6 Oscillating Frequency Set Command

6.6.1 Processing sequence chart

Oscillating Frequency Set command processing sequence

- **<1>** Wait from previous frame reception until next command transmission
- **<2>** Oscillating Frequency Set command frame transmission
- **<3>** Wait from command frame transmission until status check
- **<4>** Status check processing
- **<5>** Result of status check processing

Result:
- Normal completion
- Abnormal termination
- Time-out error

- Normal completion [A]
- Normal completion [C]
- Abnormal termination [B]
- Abnormal termination [C]
6.6.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{com}} \)).

<2> The Oscillating Frequency Set command is transmitted by command frame transmission processing.

<3> Waits from command transmission until status check processing (wait time \( t_{\text{WT9}} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

When the processing ends normally: Normal completion [A]
When the processing ends abnormally: Abnormal termination [B]
When a time-out error occurs: A time-out error [C] is returned.

6.6.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>Normal acknowledgment (ACK) The command was executed normally and the operating frequency was correctly set to the V8S0ES/Hx3.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>05H</td>
<td>Parameter error The oscillation frequency value is out of range.</td>
</tr>
<tr>
<td></td>
<td>07H</td>
<td>Checksum error The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td></td>
<td>15H</td>
<td>Negative acknowledgment (NACK) • A command other than the Status command was received during processing. • Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
</tbody>
</table>
6.6.4 Flowchart

Oscillating Frequency Set command processing

Wait from previous frame reception until next command transmission \( t_{\text{com}} \)

Command frame transmission processing (Oscillating Frequency Set)

Wait from command frame transmission until status check \( t_{\text{WT9}} \)

Status check processing

Time-out error?

Yes

Time-out error [C]

No

Normal completion?

Yes

Normal completion [A]

No

Abnormal termination [B]
6.6.5 Sample program

The following shows a sample program for Oscillating Frequency Set command processing.

```c
u16 fl_csi_setclk(u8 clk[]) {
    u16 rc;

    fl_cmd_prm[0] = clk[0]; // "D01"
    fl_cmd_prm[1] = clk[1]; // "D02"
    fl_cmd_prm[2] = clk[2]; // "D03"
    fl_cmd_prm[3] = clk[3]; // "D04"

    fl_wait(tCOM); // wait before sending command frame

    put_cmd_csi(FL_COM_SET_OSC_FREQ, 5, fl_cmd_prm);
    // send "Oscillation Frequency Set" command

    fl_wait(tWT9);

    rc = fl_csi_getstatus(tWT9_MAX); // get status frame
    switch(rc) {
    // case FLC_NO_ERR: return rc; break; // case [A]
    // case FLC_DFTO_ERR: return rc; break; // case [C]
    // default: return rc; break; // case [B]
    // }
    return rc;
}
```
6.7 Chip Erase Command

6.7.1 Processing sequence chart

Chip Erase command processing sequence

<1> Wait from previous frame reception until next command transmission

<2> Chip Erase command frame transmission

<3> Wait from command frame transmission until status check

<4> Status check processing

<5> Result of status check processing

Result
[Normal completion/ Abnormal termination/ Time-out error]

Time-out error

Normal completion

Time-out error [C]

Abnormal termination

Abnormal termination [B]

Normal completion [A]
6.7.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{COM}} \)).

<2> The Chip Erase command is transmitted by command frame transmission processing.

<3> Waits from command transmission until status check processing (wait time \( t_{\text{WT1}} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

   When the processing ends normally: Normal completion [A]
   When the processing ends abnormally: Abnormal termination [B]
   When a time-out error occurs: A time-out error [C] is returned.

6.7.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
</tbody>
</table>
| | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
| | | | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| WRITE error | 1CH | An erase error has occurred. |
| MRG10 error | 1AH | |
| MRG11 error | 1BH | |
| Time-out error [C] | – | The status frame was not received within the specified time. |
6.7.4 Flowchart

- Chip Erase command processing
- Wait from previous frame reception until next command transmission
- Command frame transmission processing (Chip Erase)
- Wait from command frame transmission until status check
- Status check processing
- Time-out error?
  - Yes: Time-out error [C]
  - No: Normal completion?
    - Yes: Normal completion [A]
    - No: Abnormal termination [B]
6.7.5 Sample program

The following shows a sample program for Chip Erase command processing.

```c
/*****************************
/*
/* Erase all(chip) command (CSI)
/*
/*
*****************************
/* [r] u16 ... error code */
/*****************************

u16 fl_csi_erase_all(void)
{
    u16 rc;

    fl_wait(tCOM);    // wait before sending command frame

    put_cmd_csi(FL_COM_ERASE_CHIP, 1, fl_cmd_prm); // send "Chip Erase" command

    fl_wait(tWT1);

    rc = fl_csi_getstatus(tWT1_MAX);  // get status frame
    // switch(rc) {
    //     // case FLC_NO_ERR: return rc; break; // case [A]
    //     // case FLC_DFTO_ERR: return rc; break; // case [C]
    //     // default: return rc; break; // case [B]
    // }
    return rc;
}
```
6.8 Block Erase Command

6.8.1 Processing sequence chart

Block Erase command processing sequence

- <1> Wait from previous frame reception until next command transmission
- <2> Block Erase command frame transmission
- <3> Wait from command frame transmission until status check
- <4> Status check processing
- <5> Result of status check processing

Result:
- Normal completion
- Abnormal termination
- Time-out error

Erasure of specified blocks completed?
- [Yes/No]

Time-out error

Abnormal termination

Normal completion

Go to <1>
6.8.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{COM}} \)).

<2> The Block Erase command is transmitted by command frame transmission processing.

<3> Waits until status frame acquisition (wait time \( t_{\text{WT2}} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

- When the processing ends normally: When the block erase for all of the specified blocks is not yet completed, processing changes the block number and re-executes the sequence from <1>. When the block erase for all of the specified blocks is completed, the processing ends normally [A].
- When the processing ends abnormally: Abnormal termination [B]
- When a time-out error occurs: A time-out error [C] is returned.

6.8.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
</tbody>
</table>
|                                 | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
|                                 |               |   | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX).  |
|                                 | MRG10 error   | 1AH | An erase error has occurred. |
|                                 | Time-out error [C] | – | The status frame was not received within the specified time. |
6.8.4 Flowchart

Block Erase command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Block Erase)

Wait from command frame transmission until status check

Status check processing

Time-out error?

Yes

Time-out error [C]

No

Normal completion? 

Yes

Erasure of specified blocks completed?

Yes

Normal completion [A]

No

Abnormal termination [B]

No
6.8.5 Sample program
The following shows a sample program for Block Erase command processing for one block.

```c
/* ********************** Erase block command (CSI) **********************/
/* [i] u16 sblk ... start block number * /
/* [i] u16 eblk ... end block number * /
/* [r] u16 ... error code * /
/* ********************** Erase block command (CSI) **********************/

u16 fl_csi_erase_blk(u16 sblk, u16 eblk)
{
    u16 rc;
    u32 wt2, wt2_max;
    u32 top, bottom;

    top = get_top_addr(sblk);    // get start address of start block
    bottom = get_bottom_addr(eblk); // get end address of end block

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    wt2 = make_wt2(sblk, eblk);    // get tWT2(Min)
    wt2_max = make_wt2_max(sblk, eblk); // get tWT2(Max)

    fl_wait(tCOM);                // wait before sending command frame

    put_cmd_csi(FL_COM_ERASE_BLOCK, 7, fl_cmd_prm); // send "Block Erase" command

    fl_wait(wt2);

    rc = fl_csi_getstatus(wt2_max); // get status frame

    switch(rc) {
        case FLC_NO_ERR: return rc; break; // case [A]
        case FLC_DFTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

    return rc;
}
```
6.9 Programming Command

6.9.1 Processing sequence chart

Programmer V850ES/Hx3

<1> Wait from previous frame reception until next command transmission

<2> Programming command frame transmission

<3> Wait from command frame transmission until status check

<4> Status check processing

<5> Result of status check processing

<6> Wait from previous frame reception until next data frame transmission

<7> Data frame (user data) transmission

<8> Wait during status check

<9> Status check processing

<10> Result of status check processing (ST1/ST2)

Reception status (ST1) (Normal completion/Abnormal termination/Time-out error)

Time-out error [C]

Abnormal termination [B]

Abnormal completion

Time-out error [C]

Other than ACK

Abnormal termination [D]

All data frames transmitted? [Yes/No]

Yes

Go to <6>

No

<11> Wait during status check (internal verify)

<12> Status check processing

<13> Result of status check processing

Result (Normal completion/Abnormal termination/Time-out error)

Time-out error

Abnormal termination

Normal completion [A]

Abnormal termination [E]
6.9.2 Description of processing sequence

1. Waits from the previous frame reception until the next command transmission (wait time \( t_{COM} \)).
2. The Programming command is transmitted by command frame transmission processing.
3. Waits from command transmission until status check processing (wait time \( t_{WT3} \)).
4. The status frame is acquired by status check processing.
5. The following processing is performed according to the result of status check processing.
   - When the processing ends normally: Proceeds to <6>.
   - When the processing ends abnormally: Abnormal termination [B]
   - When a time-out error occurs: A time-out error [C] is returned.

6. Waits until the next data frame transmission (wait time \( t_{FD3} \)).
7. User data to be written to the V850ES/Hx3 flash memory is transmitted by data frame transmission processing.
8. Waits from data frame (user data) transmission until status check processing (wait time \( t_{WT4} \)).
9. The status frame is acquired by status check processing.
10. The following processing is performed according to the result of status check processing (status code (ST1/ST2)) (also refer to the processing sequence chart and flowchart).

   - When ST1 = abnormal termination: Abnormal termination [B]
   - When ST1 = time-out error: A time-out error [C] is returned.
   - When ST1 = normal completion: The following processing is performed according to the ST2 value.
     - When ST2 \( \neq \) ACK: Abnormal termination [D]
     - When ST2 = ACK: Proceeds to <11> when transmission of all of the user data is completed.
       If there still remain user data to be transmitted, the processing re-executes the sequence from <6>.

11. Waits until status check processing (time-out time \( t_{WT5} \)).
12. The status frame is acquired by status check processing.
13. The following processing is performed according to the result of status check processing.

   - When the processing ends normally: Normal completion [A]
     (Indicating that the internal verify check has performed normally after completion of write)
   - When the processing ends abnormally: Abnormal termination [E]
     (Indicating that the internal verify check has not performed normally after completion of write)
   - When a time-out error occurs: A time-out error [C] is returned.
### 6.9.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
</tbody>
</table>
|                                | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
• Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]             | –            | The status frame was not received within the specified time. |
| Abnormal termination [D]       | WRITE error  | 1CH | A write error has occurred. |
| Abnormal termination [E]       | MRG11 error  | 1BH | An internal verify error has occurred. |
6.9.4 Flowchart

```
<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Programming command processing</td>
</tr>
<tr>
<td>2</td>
<td>Wait from previous frame reception</td>
</tr>
<tr>
<td>3</td>
<td>Command frame transmission processing (Programming)</td>
</tr>
<tr>
<td>4</td>
<td>Wait from command frame transmission until status check</td>
</tr>
<tr>
<td>5</td>
<td>Status check processing</td>
</tr>
<tr>
<td>6</td>
<td>Time-out error?</td>
</tr>
<tr>
<td>No</td>
<td>Normal completion?</td>
</tr>
<tr>
<td>Yes</td>
<td>Abnormal termination [B]</td>
</tr>
<tr>
<td>7</td>
<td>Data frame transmission processing (User program)</td>
</tr>
<tr>
<td>8</td>
<td>Wait from data frame transmission until status check</td>
</tr>
<tr>
<td>9</td>
<td>Status check processing</td>
</tr>
<tr>
<td>10</td>
<td>Time-out error?</td>
</tr>
<tr>
<td>No</td>
<td>Normal completion?</td>
</tr>
<tr>
<td>Yes</td>
<td>Abnormal termination [B]</td>
</tr>
<tr>
<td>No</td>
<td>Abnormal termination [D]</td>
</tr>
<tr>
<td>11</td>
<td>ST2 = ACK?</td>
</tr>
<tr>
<td>No</td>
<td>All data frames transmitted?</td>
</tr>
<tr>
<td>Yes</td>
<td>Abnormal termination [C]</td>
</tr>
<tr>
<td>12</td>
<td>Status check processing</td>
</tr>
<tr>
<td>13</td>
<td>Time-out error?</td>
</tr>
<tr>
<td>No</td>
<td>Normal completion?</td>
</tr>
<tr>
<td>Yes</td>
<td>Abnormal termination [E]</td>
</tr>
</tbody>
</table>
```

Abnormal termination [A]: Time-out error
Abnormal termination [B]: Normal completion
Abnormal termination [C]: Time-out error
Abnormal termination [D]: All data frames transmitted
Abnormal termination [E]: Status check (internal verify)
6.9.5 Sample program

The following shows a sample program for Programming command processing.

```c
u16 fl_csi_write(u32 top, u32 bottom)
{
    u16 rc;
    u32 send_head, send_size;
    bool is_end;
    u32 wt5, wt5_max;

    // set params
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL
    wt5 = make_wt5(get_block_num(top, bottom));
    wt5_max = make_wt5_max(get_block_num(top, bottom));

    // send command & check status
    put_cmd_csi(FL_COM_WRITE, 7, fl_cmd_prm); // send "Programming" command
    rc = fl_csi_getstatus(tWT3_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }

    // send user data
    send_head = top;
    while(1){
        if ((bottom - send_head) > 256) { // rest size > 256 ?
            is_end = false;       // yes, not end frame
            send_size = 256;       // transmit size = 256 byte
        } else{
            is_end = true;
            send_size = bottom - send_head + 1;
            // transmit size = (bottom - send_head)+1 byte
        }
    }
}
```
memcpy(fl_txdata_frm, rom_buf+send_head, send_size);  // set data frame payload
send_head += send_size;

fl_wait(tFD3);     // wait before sending data frame
put_dfrm_csi(send_size, fl_txdata_frm, is_end);   // send data frame (user data)
fl_wait(tWT4);     // wait

rc = fl_csi_getstatus(tWT4_MAX);   // get status frame
switch(rc) {
  case FLC_NO_ERR:   break; // continue
  // case FLC_DFTO_ERR: return rc; break; // case [C]
  default:  return rc; break; // case [B]
}
if (fl_st2 != FLST_ACK) {  // ST2 = ACK ?
  rc = decode_status(fl_st2);   // No
  return rc;   // case [D]
}
if (is_end)   // send all user data ?
  break;   // yes
  //continue;
}  
/************************************************/
/* Check internally verify    */
/************************************************/

fl_wait(wt5);   // wait

rc = fl_csi_getstatus(wt5_max);   // get status frame
switch(rc) {
  // case FLC_NO_ERR: return rc; break; // case [A]
  // case FLC_DFTO_ERR: return rc; break; // case [C]
  default:  return rc; break; // case [E]
}
return rc;
}
6.10 Verify Command

6.10.1 Processing sequence chart

Verify command processing sequence
6.10.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \(t_{\text{COM}}\)).
<2> The Verify command is transmitted by command frame transmission processing.
<3> Waits from command transmission until status check processing (wait time \(t_{\text{WT6}}\)).
<4> The status frame is acquired by status check processing.
<5> The following processing is performed according to the result of status check processing.

- When the processing ends normally: Proceeds to <6>.
- When the processing ends abnormally: Abnormal termination [B]
- When a time-out error occurs: A time-out error [C] is returned.

<6> Waits from the previous frame reception until the next data frame transmission (wait time \(t_{\text{FD3}}\)).
<7> User data for verifying is transmitted by data frame transmission processing.
<8> Waits from data frame transmission until status check processing (wait time \(t_{\text{WT7}}\)).
<9> The status frame is acquired by status check processing.
<10> The following processing is performed according to the result of status check processing (status code (ST1/ST2)) (also refer to the processing sequence chart and flowchart).

- When ST1 = abnormal termination: Abnormal termination [B]
- When ST1 = time-out error: A time-out error [C] is returned.
- When ST1 = normal completion: The following processing is performed according to the ST2 value.
  - When ST2 ≠ ACK: Abnormal termination [D]
  - When ST2 = ACK: If transmission of all data frames is completed, the processing ends normally [A].
    - If there still remain data frames to be transmitted, the processing re-executes the sequence from <6>.

6.10.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|                                 | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.
  • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]              | –            | The status frame was not received within the specified time. |
| Abnormal termination [D]        | Verify error | 0FH | The verify has failed, or another error has occurred. |
6.10.4 Flowchart

Verify command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Verify)

Wait from command frame transmission until status check

Status check processing

Time-out error?

Yes

No

Normal completion?

Yes

No

Wait from previous frame reception until next data frame transmission

Data frame transmission processing (User program)

Wait from data frame transmission until status check

Status check processing

Time-out error?

Yes

No

Normal completion?

Yes

No

ST2 = ACK?

Yes

No

All data frames transmitted?

Yes

No

Normal completion [A]

Time-out error [C]

Abnormal termination [B]

Abnormal termination [D]
6.10.5 Sample program
The following shows a sample program for Verify command processing.

```c
/*************************************************************************/
/*               */
/* Verify command (CSI)           */
/*               */
/*************************************************************************/
/* \[i\] u32 top    ... start address */
/* \[i\] u32 bottom  ... end address */
/* \[r\] u16   ... error code */
/*************************************************************************/
u16 fl_csi_verify(u32 top, u32 bottom, u8 *buf)
{
    u16 rc;
    u32 send_head, send_size;
    bool is_end;

    // set params
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    // send command & check status
    fl_wait(tCOM);
    put_cmd_csi(FL_COM_VERIFY, 7, fl_cmd_prm); // send "Verify" command
    fl_wait(tWT6);

    rc = fl_csi_getstatus(tWT6_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR:    break; // continue
        // case FLC_DFTO_ERR: return rc;  break; // case \[C\]
        default:  return rc;  break; // case \[B\]
    }

    // send user data
    send_head = top;
    while(1){
        if ((bottom - send_head) > 256) { // rest size > 256 ?
            is_end = false; // yes, not end frame
            send_size = 256; // transmit size = 256 byte
        } else{
            is_end = true;
            send_size = bottom - send_head + 1;
            // transmit size = (bottom - send_head)+1 byte
        }

        memcpy(fl_txdata_frm, buf+send_head, send_size);
    }
}
```
// set data frame payload
send_head += send_size;

fl_wait(tFD3);   // wait before sending data frame
put_dfrm_csi(send_size, fl_txdata_frm, is_end);  // send data frame
fl_wait(tWT7);   // wait

rc = fl_csi_getstatus(tWT7_MAX);   // get status frame
switch (rc) {
    case FLC_NO_ERR:   break; // continue
    // case FLC_DFTO_ERR: return rc; break; // case [C]
    default:  return rc; break; // case [B]
}
if (fl_st2 != FLST_ACK){  // ST2 = ACK ?
    rc = decode_status(fl_st2); // No
    return rc;   // case [D]
}

if (is_end)   // send all user data ?
    break;   // yes
    //continue;
}
return FLC_NO_ERR;  // case [A]
6.11 Block Blank Check Command

6.11.1 Processing sequence chart

Block Blank Check command processing sequence

- **<1>** Wait from previous frame reception until next command transmission
- **<2>** Block Blank Check command frame transmission
- **<3>** Wait from command frame transmission until status check
- **<4>** Status check processing
- **<5>** Result of status check processing

Result:
- Normal completion
- Abnormal termination
- Time-out error

Abnormal termination [B]

Normal completion

Blank check for all of specified blocks completed? [Yes/No]

No
- Time-out error [C]
- Abnormal termination [B]

Yes
- Normal completion [A]
- Go to <1>
6.11.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{COM}} \)).

<2> The Block Blank Check command is transmitted by command frame transmission processing.

<3> Waits from command transmission until status check processing (wait time \( t_{\text{WT8}} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

- When a time-out error occurs: A time-out error [C] is returned.
- When the processing ends abnormally: Abnormal termination [B]
- When the processing ends normally: If the blank check for all of the specified blocks is not yet completed, processing changes the block number and re-executes the sequence from <1>.
  - If the blank check for all of the specified blocks is completed, the processing ends normally [A].

6.11.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|                                 | Negative acknowledgment (NACK) | 15H | - A command other than the Status command was received during processing.  
|                                 |               |     | - Command frame data is abnormal (such as invalid data length (LEN) or no ETX).  
|                                 | MRG11 error | 18H | The specified block in the flash memory is not blank. |
| Time-out error [C]              | –            | The status frame was not received within the specified time. |
6.11.4 Flowchart

Block Blank Check command processing

Wait from previous frame reception until next command transmission

tcom

Command frame transmission processing (Block Blank Check)

Wait from command frame transmission until status check
tws

Status check processing

Time-out error?

Yes

Normal completion?

Yes

No

Blank check for all of specified blocks completed?

Yes

No

Normal completion [A]

Time-out error [C]

Abnormal termination [B]
6.11.5 Sample program

The following shows a sample program for Block Blank Check command processing for one block.

```c
u16 fl_csi_blk_blank_chk(u16 sblk, u16 eblk) {
    u16 rc;
    u32 wt8, wt8_max;
    u32 top, bottom;

    top = get_top_addr(sblk);  // get start address of start block
    bottom = get_bottom_addr(eblk); // get end address of end block

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    wt8 = make_wt8(sblk, eblk);  // get tWT8(Min)
    wt8_max = make_wt8_max(sblk, eblk); // get tWT8(Max)

    fl_wait(tCOM);                // wait before sending command frame

    put_cmd_csi(FL_COM_BLOCK_BLANK_CHK, 7, fl_cmd_prm);  // send "Block Blank Check" command

    fl_wait(wt8);

    rc = fl_csi_getstatus(wt8_max); // get status frame
    // switch(rc) {
    //     case FLC_NO_ERR: return rc; break; // case [A]
    //     case FLC_DFTO_ERR: return rc; break; // case [C]
    //     default: return rc; break; // case [B]
    // }
    return rc;
}
```
6.12 Silicon Signature Command

6.12.1 Processing sequence chart

Silicon Signature command processing sequence

- **<1>** Wait from previous frame reception until next command transmission
- **<2>** Silicon Signature command frame transmission
- **<3>** Wait from command frame transmission until status check
- **<4>** Status check processing
- **<5>** Result of status check processing

- **<6>** Wait from previous frame reception until next data frame transmission
- **<7>** Data frame (silicon signature) reception processing

Result
- Normal completion
- Abnormal termination
- Time-out error

Abnormal termination
- Time-out error [C]
- Abnormal termination [B]

Normal data frame?
- Yes
  - Normal completion [A]
- No
  - Data frame error [D]

Abnormal termination
- Abnormal termination [B]

Time-out error
- Time-out error [C]

**tCOM**

**tWT11**

**tFD2**

**tRD2**
6.12.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{com} \)).

<2> The Silicon Signature command is transmitted by command frame transmission processing.

<3> Waits from command transmission until status check processing (wait time \( t_{WT1} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

   - When the processing ends normally: Proceeds to <6>.
   - When the processing ends abnormally: Abnormal termination [B]
   - When a time-out error occurs: A time-out error [C] is returned.

<6> Waits from the previous frame reception until the next command transmission (wait time \( t_{FD2} \)).

<7> The received data frame (silicon signature data) is checked.

   - If data frame is normal: Normal completion [A]
   - If data frame is abnormal: Data frame error [D]

6.12.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|                               | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
|                               |                         |     | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]             | –                      | – | The status frame was not received within the specified time. |
| Data frame error [D]           | –                      | – | The checksum of the data frame received as silicon signature data does not match. |
6.12.4 Flowchart

1. Silicon Signature command processing
   - Wait from previous frame reception until next command transmission
     - Command frame transmission processing (Silicon Signature)
     - Wait from command frame transmission until status check
       - Status check processing
         - Time-out error?
           - Yes: Time-out error [C]
           - No: Normal completion?
             - Yes: Abnormal termination [B]
             - No: Wait from previous frame reception until next data frame reception
               - Data frame reception processing
                 - Normal data frame?
                   - Yes: Normal completion [A]
                   - No: Data frame error [D]
**6.12.5 Sample program**

The following shows a sample program for Silicon Signature command processing.

```c
/**************************
/*
/* Get silicon signature command (CSI)
/*
/*
/**************************/
/* [i] u8 *sig ... pointer to signature save area */
/* [r] u16 ... error code */
/**************************/
u16 fl_csi_getsig(u8 *sig)
{
    u16 rc;
    fl_wait(tCOM); // wait before sending command frame
    put_cmd_csi(FL_COM_GET_SIGNATURE, 1, fl_cmd_prm); // send "Silicon Signature" command
    fl_wait(tWT11);

    rc = fl_csi_getstatus(tWT11_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        case FLC_DFTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }
    fl_wait(tFD2_SIG); // wait before getting data frame

    rc = get_dfrm_csi(fl_rxdata_frm); // get data frame (signature data)
    if (rc){ // if no error,
        return rc; // case [D]
    }
    memcpy(sig, fl_rxdata_frm+OFS_STA_PLD, fl_rxdata_frm[OFS_LEN]); // copy Signature data
    return rc; // case [A]
}
```
6.13 Version Get Command

6.13.1 Processing sequence chart

Version Get command processing sequence
6.13.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{com}$).
<2> The Version Get command is transmitted by command frame transmission processing.
<3> Waits from command transmission until status check processing (wait time $t_{WT1}$).
<4> The status frame is acquired by status check processing.
<5> The following processing is performed according to the result of status check processing.

- When the processing ends normally: Proceeds to <6>.
- When the processing ends abnormally: Abnormal termination [B]
- When a time-out error occurs: A time-out error [C] is returned.

<6> Waits from the previous frame reception until the next command transmission (wait time $t_{FD2}$).
<7> The received data frame (version data) is checked.

- If data frame is normal: Normal completion [A]
- If data frame is abnormal: Data frame error [D]

6.13.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|                                | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
|                                |                           |             | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]             | – | The status frame was not received within the specified time. |
| Data frame error [D]           | – | The checksum of the data frame received as version data does not match. |
6.13.4 Flowchart

Version Get command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Version Get)

Wait from command frame transmission until status check

Status check processing

Time-out error?

Yes

Normal completion?

Yes

Abnormal termination [B]

No

Wait from previous frame reception until next data frame reception

Data frame reception processing

Normal data frame?

Yes

Normal completion [A]

No

Data frame error [D]
6.13.5 Sample program

The following shows a sample program for Version Get command processing.

```c
u16 fl_csi_getver(u8 *buf)
{
    u16 rc;

    fl_wait(tCOM);                // wait before sending command frame

    put_cmd_csi(FL_COM_GET_VERSION, 1, fl_cmd_prm);    // send "Version Get" command

    fl_wait(tWT12);

    rc = fl_csi_getstatus(tWT12_MAX);    // get status frame
    switch (rc) {
        case FLC_NO_ERR:    break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default:   return rc; break; // case [B]
    }

    fl_wait(tFD2_VG);    // wait before getting data frame

    rc = get_dfrm_csi(fl_rxdata_frm);  // get version data

    if (rc){       // if no error,
        return rc;    // case [D]
    }

    memcpy(buf, fl_rxdata_frm+OFS_STA_PLD, DFV_LEN);// copy version data
    return rc;     // case [A]
}  
```
6.14 Checksum Command

6.14.1 Processing sequence chart

Checksum command processing sequence
6.14.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{com}$).

<2> The Checksum command is transmitted by command frame transmission processing.

<3> Waits from command transmission until status check processing (wait time $t_{WT16}$).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

   When the processing ends normally: Proceeds to <6>.
   When the processing ends abnormally: Abnormal termination [B]
   When a time-out error occurs: A time-out error [C] is returned.

<6> Waits from the previous frame reception until the next command transmission (wait time $t_{FD1}$).

<7> The received data frame (checksum data) is checked.

   If data frame is normal: Normal completion [A]
   If data frame is abnormal: Data frame error [D]

6.14.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H The command was executed normally and checksum data was acquired normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H The specified start/end address is not the start/end address of the block.</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H The checksum of the transmitted command frame does not match.</td>
</tr>
</tbody>
</table>
|                                 | Negative acknowledgment (NACK) | 15H • A command other than the Status command was received during processing.  
|                                 |                           | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]              | –                        | The status frame was not received within the specified time.               |
| Data frame error [D]            | –                        | The checksum of the data frame received as version data does not match.    |
6.14.4 Flowchart

- Checksum command processing
  - Wait from previous frame reception until next command reception
  - Command frame transmission processing (Checksum)
  - Wait from command frame transmission until status check
  - Status check processing
  - Time-out error?
    - No: Normal completion?
      - Yes: Abnormal termination [B]
      - No: Wait from previous frame reception until next data frame reception
  - Time-out error [C]
- Normal completion [A]
- Data frame error [D]
6.14.5 Sample program
The following shows a sample program for Checksum command processing.

```c
u16  fl_csi_getsum(u16 *sum, u32 top, u32 bottom)
{
  u16  rc;
  u32  fd1;

  /* set params */
  set_range_prm(fl_cmd_prm, top, bottom);  // set SAH/SAM/SAL, EAH/EAM/EAL
  fd1 = get_fd1(get_block_num(top, bottom)); // get tFD1(Min)

  /* send command */
  fl_wait(tCOM);   // wait before sending command frame
  put_cmd_csi(FL_COM_GET_CHECK_SUM, 7, fl_cmd_prm);// send "Checksum" command
  fl_wait(tWT16);

  rc = fl_csi_getstatus(tWT16_MAX); // get status frame
  switch(rc) {
    case FLC_NO_ERR:   break; // continue
    // case FLC_DFTO_ERR: return rc; break; // case [C]
    default:  return rc; break; // case [B]
  }

  /* get data frame (Checksum data) */
  fl_wait(fd1);
  rc = get_dfrm_csi(fl_rxdata_frm); // get data frame(version data)

  if (rc){ // if error,
    return rc; // case [D]
  }

  *sum = (fl_rxdata_frm[OFS_STA_PLD] << 8) + fl_rxdata_frm[OFS_STA_PLD+1];
    // set SUM data
  return rc; // case [A]
}
```
6.15 Security Set Command

6.15.1 Processing sequence chart

Security Set command processing sequence

Programmer

V850ES/Hx3

1. Wait from previous frame reception until next command transmission

2. Security Set command frame transmission

3. Wait from command frame transmission until status check

4. Status check processing

5. Result of status check processing

6. Wait from previous frame reception until next data frame transmission

7. Data frame (security data) transmission

8. Wait from data frame transmission until status check

9. Status check processing

10. Result of status check processing

11. Wait during status check (internal verify)

12. Status check processing

13. Result of status check processing

Result
[Normal completion/ Abnormal termination/ Time-out error]

Time-out error [C]

Abnormal termination [B]

Abnormal termination [D]

Abnormal termination [E]

Normal completion [A]
6.15.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{COM}$).
<2> The Security Set command is transmitted by command frame transmission processing.
<3> Waits from command transmission until status check processing (wait time $t_{WT13}$).
<4> The status frame is acquired by status check processing.
<5> The following processing is performed according to the result of status check processing.

   When the processing ends normally: Proceeds to <6>.
   When the processing ends abnormally: Abnormal termination [B]
   When a time-out error occurs: A time-out error [C] is returned.

<6> Waits from the previous frame reception until the data frame transmission (wait time $t_{FD3}$).
<7> The data frame (security setting data) is transmitted by data frame transmission processing.
<8> Waits from data frame transmission until status check processing (wait time $t_{WT14}$).
<9> The status frame is acquired by status check processing.
<10> The following processing is performed according to the result of status check processing.

   When the processing ends normally: Proceeds to <11>.
   When the processing ends abnormally: Abnormal termination [D]
   When a time-out error occurs: A time-out error [C] is returned.

<11> Waits until status acquisition (completion of internal verify) (wait time $t_{WT15}$).
<12> The status frame is acquired by status check processing.
<13> The following processing is performed according to the result of status check processing.

   When the processing ends normally: Normal completion [A]
   When the processing ends abnormally: Abnormal termination [E]
   When a time-out error occurs: A time-out error [C] is returned.
### 6.15.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
| Abnormal termination [B]                         | Negative acknowledgment (NACK) | 15H                                                      | • A command other than the Status command was received during processing.  
|                                                 |              |                                                      | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]                               |              | –                                                          | The status frame was not received within the specified time. |
| Abnormal termination [D]                         | Negative acknowledgment (NACK) | 15H                                                      | The security data frame is abnormal. |
| Abnormal termination [D]                         | Checksum error | 07H                                                      | The checksum of the transmitted security data frame does not match. |
| Abnormal termination [D]                         | Protect error | 10H                                                      | When security data is in the following statuses  
|                                                 |              |                                                      | • The security is changed from disabled to enabled.  
|                                                 |              |                                                      | • The value of the last block number in the boot block cluster is changed when boot block cluster rewriting is disabled. |
| Abnormal termination [E]                         | Parameter error | 05H                                                      | When security data is in the following statuses  
|                                                 |              |                                                      | • The last block number of the boot block cluster is larger than the last block number of the device.  
|                                                 |              |                                                      | • The value of the reset vector handler address is not 00000000H. |
| Abnormal termination [E]                         | MRG10 error | 1AH                                                      | A write error has occurred. |
| Abnormal termination [E]                         | MRG11 error | 1BH                                                      |                                                     |
| Abnormal termination [E]                         | WRITE error  | 1CH                                                      |                                                     |
6.15.4 Flowchart

Security Set command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Security Set)

Wait from command frame transmission until status check

Status check processing

Time-out error?

Yes

No

Normal completion?

Yes

No

Wait from previous frame reception until next data frame transmission

Data frame transmission processing (Internal verify)

Wait from data frame transmission until status check

Status check processing

Time-out error?

Yes

No

Normal completion?

Yes

No

Wait during status check (internal verify)

Status check processing

Time-out error?

Yes

No

Normal completion?

Yes

No

Normal completion (A)

Abnormal termination (B)
6.15.5 Sample program

The following shows a sample program for Security Set command processing.

```c
u16 fl_csi_setscf(u8 scf, u8 bot, u32 vect)
{
    u16 rc;

    fl_cmd_prm[0] = 0x00;   // "BLK" (must be 0x00)
    fl_cmd_prm[1] = 0x00;   // "PAG" (must be 0x00)
    fl_txdata_frm[0] = scf|= 0b11100000; // "FLG" (bit 7,6,5 must be '1')
    fl_txdata_frm[1] = bot;   // "BOT"
    fl_txdata_frm[2] = (u8)(vect >> 16); // "ADH"
    fl_txdata_frm[3] = (u8)(vect >>  8); // "ADM"
    fl_txdata_frm[4] = (u8) vect;  // "ADL"

    fl_wait(tCOM);    // wait before sending command frame
    put_cmd_csi(FL_COM_SET_SECURITY, 3, fl_cmd_prm);// send "Security Set" command
    fl_wait(tWT13);   // wait
    rc = fl_csi_getstatus(tWT13_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }

    fl_wait(tFD3);   // wait before getting data frame
    put_dfrm_csi(5, fl_txdata_frm, true); // send data frame(Security data)
    fl_wait(tWT14);
    rc = fl_csi_getstatus(tWT14_MAX); // get status frame
    switch(rc) {
```
```c
    case FLC_NO_ERR: break; // continue
    // case FLC_DFTO_ERR: return rc; break; // case [C]
    default: return rc; break; // case [B]
}

/*************************************************************/
/* Check internally verify */
/*************************************************************/
fl_wait(tWT15);

rc = fl_csi_getstatus(tWT15_MAX); // get status frame
    // switch(rc) {
    //     // case FLC_NO_ERR: return rc; break; // case [A]
    //     // case FLC_DFTO_ERR: return rc; break; // case [C]
    //     // default: return rc; break; // case [B]
    // }
    return rc;
```
6.16 Read Command

6.16.1 Processing sequence chart

Read command processing sequence
6.16.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time tCOM).

<2> The Read command is transmitted by command frame transmission processing.

<3> Waits from command transmission until status check processing (wait time tWT17).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

<table>
<thead>
<tr>
<th>When the processing ends normally:</th>
<th>Proceeds to &lt;6&gt;.</th>
</tr>
</thead>
<tbody>
<tr>
<td>When the processing ends abnormally:</td>
<td>Abnormal termination [B]</td>
</tr>
<tr>
<td>When a time-out error occurs:</td>
<td>A time-out error [C] is returned.</td>
</tr>
</tbody>
</table>

<6> Waits from the previous frame reception until the data frame reception (wait time tWT18).

<7> The data frame (user data) is received by data frame reception processing.

The following processing is performed according to the result of reception processing.

<table>
<thead>
<tr>
<th>When the processing ends normally:</th>
<th>Proceeds to &lt;10&gt;.</th>
</tr>
</thead>
<tbody>
<tr>
<td>When the processing ends abnormally:</td>
<td>Proceeds to &lt;8&gt;.</td>
</tr>
</tbody>
</table>

<8> Waits from the previous frame reception until the next status (NACK) frame transmission (wait time tWT19).

<9> The NACK frame is transmitted by data frame transmission processing.

A data frame error [D] is returned.

<10> Waits from the previous frame reception until the next status (ACK) frame transmission (wait time tWT19).

<11> The ACK frame is transmitted by data frame transmission processing.

When reception of all data frames is completed, the normal completion status [A] is returned.

If there still remain data frames to be received, the sequence is re-executed from <5>.

6.16.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as read data does not match.</td>
</tr>
</tbody>
</table>
6.16.4 Flowchart

```
Read command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Read)

Wait from command frame transmission until status check

Status check processing

Time-out error?
  Yes
  Time-out error [C]
  No
  Normal completion?
    Yes
    Abnormal termination [B]
    No

Wait from previous frame reception until next data frame transmission

Data frame (user program) reception processing

Processing of data frame reception completed normally?
  Yes
  No

Wait from previous frame reception until next status frame transmission

Status (NACK) frame transmission

Data frame error [D]

Wait from previous frame reception until next status frame transmission

Status (ACK) frame transmission

All data frames received?
  No
  Abnormal termination [B]
  Yes
  Normal completion [A]
```
6.16.5 Sample program

The following shows a sample program for Read command processing.

```c
u16 fl_csi_read(u32 top, u32 bottom)
{
    u16 rc;
    u32 read_head;
    u16 len;
    u8 hooter;

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    fl_wait(tCOM);  // wait before sending command
    put_cmd_csi(FL_COM_READ, 7, fl_cmd_prm); // send "Read" command
    fl_wait(tWT17);  // wait

    rc = fl_csi_getstatus(tWT17_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        case FLC_RX_DFSUM_ERR: return rc; // case [C]
        default:  return rc; break; // case [B]
    }

    read_head = top;
    while(1)
    {
        fl_wait(tWT18);

        rc = get_dfrm_csi(fl_rxdata_frm);  // get ROM data from FLASH
        switch(rc) {
            case FLC_NO_ERR: break; // continue
            case FLC_RX_DFSUM_ERR: return rc; // case [D]
            default: fl_wait(tWT19);
                put_sfrm_csi(FLST_NACK); // send status(NACK) frame
```
return rc;
break;
}

fl_wait(tWT19);
put_sfrm_csi(FLST_ACK);    // send status(ACK) frame

/*********************************************/
/* save ROM data */
/*********************************************/
if ((len = fl_rxdata_frm[OFS_LEN]) == 0)    // get length
    len = 256;

memcpy(read_buf+read_head, fl_rxdata_frm+2, len);    // save to external RAM
    read_head += len;

/*********************************************/
/* end check */
/*********************************************/
hooter = fl_rxdata_frm[len + 3];
if (hooter == FL_ETB)    // end frame ?
    continue;    // no
    break;    // yes
}

return FLC_NO_ERR;
}
CHAPTER 7 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS

This chapter describes the parameter characteristics between the programmer and the V850ES/Hx3 in the flash memory programming mode. Be sure to refer to the user’s manual of the V850ES/Hx3 for the electrical specifications when designing with a programmer.

(1) Flash memory parameter characteristics

(a) Operating clock
The main clock frequency (fxx) of the V850ES/Hx3 is changed according to the value of the main clock oscillation frequency (fx) specified with the Oscillation Frequency Set command by the programmer.

Flash ROM size ≤ 256 KB
• fx = 4.0 MHz: fxx = fx × 8 (PLL mode)
• 4.0 MHz < fx ≤ 8.0 MHz: fxx = fx × 4 (PLL mode)
• 8.0 MHz < fx ≤ 16.0 MHz: fxx = fx × 2 (PLL mode)

Flash ROM size ≥ 384 KB
• 4.0 MHz ≤ fx ≤ 6.0 MHz: fxx = fx × 8 (PLL mode)
• 6.0 MHz < fx ≤ 12.0 MHz: fxx = fx × 4 (PLL mode)
• 12.0 MHz < fx ≤ 16.0 MHz: fxx = fx × 2 (PLL mode)

Therefore, it is obtained by assigning fx (fx = fxx) before the Oscillation Frequency Set command (until a wait (tWT9) after issuance of the Oscillation Frequency Set command from the programmer) and after that, by assigning a frequency value to fxx in accordance with the fx as shown above.

Remark The main clock frequency (fxx) is automatically set in the V850ES/Hx3 in accordance with fx in the flash memory programming mode.
**(b) Flash memory programming mode setting time**

(\(TA = -40\) to +85°C, \(V_{DD} = EV_{DD} = BV_{DD}, AV_{REF0} = 3.8\) to 5.5 V, \(V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0\) V, \(CL = 50\) pF)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{DD})(\uparrow) to FLMD0(\uparrow)</td>
<td>(t_{DP})</td>
<td></td>
<td>1 ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FLMD0(\uparrow) to (\overline{RESET})(\uparrow)</td>
<td>(t_{PR})</td>
<td></td>
<td>2 ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Count start time from (\overline{RESET})(\uparrow) to FLMD0(\uparrow)</td>
<td>(t_{RP})</td>
<td></td>
<td>800 (\mu)s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Count finish time from (\overline{RESET})(\uparrow) to FLMD0(\uparrow)</td>
<td>(t_{RPE})</td>
<td></td>
<td></td>
<td>10 ms</td>
<td></td>
</tr>
<tr>
<td>FLMD0 counter high-level width/low-level width</td>
<td>(t_{PW})</td>
<td></td>
<td>10 (\mu)s</td>
<td>100 (\mu)s</td>
<td></td>
</tr>
<tr>
<td>Wait for Reset command</td>
<td>(t_{RC})</td>
<td>CSI, CSI + HS</td>
<td>0.3 s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for low level (data 1)</td>
<td>(t_{R1})</td>
<td>UART</td>
<td>0.3 s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for low level (data 2)</td>
<td>(t_{12})</td>
<td>UART</td>
<td>30,000/f (f_{xx})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for Reset command</td>
<td>(t_{RC})</td>
<td>UART</td>
<td>30,000/f (f_{xx})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low level width (data 1)</td>
<td>(t_{L1})</td>
<td>UART</td>
<td></td>
<td>300 (\mu)s</td>
<td></td>
</tr>
<tr>
<td>Low level width (data 2)</td>
<td>(t_{L2})</td>
<td>UART</td>
<td></td>
<td>Note 2</td>
<td></td>
</tr>
<tr>
<td>FLMD0 counter rise time</td>
<td>(t_{R})</td>
<td></td>
<td>1 (\mu)s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FLMD0 counter fall time</td>
<td>(t_{F})</td>
<td></td>
<td>1 (\mu)s</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

1. \((t_{RP} + t_{RPE})/2\) is recommended as the standard value for the FLMD0 pin signal input timing.
2. The low-level width is the same as the 00H data width at 9,600 bps.
(c) Programming characteristics

\( (T_A = -40 \text{ to } +85^\circ C, V_{DD} = EV_{DD} = BV_{DD}, AV_{REF0} = 3.8 \text{ to } 5.5 \text{ V}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 \text{ V}, C_L = 50 \text{ pF}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data to Data</td>
<td>( t_{DR} )</td>
<td>Receive data frame</td>
<td>CSI, CSI + HS</td>
<td>226/f_xxx</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>226/f_xxx</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( t_{ST} )</td>
<td>Send data frame</td>
<td>CSI, CSI + HS</td>
<td>196/f_xxx</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note</td>
<td></td>
</tr>
<tr>
<td>Status command frame reception to status frame transmission</td>
<td>( t_{SF} )</td>
<td>CSI, CSI + HS</td>
<td>3,403/f_xxx</td>
<td></td>
</tr>
<tr>
<td>Status frame reception to data frame transmission (1)</td>
<td>( t_{FD1} )</td>
<td>CSI, CSI + HS</td>
<td>1,329/f_xxx ( + 245,837/f_xxx \times M ) ( + 19 \ \mu s )</td>
<td>1,595/f_xxx ( + 295,005/f_xxx \times M ) ( + 23 \ \mu s )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note</td>
<td></td>
</tr>
<tr>
<td>Status frame transmission to data frame transmission (2)</td>
<td>( t_{FD2} )</td>
<td>CSI, CSI + HS</td>
<td>6,045/f_xxx ( + 56 \ \mu s )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note</td>
<td></td>
</tr>
<tr>
<td>Status frame transmission to data frame reception (3)</td>
<td>( t_{FD3} )</td>
<td>CSI, CSI + HS</td>
<td>3,856/f_xxx ( + 38 \ \mu s )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>3,856/f_xxx ( + 38 \ \mu s )</td>
<td></td>
</tr>
<tr>
<td>Status frame transmission to command frame reception</td>
<td>( t_{COM} )</td>
<td>–</td>
<td>749/f_xxx ( + 5 \ \mu s )</td>
<td></td>
</tr>
</tbody>
</table>

**Note** Successive reception must be enabled for the programmer. Set the programmer time-out time to 3 seconds or more.

**Remark** M: Number of blocks
f_xxx: Main clock frequency

\(<t_{DR}, t_{FD3}, t_{COM}>\)

The V850ES/Hx3 is readied for the next communication after the MIN. time has elapsed after completion of the previous communication.

The programmer must transmit the next data after the MIN. time has elapsed after completion of the previous communication.

\(<t_{ST}, t_{SF}, t_{FD2}>\)

The V850ES/Hx3 is readied for the next communication after the MIN. time has elapsed after completion of the previous communication.

The programmer must receive the next data after the MIN. time has elapsed after completion of the previous communication.

In CSI communication, the programmer must issue the Status command after the MIN. time has elapsed. If ACK is not returned, do not repeat the status check and execute the error processing (time-out processing, etc.).

\(<t_{FD1}>\)

The V850ES/Hx3 completes each command processing between the MIN. and MAX. times. If the V850ES/Hx3 does not complete each command processing after the MAX. time has elapsed, execute the error processing (time-out processing, etc.).

In CSI communication, the programmer must repeat the status check from the MIN. time to MAX. time.

In UART communication, the V850ES/Hx3 transmits the status frame between the MIN. and MAX. times.
(d) Command characteristics  

\( (T_A = -40 \text{ to } +85^\circ C, V_{DD} = EV_{DD} = BV_{DD}, AV_{REF} = 3.8 \text{ to } 5.5 \text{ V}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 \text{ V}, C_L = 50 \text{ pF}) \)  

<table>
<thead>
<tr>
<th>Command</th>
<th>Symbol</th>
<th>Condition</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>( t_{WT0} )</td>
<td>CSI, CSI + HS</td>
<td>399/f ( XX )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td>Chip Erase</td>
<td>( t_{WT1} )</td>
<td>—</td>
<td>45,006/f ( XX ) + 97,937 ( \mu s )</td>
<td>48,467/f ( XX ) + 1,937,391 ( \mu s )</td>
</tr>
<tr>
<td>Block Erase</td>
<td>( t_{WT2} )</td>
<td>—</td>
<td>4,885/f ( XX ) + (798/f ( XX ) + 28,432 ( \mu s ) + 307 ( \mu s \times BM )) + (( \ldots ) Note 2) + 42 ( \mu s )</td>
<td>6,078/f ( XX ) + (284,125 ( \mu s ) + 3,072 ( \mu s \times BM )) + 795/f ( XX ) + (( \ldots ) Note 2) + 61 ( \mu s )</td>
</tr>
<tr>
<td>Program</td>
<td>( t_{WT3} )</td>
<td>CSI, CSI + HS</td>
<td>3,433/f ( XX ) + 38 ( \mu s )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( t_{WT4} )Note 3</td>
<td>—</td>
<td>17,972/f ( XX ) + 1,062 ( \mu s )</td>
<td>580,751/f ( XX ) + 17,195 ( \mu s )</td>
</tr>
<tr>
<td></td>
<td>( t_{WT5} )</td>
<td>CSI, CSI + HS</td>
<td>3,948/f ( XX ) + (341,668/f ( XX ) + 2,071 ( \mu s ) \times M + 25 ( \mu s ))</td>
<td>4,738/f ( XX ) + (410,002/f ( XX ) + 2,486 ( \mu s ) \times M + 30 ( \mu s ))</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( t_{WT6} )</td>
<td>CSI, CSI + HS</td>
<td>584/f ( XX )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( t_{WT7} )Note 3</td>
<td>CSI, CSI + HS</td>
<td>9,846/f ( XX ) + 56 ( \mu s )</td>
<td></td>
</tr>
<tr>
<td>Block Blank Check</td>
<td>( t_{WT8} )</td>
<td>—</td>
<td>4,040/f ( XX ) + (308/f ( XX ) + 327 ( \mu s ) \times M + 23 ( \mu s ))</td>
<td>4,848/f ( XX ) + (370/f ( XX ) + 392 ( \mu s ) \times M + 28 ( \mu s ))</td>
</tr>
<tr>
<td>Oscillating Frequency Set</td>
<td>( t_{WT9} )</td>
<td>CSI, CSI + HS</td>
<td>21,308/f ( XX )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td>Baud Rate Set</td>
<td>( t_{WT10} )</td>
<td>UART</td>
<td>4,378/f ( XX )</td>
<td></td>
</tr>
<tr>
<td>Silicon Signature</td>
<td>( t_{WT11} )</td>
<td>CSI, CSI + HS</td>
<td>688/f ( XX )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td>Version Get</td>
<td>( t_{WT12} )</td>
<td>CSI, CSI + HS</td>
<td>701/f ( XX )</td>
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<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note 1</td>
<td></td>
</tr>
</tbody>
</table>

Notes  
1. Reception must be enabled for the programmer before command frame transmission. Set the programmer time-out time to 3 seconds or more.  
2. When how many times the simultaneous selection processing is repeated is indicated by BN, perform the calculation in the parentheses, as shown in the Example below.  
Example  When executing simultaneous processing with changing block size from 2 \( \rightarrow \) 4 \( \rightarrow \) 8  
(Block Erase command’s MIN. value) (BN = 3)  
\[ 7,327/f_{XX} + (28,413 \mu s + 308 \mu s \times 2 + 600/f_{XX}) + (28,413 \mu s + 308 \mu s \times 4 + 600/f_{XX}) + (28,413 \mu s + 308 \mu s \times 8 + 600/f_{XX}) + 72 \mu s \]
3. 64-word units

Remark  
M: Number of blocks  
BM: Number of blocks to be selected and processed simultaneously (blocks)  
BN: Number of executions of simultaneous selection and processing (number of repetitions of addition in the parentheses in Table above)  
f_{XX}: Main clock frequency
(d) Command characteristics

\( TA = -40 \text{ to } +85^\circ C, V_{DD} = EV_{DD} = BV_{DD}, AV_{REF0} = 3.8 \text{ to } 5.5 \text{ V}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 \text{ V, } CL = 50 \text{ pF} \) (1/2)

<table>
<thead>
<tr>
<th>Command</th>
<th>Symbol</th>
<th>Condition</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Security Setting</td>
<td>tWT13</td>
<td>CSI, CSI + HS</td>
<td>653/fXX</td>
<td></td>
</tr>
<tr>
<td></td>
<td>UART</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT14</td>
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<tr>
<td></td>
<td>UART</td>
<td></td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT15</td>
<td>CSI, CSI + HS</td>
<td>277/fXX</td>
<td>17,524/fXX + 284,613 \mu s</td>
</tr>
<tr>
<td></td>
<td>UART</td>
<td></td>
<td>Note 1</td>
<td>17,524/fXX + 284,613 \mu s</td>
</tr>
<tr>
<td>Checksum</td>
<td>tWT16</td>
<td>CSI, CSI+HS</td>
<td>960/fXX</td>
<td></td>
</tr>
<tr>
<td></td>
<td>UART</td>
<td></td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td>Read</td>
<td>tWT17</td>
<td>CSI, CSI + HS</td>
<td>2,074/fXX + 19 \mu s</td>
<td></td>
</tr>
<tr>
<td></td>
<td>UART</td>
<td></td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT18</td>
<td>CSI, CSI + HS</td>
<td>13,594/fXX + 15 \mu s</td>
<td></td>
</tr>
<tr>
<td></td>
<td>UART</td>
<td></td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT19</td>
<td></td>
<td>202/fXX</td>
<td>Note 2</td>
</tr>
</tbody>
</table>

Notes
1. Reception must be enabled for the programmer before command frame transmission. Set the programmer time-out time to 3 seconds or more.
2. Wait for transmit of the command frame from the programmer
3. 64-word units

Remark  \( f_{XX} \): Main clock frequency

\(<t_{WT0} \text{ to } t_{WT9}, t_{WT11} \text{ to } t_{WT19}>\)

- For parameters with both MIN. and MAX. values specified
  - The V850ES/Hx3 completes each command processing between the MIN. and the MAX. times. If the V850ES/Hx3 does not complete each command processing after the MAX. time has elapsed, execute the error processing (time-out processing, etc.).
  - In CSI communication, the programmer must repeat the status check from the MIN. time to the MAX. time.
  - In UART communication, the V850ES/Hx3 transmits the status frame between the MIN. and the MAX. times.

- For parameters with only MIN. value specified
  - In CSI communication, the programmer must issue the Status command after the MIN. time has elapsed. If ACK is not returned, do not repeat the status check and execute the error processing (time-out processing, etc.).

\(<t_{WT10}>\)

- The V850ES/Hx3 is readied for the next communication after the MIN. time has elapsed after completion of the previous communication.
- The programmer must transmit the next data after the MIN. time has elapsed after completion of the previous communication.
CSI Communication Timing

(a) Data frame

(b) Programming mode setting

(c) Reset command

(d) Chip Erase command/Block Erase command/Block Blank Check command/Oscillating Frequency Set command

(e) Silicon Signature command/Version Get command

Remark  
SCR: SCKB0  
SO: SOB0  
SI: SIB0
(f) **Checksum command**

- Command frame
- Status command
- Status frame
- Data frame

<table>
<thead>
<tr>
<th>SCR (input)</th>
<th>SO (output)</th>
<th>SI (input)</th>
</tr>
</thead>
<tbody>
<tr>
<td>tWT16</td>
<td>tSF</td>
<td>tFD1</td>
</tr>
</tbody>
</table>

(g) **Programming command**

- Command frame
- Status command
- Status frame
- Data frame (1)
- Status command (1)
- Status frame (1)

<table>
<thead>
<tr>
<th>SCR (input)</th>
<th>SO (output)</th>
<th>SI (input)</th>
</tr>
</thead>
<tbody>
<tr>
<td>tWT3</td>
<td>tSF</td>
<td>tFD3</td>
</tr>
<tr>
<td>tWT4</td>
<td>tSF</td>
<td>tFD3</td>
</tr>
</tbody>
</table>

(h) **Verify command**

- Command frame
- Status command
- Status frame
- Data frame (1)
- Status command (1)
- Status frame (1)

<table>
<thead>
<tr>
<th>SCR (input)</th>
<th>SO (output)</th>
<th>SI (input)</th>
</tr>
</thead>
<tbody>
<tr>
<td>tWT6</td>
<td>tSF</td>
<td>tFD3</td>
</tr>
<tr>
<td>tWT7</td>
<td>tSF</td>
<td>tFD3</td>
</tr>
</tbody>
</table>

**Remark**

- SCK: SCKB0
- SO: SOB0
- SI: SIB0
Problem 5-2

(i) Security Setting command

![Security Setting command diagram](image1)

(j) Read command

![Read command diagram](image2)

(k) Wait before command frame transmission

![Wait before command frame transmission diagram](image3)

Remark
- SCK: SCKB0
- SO: SOB0
- SI: SIB0
UART communication timing

(a) Data frame

(TxD (output)  
RxD (input)

(b) Programming mode setting

VDD  
FLMD0 (input)  
RESET (input)  
FLMD1 (input)

(c) Reset command

(RESET (input)  
TxD (output)  
RxD (input)

(d) Chip Erase command/Block Erase command/Block Blank Check command/Oscillating Frequency Set command

(e) Baud Rate Set command

Remark  
TxD: TXDD0  
RxD: RXDD0
(f) Silicon Signature command/Version Get command

Command frame  Status frame  Data frame

TxD (output)  

RxD (input)  

\[ t_{WT11}, t_{WT12}, t_{RD2} \]

(g) Checksum command

Command frame  Status frame  Data frame

TxD (output)  

RxD (input)  

\[ t_{WT16}, t_{RD1} \]

(h) Programming command

Command frame  Status frame  Data frame  Status frame

TxD (output)  

RxD (input)  

\[ t_{WT3}, t_{RD3}, t_{WT4}, t_{RD4}, t_{WT5} \]

(i) Verify command

Command frame  Status frame  Data frame  Status frame

TxD (output)  

RxD (input)  

\[ t_{WT6}, t_{RD3}, t_{WT7} \]

\[ t_{WT7}, t_{RD3}, t_{WT7} \]

Remark

TxD: TXDD0
RxD: RXDD0
(j) Security Set command

TxD (output)  RxD (input)

Command frame  Status frame  Data frame  Status frame  Status frame

\( t_{WT13} \)  \( t_{FD3} \)  \( t_{WT14} \)  \( t_{WT15} \)

(k) Read command

TxD (output)  RxD (input)

Command frame  Status frame  Data frame  Status frame  Status frame

\( t_{WT17} \)  \( t_{WT18} \)  \( t_{WT19} \)

Data frame (n-1)  Status frame (n-1)  Data frame (n)  Status frame (n)

(l) Wait before command frame transmission

TxD (output)  RxD (input)

Status frame  Command frame

\( t_{COM} \)

Remark  TxD: TXDD0  RxD: RXDD0
(2) Simultaneous selection block processing

The block erasure, blank check, and internal verification functions are executed by repeating “simultaneous selection and processing”, which processes multiple blocks simultaneously. The wait time is therefore equal to the total execution time of “simultaneous selection and processing”.

To calculate the total execution time of simultaneous selection and processing, the execution count (BN) and the number of blocks (BM) to be selected and processed simultaneously must first be calculated.

(a) Number of blocks (BM) and execution count (BN) of the simultaneous selection and processing

BN is calculated by obtaining the number of blocks to be processed simultaneously (BM: number of blocks to be selected and processed simultaneously).

The number of blocks to be selected and processed simultaneously (BM) should be 1, 2, 4, 8, 16, 32, 64, or 128, depending on which satisfies all of the following conditions.

[Condition 1]

Number of blocks (ER_BKNUM) processed ≥ Potential number of blocks to be selected and processed simultaneously (SSER_BKNUM)

[Condition 2]

Start block number (ST_BKNO) / Potential number of blocks to be selected and processed simultaneously (SSER_BKNUM) = Remainder is 0

[Condition 3]

The maximum value among the values that satisfy both Conditions 1 and 2

Example of simultaneous selection block processing that satisfies Conditions 1, 2, and 3 is shown below.
Example 1  Processing blocks 1 to 127

<1> The first start block number is 1 and the number of blocks to be processed is 127, so the values that satisfy Condition 1 are as follows.

1, 2, 4, 8, 16, 32, 64

The value that satisfies Condition 2 is as follows.

1

The value that satisfies Condition 3 is therefore 1, so the number of blocks to be selected and processed simultaneously (BM) is 1. Thus only block 1 is processed.

<2> After block 1 is processed, the next start block number is 2 and the number of blocks to be processed is 126, so the values that satisfy Condition 1 are as follows.

1, 2, 4, 8, 16, 32, 64

The values that satisfy Condition 2 are as follows.

1, 2

The value that satisfies Condition 3 is therefore 2, so the number of blocks to be selected and processed simultaneously (BM) is 2. Thus blocks 2 and 3 are processed.

<3> After blocks 2 and 3 are processed, the next start block number is 4 and the number of blocks to be processed is 124, so the values that satisfy Condition 1 are as follows.

1, 2, 4, 8, 16, 32, 64

The values that satisfy Condition 2 are as follows.

1, 2, 4

The value that satisfies Condition 3 is therefore 4, so the number of blocks to be selected and processed simultaneously (BM) is 4. Thus blocks 4 to 7 are processed.

<4> After blocks 4 to 7 are processed, the next start block number is 8 and the number of blocks to be processed is 120, so the values that satisfy Condition 1 are as follows.

1, 2, 4, 8, 16, 32, 64

The values that satisfy Condition 2 are as follows.

1, 2, 4, 8

The value that satisfies Condition 3 is therefore 8, so the number of blocks to be selected and processed simultaneously (BM) is 8. Thus blocks 8 to 15 are processed.

<5> After blocks 8 to 15 are processed, the next start block number is 16 and the number of blocks to be processed is 112, so the values that satisfy Condition 1 are as follows.

1, 2, 4, 8, 16, 32, 64

The values that satisfy Condition 2 are as follows.

1, 2, 4, 8, 16

The value that satisfies Condition 3 is therefore 16, so the number of blocks to be selected and processed simultaneously (BM) is 16. Thus blocks 16 to 31 are processed.

<6> After blocks 16 to 31 are processed, the next start block number is 32 and the number of blocks to be processed is 96, so the values that satisfy Condition 1 are as follows.

1, 2, 4, 8, 16, 32, 64

The values that satisfy Condition 2 are as follows.

1, 2, 4, 8, 16, 32

The value that satisfies Condition 3 is therefore 32, so the number of blocks to be selected and processed simultaneously (BM) is 32. Thus blocks 32 to 63 are processed.
After blocks 32 to 63 are processed, the next start block number is 64 and the number of blocks to be processed is 64, so the values that satisfy Condition 1 are as follows.
1, 2, 4, 8, 16, 32, 64

The values that satisfy Condition 2 are as follows.
1, 2, 4, 8, 16, 32, 64

The value that satisfies Condition 3 is therefore 64, so the number of blocks to be selected and processed simultaneously (BM) is 64. Thus blocks 64 to 127 are processed.

Therefore, simultaneous selection and processing is executed seven times (1, 2 and 3, 4 to 7, 8 to 15, 16 to 31, 32 to 63, and 64 to 127) to erase blocks 1 to 127, so BN = 7 is obtained.
Example 2  Processing blocks 5 to 10

<1> The first start block number is 5 and the number of blocks to be processed is 6, so the values
that satisfy Condition 1 are as follows.
  1, 2, 4
The value that satisfies Condition 2 is as follows.
  1
The value that satisfies Condition 3 is therefore 1, so the number of blocks to be selected and
processed simultaneously (BM) is 1. Thus only block 5 is processed.

<2> After block 5 is processed, the next start block number is 6 and the number of blocks to be
processed is 5, so the values that satisfy Condition 1 are as follows.
  1, 2, 4
The values that satisfy Condition 2 are as follows.
  1, 2
The value that satisfies Condition 3 is therefore 2, so the number of blocks to be selected and
processed simultaneously (BM) is 2. Thus blocks 6 and 7 are processed.

<3> After blocks 6 and 7 are processed, the next start block number is 8 and the number of blocks
to be processed is 3, so the values that satisfy Condition 1 are as follows.
  1, 2
The values that satisfy Condition 2 are as follows.
  1, 2
The value that satisfies Condition 3 is therefore 2, so the number of blocks to be selected and
processed simultaneously (BM) is 2. Thus blocks 8 and 9 are processed.

<4> After blocks 8 and 9 are processed, the next start block number is 10 and the number of blocks
to be processed is 1, so the value that satisfies Condition 1 is as follows.
  1
This also satisfies Conditions 2 and 3, so the number of blocks to be selected and processed
simultaneously (BM) is 1. Thus block 10 is processed.

Therefore, simultaneous selection and processing is executed four times (5, 6 and 7, 8 and 9, and 10)
to erase blocks 5 to 10, so \( BN = 4 \) is obtained.
An example of how to obtain BM and BN satisfying Conditions 1, 2, and 3 is illustrated in the following flowchart.

**Remark**
- ST_BKNO: Start block number
- END_BKNO: End block number
- ER_BKNUM: Number of blocks to be erased
- SSER_BKNUM: Potential number of blocks to be selected and processed simultaneously
- BM: Number of blocks to be selected and processed simultaneously
- BN: Number of executions of simultaneous selection and processing
APPENDIX A  CIRCUIT DIAGRAM (REFERENCE)

Figure A-1 show circuit diagrams of the programmer and the V850ES/Hx3, for reference.
Figure A-1. Reference Circuit Diagram of Programmer and V850ES/Hx3 (Main board)
For further information, please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
http://www.necel.com/

[America]
NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-8000
800-366-9782
http://www.am.necel.com/

[Europe]
NEC Electronics (Europe) GmbH
Arcadiastraße 10
40472 Düsseldorf, Germany
Tel: 0211-65030
http://www.eu.necel.com/

Hanover Office
Podbielskistrasse 166 B
30177 Hannover
Tel: 0 511 33 40 2-0

Munich Office
Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

Succursale Française
9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cedex
France
Tel: 01-3067-5800

Succursal en España
Juan Esplandiu, 15
28007 Madrid, Spain
Tel: 91-504-2787

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands
Steigweg 6
5616 HS Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]
NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: 010-8235-1155
http://www.cn.necel.com/

Shanghai Branch
Room 2509-2510, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai, P.R.China P.C:200120
Tel:021-5888-5400
http://www.cn.necel.com/

Shenzhen Branch
Unit 01, 39/F, Excellence Times Square Building,
No. 4068 Yi Tian Road, Futian District, Shenzhen,
PR.China P.C:518048
Tel:0755-8282-9800
http://www.cn.necel.com/

NEC Electronics Hong Kong Ltd.
Unit 1601-1613, 16/F., Tower 2, Grand Century Place,
193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: 2886-9318
http://www.hk.necel.com/

NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-8175-9600
http://www.tw.necel.com/

NEC Electronics Singapore Pte. Ltd.
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/

NEC Electronics Korea Ltd.
11F., Samik Lavied’or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul, 135-080, Korea
Tel: 02-558-3737
http://www.kr.necel.com/