# V850E/MA3, RX651 Group

## V850E/MA3 to RX651 Migration Guide

### Introduction

This application note describes key points to consider when migrating from the V850E/MA3 to the RX651 Group, as well as points of difference between the two groups. For detailed information on the various functions, refer to the latest User's Manual: Hardware of each product.

The descriptions in this document use the specifications of the μPD70F3134BY as representative of the V850E/MA3. Other V850E/MA3 products have somewhat different specifications for memory capacity, but their functions are equivalent to those of the μPD70F3134BY. Therefore this document applies to them as well. In addition, the specifications of the R5F56519 are used as representative of the RX651 Group.

Note that the RX651 Group supports use of a variety of drivers and middleware (Firmware Integration Technology) and the driver generator tool (included with Smart Configurator), which helps to reduce the software development burden.

## Contents

# 1. Overview

## 1.1 Product Lineup

Table 1.1 lists the product lineup (code sizes and pin counts) of the V850E/MA3 and RX651 Group.

**Table 1.1 Code Sizes and Pin Counts of V850E/MA3 and RX651 Group Products**

| V850E/MA3 | | RX651 | |
|---|---|---|---|
| **ROM/RAM** | **Pin Count** | **Code Flash/RAM** | **Pin Count** |
| 256 KB/8 KB (mask ROM) | 144 or 161 pins | — | — |
| 256 KB/16 KB (mask ROM) | 144 or 161 pins | — | — |
| 256 KB/32 KB (mask ROM) | 144 or 161 pins | — | — |
| 512 KB/16 KB (mask ROM) | 144 or 161 pins | 512 KB/256 KB | 64, 100, 144, or 145 pins |
| 512 KB/32 KB (mask ROM, flash memory) | 144 or 161 pins | | |
| — | — | 768 KB/256 KB | 64, 100, 144, or 145 pins |
| — | — | 1 MB/256 KB | 64, 100, 144, or 145 pins |
| — | — | 1.5 MB/640 KB | 64, 100, 144, 145, 176, or 177 pins |
| — | — | 2 MB/640 KB | 64, 100, 144, 145, 176, or 177 pins |

## 1.2 Substitutable and Non-substitutable Functions

Table 1.2 lists which functions of the V850E/MA3 (µPD70F3134BY) are substitutable with functions on the RX651 Group (R5F56519) and which functions are not substitutable.

**Table 1.2 Substitutable and Non-substitutable Functions**

| Function on V850E/MA3 | Substitutable on RX651 Group? |
|---|---|
| Port functions | Yes |
| External bus control functions (external bus interface function) | Yes<br>However, the bus hold function using pins is not supported. |
| Clock generator | Yes |
| Timer functions (TMP and TMQ) | Can be implemented using the multi-function timer pulse unit (MTU3a).<br>However, some functionality requires utilization of CPU interrupts. |
| 16-bit interval timer D (TMD) | Can be implemented using the compare match timer (CMT). |
| 16-bit 2-phase encoder input up/ down counter general-purpose timer (TMENC1) | Can be implemented using the multi-function timer pulse unit (MTU3a). |
| Motor control function | Can be implemented using the multi-function timer pulse unit (MTU3a). |
| Watchdog timer functions | Can be implemented using the watchdog timer (WDTA) or independent watchdog timer (IWDTa). |
| A/D converter | Can be implemented using the 12-bit A/D converter (S12ADFa). |
| D/A converter | Can be implemented using the 12-bit D/A converter (R12DAa). |
| Asynchronous serial interface A (UARTA) | Can be implemented using the serial communications interface (SCIg, SCIi, or SCIh). |
| Clocked serial interface B (CSIB) | Can be implemented using the serial peripheral interface (RSPIc) or serial communications interface (SCIg, SCIi, or SCIh). |
| $I^2C$ bus | Can be implemented using the serial communications interface (SCIg, SCIi, or SCIh) or $I^2C$-bus interface (RIICa). |

| Function on V850E/MA3 | Substitutable on RX651 Group? |
|---|---|
| DMA functions (DMA controller) | Can be implemented using the DMA controller (DMACAa).<br>However, single-step transfer mode is not supported. |
| Interrupt/exception processing function | Yes<br>However, specifications dependent on external interrupts or peripheral modules are excluded. |
| Standby function | Yes |

# 2. On-Chip Functions

## 2.1 CPU Functions

### 2.1.1 Comparative Specifications

Table 2.1 lists comparative specifications of the CPU functions of the V850E/MA3 and RX651 Group.

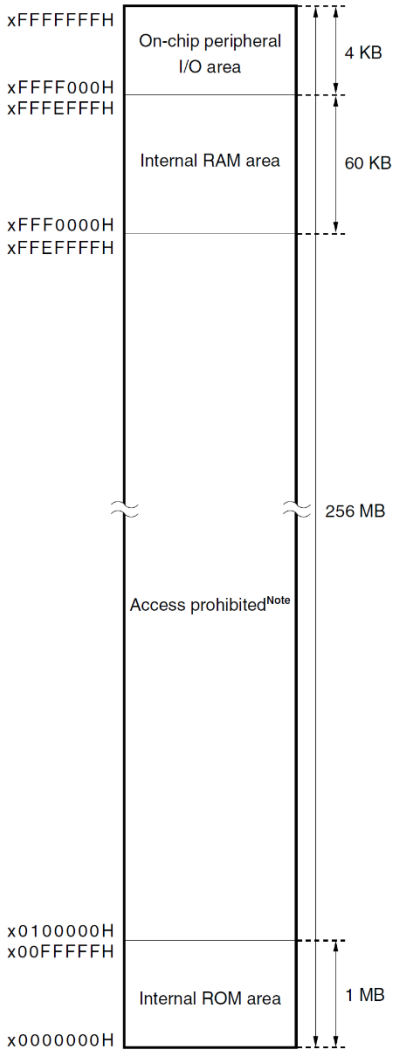
**Table 2.1 CPU Functions of V850E/MA3 and RX651 Group**

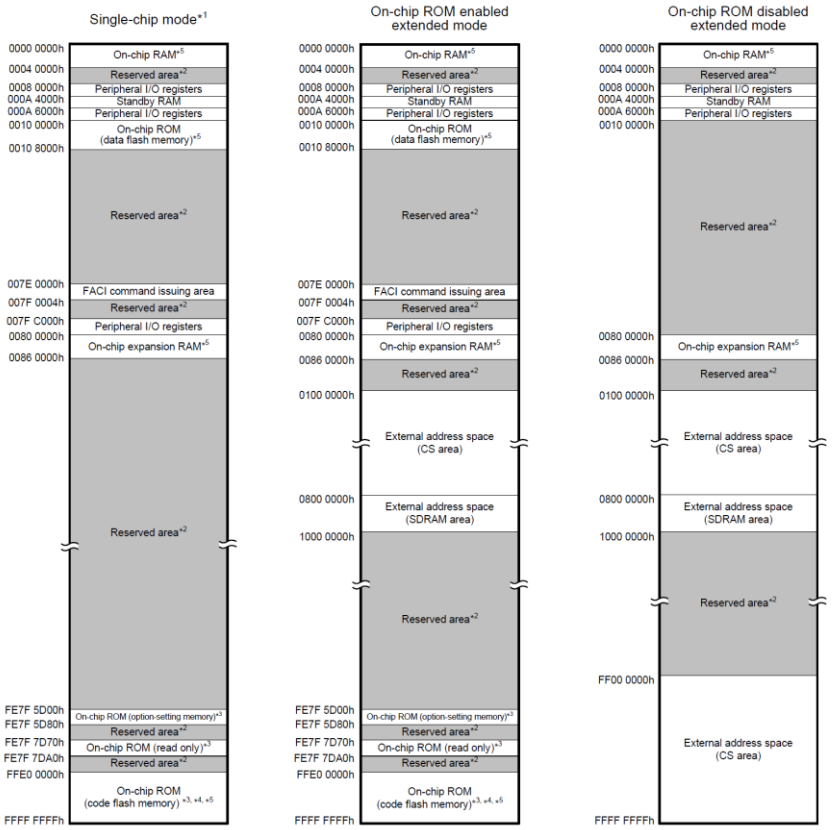
| Item | V850E/MA3 | RX651 |
|---|---|---|
| Max. operating frequency | 80 MHz | 120 MHz |

### 2.1.2 Memory Map

Table 2.2 shows memory maps of the V850E/MA3 and RX651 Group.

**Table 2.2 Memory Maps of V850E/MA3 and RX651 Group**

| Item | V850E/MA3 |
|---|---|
| Memory map |  <br>**Note** By setting the PMCAL, PMCAH, PMCDL, PMCCS, PMCCT, PMCCM, and PMCCD registers to the alternate function, this area can be used as external memory area. |

| Item | RX651 |
|---|---|
| Memory map |  |



Note 1. The address space in boot mode is the same as the address space in single-chip mode.
Note 2. Reserved areas should not be accessed.
Note 3. The access cycle is 1 cycle, 2 cycles, and 3 cycles while the ROMWT[1:0] bits are 00b, 01b, and 10b respectively.
Note 4. The on-chip ROM (code flash memory) can be used in linear mode, where the user area forms a single area, or in dual mode, where the user area is divided into two banks. For details, refer to section 59.2, Structure of Memory in section 59, Flash Memory.
Note 5. The capacities of the code flash memory, data flash memory, and RAM differ depending on the products.

| Code Flash Memory | | | Data Flash Memory | | RAM | |
|---|---|---|---|---|---|---|
| Capacity | Address | | Capacity | Address | Capacity | Address |
| | Linear mode | Dual mode (BANKSEL.BANKSWP[2:0] = 111b) | | | | |
| 2 Mbytes | FFE0 0000h to FFFF FFFFh | bank 1: FFE0 0000h to FFEF FFFFh | 32 Kbytes | 0010 0000h to 0010 7FFFh | 640 Kbytes | 0000 0000h to 0003 FFFFh |
| | | bank 0: FFF0 0000h to FFFF FFFFh | | | | 0080 0000h to 0085 FFFFh |
| 1.5 Mbytes | FFE8 0000h to FFFF FFFFh | bank 1: FFE4 0000h to FFEF FFFFh | 32 Kbytes | 0010 0000h to 0010 7FFFh | 640 Kbytes | 0000 0000h to 0003 FFFFh |
| | | bank 0: FFF4 0000h to FFFF FFFFh | | | | 0080 0000h to 0085 FFFFh |
| 1 Mbyte | FFF0 0000h to FFFF FFFFh | — | — | — | 256 Kbytes | 0000 0000h to 0003 FFFFh |
| 768 Kbytes | FFF4 0000h to FFFF FFFFh | — | — | — | 256 Kbytes | 0000 0000h to 0003 FFFFh |
| 512 Kbytes | FFF8 0000h to FFFF FFFFh | — | — | — | 256 Kbytes | 0000 0000h to 0003 FFFFh |

## 2.2 Port Functions

### 2.2.1 Comparative Specifications

Table 2.3 lists correspondences between the specifications of I/O ports on the RX651 Group and port functions on the V850E/MA3.

**Table 2.3 Substitutability of Port Functions**

| Item | V850E/MA3 | RX651 |
|---|---|---|
| CMOS output | Yes | Yes |

### 2.2.2 Usage Note

#### 2.2.2.1 Unimplemented Ports

Due to different pin counts among products in the RX651 Group, some ports are not implemented on some products. It is therefore necessary to make appropriate settings for unimplemented ports, as described in 22.4, Initialization of the Port Direction Register (PDR), in RX65N Group, RX651 Group User's Manual: Hardware.

This corresponds to setting the port n mode registers (PMn) on the V850E/MA3. For details of port n mode register (PMn) settings, refer to chapter 4, PORT FUNCTIONS, in V850E/MA3 User's Manual: Hardware.

#### 2.2.2.2 Open-Drain Outputs

Pins used as SDA and SCL pins on the V850E/MA3 function as dummy open-drain output pins (P-ch always off). On the RX651 Group all general port pins can be used as open-drain outputs.

## 2.3 External Bus Control Functions (External Bus Interface Function)

### 2.3.1 Comparative Specifications

Table 2.4 lists correspondences between the specifications of the external bus interface function on the V850E/MA3 Group and the external bus function on the RX651 Group. Table 2.5 is a comparative listing of pins used by the external bus interface functions.

**Table 2.4 External Bus Interface Function Correspondences**

| Item | V850E/MA3<br>External Bus Interface Function | RX651<br>External Bus |
|---|---|---|
| Bus width | 8-bit/16-bit | • Separate bus: 8-, 16-, or 32-bit<br>• Address/data multiplexed bus: 8- or 16-bit |
| Bus space | 8 blocks (block size: 2 MB to 64 MB) | Divided into eight CS areas and an SDRAM area (CS areas: 16 MB each, SDRAM area: 128 MB) |
| Wait functions | Data wait | Possible by configuring cycle wait, assert wait, and data output wait settings.*1 |
| | Address setup wait | Possible using CS assert wait setting. |
| | Address hold wait | Possible using address cycle wait setting. |
| | External wait using pin | Possible using WAIT# pin. |
| Bus arbitration in multi-processor configuration | Bus mastership arbitration using bus hold function | Not supported. |
| Bus modes | Ability to select between separate bus mode and multiplexed bus mode | Ability to select between separate bus interface and address/data multiplexed I/O interface |
| Bus cycle type control function | Ability to specify connection to external devices<br>• SRAM, external ROM, or external I/O<br>• Page ROM<br>• SDRAM | • CS area:<br>Ability to connect to an external device (page access also supported)<br>• SDRAM area:<br>Ability to connect to SDRAM |
| Endian control function | Ability to specify for each CS space whether data is processed in big-endian or little-endian mode | Ability to specify for each area whether data is processed in big-endian or little-endian mode |

Note: 1. Read operation: An equivalent setting is possible using the normal read cycle wait setting (CSRWAIT) and RD assert wait (RDON).
Write operation: An equivalent setting is possible using the normal write cycle wait setting (CSWWAIT) and WR assert wait (WRON) or write data output wait (WDON).

**Table 2.5 Comparative Listing of External Bus Interface Function–Related Pins**

| V850E/MA3 | | | RX651 | | |
|---|---|---|---|---|---|
| **Pin Name** | **I/O** | **Function** | **Pin Name** | **I/O** | **Function** |
| AD0 to AD15 | Input/ output | Address/data bus in multiplexed bus mode, data bus in separate bus mode<br>• 8-bit data bus: AD0 to AD7 enabled (AD8 to AD15 enabled as address outputs in multiplexed bus mode)<br>• 16-bit data bus: AD0 to AD15 enabled | D0 to D31 | Input/ output | Data bus (multiplexed with address bus in multiplexed bus mode)<br>• 8-bit data bus: D0 to D7 enabled (A0, D0 to A7, or D7 in multiplexed bus mode)<br>• 16bit data bus: D0 to D15 enabled (A0, D0 to A15, or D15 in multiplexed bus mode)<br>• 32-bit data bus: D0 to D31 enabled (separate bus mode only) |
| A0 to A25 | Output | Address bus<br>• Multiplexed bus mode: A16 to A25 enabled<br>• Separate bus mode: A0 to A25 enabled | A0 to A23 | Output | Address bus<br>• Multiplexed bus mode (8-bit data bus): A8 to A23 enabled<br>• Multiplexed bus mode (16-bit data bus): A16 to A23 enabled<br>• Separate bus mode: A0 to A23 enabled |
| $\overline{CS0}$ to $\overline{CS7}$ | Output | Chip select | CS0# to CS7# | Output | CS area selection |
| | | | SDCS# | Output | SDRAM chip select |
| $\overline{IOWR}$ | Output | I/O write strobe | — | — | — |
| $\overline{IORD}$ | Output | I/O read strobe | — | — | — |
| $\overline{LWR}$ | Output | Write strobe (D0 to D7) | WR0# | Output | Write strobe in byte strobe mode (D0 to D7) |
| $\overline{UWR}$ | Output | Write strobe (D8 to D15) | WR1# | Output | Write strobe in byte strobe mode (D8 to D15) |
| LDQM | Output | SDRAM I/O mask (D0 to D7) | DQM0 | Output | SDRAM I/O data mask enable (D0 to D7) |
| UDQM | Output | SDRAM I/O mask (D8 to D15) | DQM1 | Output | SDRAM I/O data mask enable (D8 to D15) |
| $\overline{LBE}$ | Output | Byte enable (D0 to D7) | BC0# | Output | Byte strobe in single write strobe mode (D0 to D7) |
| $\overline{UBE}$ | Output | Byte enable (D8 to D15) | BC1# | Output | Byte strobe in single write strobe mode (D8 to D15) |
| $\overline{RD}$ | Output | Read strobe | RD# | Output | Read strobe |
| $\overline{WE}$ | Output | SDRAM write enable | WE# | Output | SDRAM write enable |
| $\overline{WR}$ | Output | Write strobe | WR# | Output | Write strobe in single write strobe mode |
| ASTB | Output | Address strobe | ALE | Output | Address latch |
| $\overline{BCYST}$ | Output | Bus cycle start | — | — | — |
| $\overline{WAIT}$ | Input | External wait request | WAIT# | Input | Wait request |
| $\overline{HLDAK}$ | Output | Bus hold acknowledge | — | — | — |
| $\overline{HLDRQ}$ | Input | Bus hold request | — | — | — |
| $\overline{REFRQ}$ | Output | SDRAM refresh request | — | — | — |
| BUSCLK | Output | Bus clock | BCLK | Output | External bus clock |
| SDCKE | Output | SDRAM clock enable | CKE | Output | SDRAM clock enable |

| V850E/MA3 | | | RX651 | | |
|---|---|---|---|---|---|
| **Pin Name** | **I/O** | **Function** | **Pin Name** | **I/O** | **Function** |
| SDCLK | Output | SDRAM clock | SDCLK | Output | SDRAM clock |
| $\overline{\text{SDCAS}}$ | Output | SDRAM column address strobe | CAS# | Output | SDRAM column address strobe |
| $\overline{\text{SDRAS}}$ | Output | SDRAM row address strobe | RAS# | Output | SDRAM row address strobe |

### 2.3.2 Usage Notes

#### 2.3.2.1 Differences Among Products with Different Pin Counts

RX651 Group products with package pin counts less than 144 do not support an SDRAM area. Also, products with 64-pin packages do not support the external bus function.

#### 2.3.2.2 Note on Endianness

On the RX651 Group is not possible to allocate instruction codes to areas with a different endian setting from that of the CPU.

## 2.4 Clock Generator

### 2.4.1 Comparative Specifications

Table 2.6 lists correspondences between the specifications of the clock generator on the V850E/MA3 and the clock generation circuit on the RX651 Group.

**Table 2.6 Clock Generator Function Correspondences**

| Item | V850E/MA3<br>Clock Generator | RX651<br>Clock Generation Circuit |
|---|---|---|
| CPU clock source | Selectable among the following two:<br>• Oscillation clock<br>(PLL mode: 4 MHz to 8 MHz,<br>clock-through mode: 5 MHz to 25 MHz)<br>• PLL clock (×1.25, ×2.5, ×5, or ×10) | Selectable among the following five:<br>• Main clock<br>(Resonator frequency 8 MHz to 24 MHz)<br>(Selectable between resonator and external clock.)<br>• PLL clock<br>(×10 to ×30, ×1/1, ×1/2, or ×1/3)*1<br>• Subclock (32.768 kHz)<br>• HOCO (16 MHz, 18 MHz, and 20 MHz)<br>• LOCO (240 kHz) |
| Operating frequency | Stipulations by function<br>• CPU clock $f_{CPU}$: 80 MHz (max.)<br>• Internal system clock $f_{CLK}$: 80 MHz (max.)<br>• Peripheral clock: 80 MHz (max.)<br>• Watchdog timer clock $f_{XW}$: 40 MHz (max.) | Different clock frequencies are generated according to the function.<br>• ICLK: 120 MHz (max.)<br>• PCLKA: 120 MHz (max.)<br>• PCLKB: 60 MHz (max.)<br>• PCLKC: 60 MHz (max.)<br>• PCLKD: 60 MHz (max.)<br>• FCLK: 4 MHz to 60 MHz<br>(when programming/erasing flash memory)<br>60 MHz (max.)<br>(when reading data flash memory)<br>• BCLK: 120 MHz (max.)<br>• BCLK pin output: 60 MHz (max.)<br>• UCLK: 48 MHz (max.)<br>• CACCLK:<br>Same frequency as each oscillator<br>• CANMCLK: 24 MHz (max.)<br>• RTCSCLK: 32.768 kHz<br>• RTCMCLK: 8 MHz to 16 MHz<br>• IWDTCLK: 120 kHz<br>• JTAGTCK: 10 MHz (max.) |

Note: 1. The PLL clock source is selectable between the main clock and the HOCO.

### 2.4.2 Usage Notes

#### 2.4.2.1 Usage Note Regarding Clock Generation Circuit

On the RX651 Group restrictions apply regarding the frequencies of the system clock (ICLK) and the clocks supplied to the peripheral modules, such as the peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD), the FlashIF clock (FCLK), the external bus clock (BCLK), and the SDRAM clock (SDCLK). For details, refer to 9.10.1, Notes on Clock Generation Circuit, RX65N Group, RX651 Group User's Manual: Hardware.

## 2.5 Timer Functions (TMP and TMQ)

### 2.5.1 Units

Table 2.7 lists the timer function units on the V850E/MA3 and RX651 Group.

**Table 2.7 Timer Functions on V850E/MA3 and RX651 Group**

| Item | V850E/MA3 | RX651 |
|---|---|---|
| Multi-function timer/counter integrated modules | • 16-bit timer/event counter P (TMP)<br>• 16-bit timer/event counter Q (TMQ) | • Multi-function timer pulse unit 3 (MTU3a) |

### 2.5.2 Comparative Specifications

Table 2.8 lists correspondences between the specifications of the timer functions (TMP and TMQ) on the V850E/MA3 and multi-function timer pulse unit 3 (MTU3a) on the RX651 Group.

**Table 2.8 Timer Function Correspondences**

| Item | V850E/MA3<br>TMP, TMQ | RX651<br>MTU3a |
|---|---|---|
| Timer counters | 4 channels<br>(1 channel each for TMP0 to TMP2,<br>1 channel for TMQ0) | 11 channels<br>(1 channel each for MTU0 to MTU4, MTU6 to MTU8, 3 channels for MTU5) |
| Modes | Interval timer<br>Interrupt generation and square wave output at user-defined period<br>• Counters:<br>Up to 4 channels<br>• Waveform output:<br>Up to 10 channels<br>(TMP0 to TMP2: 2 each, TMQ0: 4) | Possible using normal mode (periodic counter operation).<br>• Counters:<br>Up to 8 channels<br>(MTU0 to MTU4 and MTU6 to MTU8)<br>• Waveform output:<br>Up to 28 channels<br>(MTU0, MTU3, MTU4, and MTU6 to MTU8: 4 each, MTU1 and MTU2:<br>2 each) |
| | External event count<br>Counts based on user-defined external event input.<br>• Up to 4 channels<br>• Input pins<br>(TMP0 to TMP2: 1 for each input,<br>TMQ0: 1 input) | Possible on up to 8 channels:<br>MTU0 to MTU4 and MTU6 to MTU8.<br>• External clock input pins:<br>Up to 4 (1 selectable for each channel) |
| | External trigger pulse output<br>Count start and PWM waveform output based on external trigger input.<br>• Up to 7 outputs (TMP0 to TMP2: 1 for each input/output, TMQ0: 1 external event input, 4 outputs) | No equivalent functionality is implemented in hardware.*1 However, equivalent operation can be achieved using PWM mode and CPU interrupts on MTU0 to MTU4, MTU6 and MTU7.<br>• Waveform output:<br>Up to 16 PWM outputs are supported by combining PWM modes 1 and 2. |
| | One-shot pulse output<br>Count start and one-shot pulse output based on external trigger input.<br>• Up to 6 outputs (TMP0 to TMP2: 1 for each input/output, TMQ: 1 external event input, 4 outputs) | |

| Item | V850E/MA3<br>TMP, TMQ | RX651<br>MTU3a |
|---|---|---|
| Modes | PWM output<br>• Up to 10 outputs (TMP0 to TMP2: 2 each, TMQ0: 4) | Waveform output:<br>Up to 16 PWM outputs are supported by combining PWM modes 1 and 2. |
| | Free running timer<br>• Up to 4 channels (TMP0 to TMP2, TMQ0) | Possible using normal mode (free-running counter operation).<br>• Up to 9 channels<br>• 11 count sources (MTU0 to MTU4 and MTU6 to MTU8: 1 each, MTU5: 3) |
| | Pulse width measurement<br>• Measurement on up to 4 channels (input pins: TMP0 to TMP2: 1 each, TMQ0: 1) | Possible using either of the following methods:<br>• Using input capture on each channel (MTU0 to MTU4 and MTU6 to MTU8: 1 each, MTU5: 3)<br>• Using the pulse width measurement function on MTU5 (ability to measure width of up to 3 external pulse inputs) |

Note: 1. Sample programs are available to demonstrate how to reproduce in software external trigger mode and one-shot pulse mode, which are not supported in hardware on the RX651. For details, refer to section 3, Sample Programs.

## 2.6 16-Bit Interval Timer D (TMD)

### 2.6.1 Comparative Specifications

Table 2.9 lists correspondences between the specifications of 16-bit interval timer D (TMD) on the V850E/MA3 and the compare match timer (CMT) on the RX651 Group.

**Table 2.9 16-Bit Interval Timer Function Correspondences**

| Item | V850E/MA3<br>TMD | RX651<br>CMT |
|---|---|---|
| Number of channels | 4 channels | 4 channels |
| Counter bits | 16 | 16 |
| Selectable clock frequency division ratios | 8 ratios<br>A ratio $f_{XX}$/4, $f_{XX}$/8, $f_{XX}$/16, $f_{XX}$/32, $f_{XX}$/64, $f_{XX}$/128, $f_{XX}$/256, or $f_{XX}$/512 can be selected for each channel. | 4 ratios<br>A ratio of PCLK/8, PCLK/32, PCLK/128, PCLK/512 can be selected for each channel. |

### 2.6.2 Usage Note

#### 2.6.2.1 Initializing the Timer

When supply of the count clock to TMD is stopped on the V850E/MA3, TMD unit registers are reset out of sync. On the RX651 Group the CMT retains all register values even if a transition to the module stop state occurs. However, it is not possible to read the values of the registers while in the module stop state.

## 2.7 16-Bit 2-Phase Encoder Input Up/Down Counter General-Purpose Timer (TMENC1)

### 2.7.1 Comparative Specifications

Table 2.10 lists correspondences between the specifications of the 16-bit 2-phase encoder input up/down counter general-purpose timer (TMENC1) on the V850E/MA3 and multi-function timer pulse unit 3 (MTU3a) on the RX651 Group.

**Table 2.10 16-Bit 2-Phase Encoder Input Up/Down Counter General-Purpose Timer Correspondences**

| Item | V850E/MA3<br>TMENC1 | RX651<br>MTU3a |
|---|---|---|
| Timer counters | 1 channel (TMENC1) | 11 channels<br>(1 channel each for MTU0 to MTU4, MTU6 to MTU8, 3 channels for MTU5) |
| Modes | General-purpose timer mode<br>• Interval operation<br>• Free-running operation<br>• Capture function<br>• 1 channel (TMENC10)<br>• Timer input pins: 2<br>• Timer output pin: 1 | Possible in normal mode using periodic counter operation or free-running counter operation (but without external clear source).<br>When used simultaneously with the capture function, it is possible to realize equivalent functionality by combining channels on which the input capture function is enabled in normal mode using synchronous operation.<br>• Up to 8 channels (MTU0 to MTU4 and MTU6 to MTU8)<br>• Input/output pins: Up to 28 (MTU0, MTU3, MTU4, and MTU6 to MTU8: 4 each, MTU1 and MTU2: 2 each) |
| | UDC mode<br>• Up/down count operation based on 2-phase encoder input<br>• Valid edges: Rising edge, falling edge, or both edges | Operation equivalent to mode 3 of UDC mode can be realized using phase counting mode.<br>• Up to 2 channels (MTU1, MTU2)<br>• Valid edges: Rising edge or falling edge |

### 2.7.2 Usage Notes

#### 2.7.2.1 Differences in Count Operation in UDC Mode and Phase Counting Mode

Phase counting mode on the RX651 Group does not have a function for detecting both edges, so it is not possible to realize operation equivalent to mode 4 of UDC mode.

The count conditions in phase counting mode include not only the input pin level on the side where edge detection occurs but also the input pin level on the side where no valid edge is detected. This means that operation equivalent to mode 1 or to mode 2 cannot be realized.

For details of count operation in phase counting mode, refer to 24.3.6.1, 16-Bit Phase Counting Mode, in RX65N Group, RX651 Group User's Manual: Hardware.

## 2.8 Motor Control Functions

### 2.8.1 Comparative Specifications

Table 2.11 lists correspondences between the specifications of multi-function timer pulse unit 3 (MTU3a) on the RX651 Group and the motor control functions on the V850E/MA3.

**Table 2.11 Motor Control Function Correspondences**

| Item | V850E/MA3<br>Motor Control Function | RX651<br>MTU3a |
|---|---|---|
| Number of channels | 6-phase PWM output<br>(3 positive-phase and 3 negative-phase)<br>TMQ and TMQOP are used in combination.<br>• 1 channel (MQ0 + TMQOP0) | Possible using complementary PWM mode.<br>12-phase PWM output<br>(6 positive-phase and 6 negative-phase)<br>• Up to 2 channels (MTU3 + MTU4 and MTU6 + MTU7)<br>• Possible to toggle output in synchronization with PWM period (1 for each channel). |
| Dead time control | Dead time control<br>Generation of negative-phase wave signal | Possible using timer dead time data register. |
| Interrupt culling (skipping) | Interrupt culling function<br>Masking of specified culling count of crest interrupts and valley interrupts (masking possible up to 31 times) | Possible using timer interrupt skipping set register. (masking possible up to 7 times) |
| Forced output stop function | High-impedance output control<br>Ability to switch to high-impedance at detection of a valid edge on the INTP000 pin | Ability to switch to high-impedance in conjunction with port output enable 3.*1 |
| A/D conversion trigger | A/D conversion start trigger output function<br>Trigger source selectable among the following 4:<br>• TMQ counter underflow<br>• TMQ cycle match<br>• TMP compare match during tuning operation (2 sources) | The A/D conversion start request delaying function can be used to generate A/D conversion start requests at a user-defined cycle.<br>• Timer A/D converter start request cycle set registers (2 registers) |

Note: 1. For details of the functions of POE3a, refer to section 25, Port Output Enable 3 (POE3a), in RX65N Group, RX651 Group User's Manual: Hardware.

## 2.9 Watchdog Timer Functions

### 2.9.1 Units

Table 2.12 lists the watchdog timer functions on the V850E/MA3 and the RX651 Group.

**Table 2.12 Watchdog Timer Functions on V850E/MA3 and RX651 Group**

| Item | V850E/MA3 | RX651 |
|---|---|---|
| Watchdog timer functions | Watchdog timer functions | • Watchdog timer (WDTA)<br>• Independent watchdog timer (IWDTa) |

### 2.9.2 Comparative Specifications

Table 2.13 lists correspondences between the specifications of the watchdog timer functions on the V850E/MA3 and the watchdog timer (WDTA) and independent watchdog timer (IWDTa) functions on the RX651 Group.

**Table 2.13 Watchdog Timer Function Correspondences**

| | V850E/MA3 | RX651 | |
|---|---|---|---|
| Item | Watchdog Timer Function | WDTA | IWDTa |
| Counter bit length | 8 bits | 14 bits | 14 bits |
| Count clock sources | • Oscillation clock<br>• PLL clock | Peripheral clock (PCLKB) | IWDT-dedicated clock (IWDTCLK)<br>Generated by on-chip oscillator. |
| Overflow time selection | 8 options<br>$2^{14}$/fxx, $2^{15}$/fxx, $2^{16}$/fxx, $2^{17}$/fxx, $2^{18}$/fxx, $2^{19}$/fxx, $2^{20}$/fxx, $2^{22}$/fxx | 15 options<br>Timeout period:<br>1024, 4096, 8192, or 16384 cycles<br>Clock division ratio:<br>6 options (division by 4, division by 64, division by 128, division by 512, division by 2048, or division by 8192) | 12 options<br>Timeout period:<br>128, 512, 1024, or 2048 cycles<br>Clock division ratio:<br>6 options (no division, division by 16, division by 32, division by 64, division by 128, or division by 256) |
| Operation when overflow occurs | Selectable among interval timer mode, watchdog timer mode 1, and watchdog timer mode 2. | Selectable between non-maskable interrupt request output and reset output. | Selectable between non-maskable interrupt request output and reset output. |
| Interrupt/reset generation source | Overflow interrupt | • Underflow interrupt<br>• Refresh error (window function) | • Underflow interrupt<br>• Refresh error (window function) |

### 2.9.3 Usage Note

#### 2.9.3.1 Count Operation

On the V850E/MA3 watchdog timer counts up, and on the RX651 Group the watchdog timer (WDTA) and independent watchdog timer (IWDTa) count down.

## 2.10 A/D Converter

### 2.10.1 Units

Table 2.14 lists the A/D converter units on the V850E/MA3 and on the RX651 Group.

**Table 2.14 A/D Converters of V850E/MA3 and RX651**

| Item | V850E/MA3 | RX651 |
|---|---|---|
| A/D converter | A/D converter | 12-bit A/D converter (S12ADFa) |

### 2.10.2 Comparative Specifications

Table 2.15 lists correspondences between the specifications of the A/D converter on the V850E/MA3 and the 12-bit A/D converter (S12ADFa) on the RX651 Group.

**Table 2.15 A/D Converter Correspondences**

| Item | V850E/MA3<br>A/D Converter | RX651<br>S12ADFa |
|---|---|---|
| Analog inputs | 8 channels | 2 units, 29 channels<br>• S12AD: 8 channels<br>• S12AD1: 21 channels |
| Resolution | 10 bits | 12 bits |
| A/D conversion method | Successive approximation method | Successive approximation method |
| A/D conversion operating mode | Select mode (single buffer)<br>The voltage on one analog input pin is A/D converted once. | Possible using single scan mode. |
| | Select mode (4 buffers)<br>The voltage on one analog input pin is A/D converted four times. | Possible to perform A/D conversion twice on an arbitrarily selected analog input channel by selecting double trigger mode in single scan mode. |
| | Scan mode<br>A/D conversion is performed in sequence on the ANI0 pin up to an arbitrarily selected analog input pin (ANIn: n = 0 to 7). | Possible to perform A/D conversion on arbitrarily selected channels in single scan mode. |
| A/D conversion trigger mode | Software trigger mode | Software trigger |
| | Timer trigger mode (3 channels) | Possible by accepting a synchronous trigger (such as a trigger from an MTU timer function*1). |
| | External trigger mode (1 channel) | asynchronous trigger<br>• S12AD: ADTRG0# pin<br>• S12AD1: ADTRG1# pin |
| External trigger edges | Falling edge, rising edge, both edges | Falling edge only |
| Conversion time (fastest) | 2.25 µs | • 12-bit conversion mode: 0.48 µs<br>• 10-bit conversion mode: 0.45 µs<br>• 8-bit conversion mode: 0.42 µs |
| Interrupts | A/D conversion end | • Scan end<br>• Match with comparison condition of digital compare function |

Note: 1. Specifically, the timer functions referred to are the following modules:
Multi-function timer pulse unit (MTU)
8-bit timer (TMR)
16-bit timer pulse unit (TPU)
Event link controller (ELC)

### 2.10.3 Usage Note

#### 2.10.3.1 A/D Converter Operating Status

On the V850E/MA3 there are status flags that indicate whether conversion operation is in progress on the A/D converter. On the RX651 Group there are no status flags for the 12-bit A/D converter, but the operating status can be confirmed by checking the A/D conversion start bit in the A/D control register.

## 2.11 D/A Converter

### 2.11.1 Comparative Specifications

Table 2.16 lists correspondences between the specifications of the D/A converter on the V850E/MA3 and the 12-bit D/A converter (R12DAa) on the RX651 Group.

**Table 2.16 D/A Converter Correspondences**

| Item | V850E/MA3<br>D/A Converter | RX651<br>R12DAa |
|---|---|---|
| Analog output | 2 channels | 2 channels |
| Resolution | 8 bits | 12 bits |
| Settling time/ conversion time | Settling time: 3 µs | Conversion time<br>• Unbuffered output: 3 µs<br>• Buffered output: 4 µs |
| Analog output voltage | $AV_{DD1} \times m/256$<br>(m = 0 to 255; value set in DA0CSn register) | AVCC1 × m/4096<br>(m = 0 to 4096; value set in DADRn register) |
| Operating modes | Normal mode<br>(D/A conversion when register is overwritten) | Normal mode<br>(D/A conversion when register is overwritten) |
| | Real-time output mode (D/A conversion triggered by TMD interrupt request signal) | Possible using timer interrupt and event link function*1 in combination. |

Note: 1. For details of the event link function, refer to 21. Event Link Controller (ELC), in RX65N Group, RX651 Group User's Manual: Hardware.

## 2.12 Asynchronous Serial Interface A (UARTA)

### 2.12.1 Comparative Specifications

Table 2.17 lists correspondences between the specifications of asynchronous serial interface A (UARTA) on the V850E/MA3 and the asynchronous mode of the serial communications interface (SCIg, SCIi, and SCIh) on the RX651 Group.

**Table 2.17 Asynchronous Serial Interface Correspondences**

| Item | V850E/MA3<br>UARTA | RX651<br>Asynchronous Mode of SCIg, SCIi, and SCIh |
|---|---|---|
| Number of channels | 4 channels | 13 channels<br>Individual channels can be put into the module stop state. |
| Communication speed (max.) | 5 Mbps (fxx = 80 MHz) | SCIh (SCI10, SCI11):<br>15 Mbps (PCLKA = 120 MHz)<br>SCIg, SCIi (channels other than the above): 7.5 Mbps (PCLKB = 60 MHz) |
| Full-duplex communications | Yes | Yes |
| Character length | Selectable between 7 and 8 bits. | Selectable between 7, 8, and 9 bits. |
| Transmit stop bits | Selectable between 1 and 2 bits. | Selectable between 1 and 2 bits. |
| Parity function | Selectable among odd parity, even parity, 0 parity, or no parity. | Selectable among odd parity, even parity, or no parity. |
| Data transfer | Selectable between MSB- or LSB-first. | Selectable between MSB- or LSB-first. |
| Inverted data | Ability to invert input/output of transmit/ receive data | Ability to invert input/output of transmit/ receive data |
| Clock sources | Selectable between internal and external.*1 | Selectable between internal and external.*2 |
| Noise filter | Noise filter circuit suppresses noise. | Possible to use digital filter to suppress noise.<br>Possible to enable or disable filter. |
| Pins | • Serial baud rate clock input<br>• Transmit data output<br>• Receive data input | • Clock I/O<br>• Transmit data output<br>• Receive data input<br>• Transmit/receive start control I/O |
| Receive error detection | • Parity error<br>• Framing error<br>• Overrun error | • Parity error<br>• Framing error<br>• Overrun error |
| Interrupt sources | • Reception error<br>• Reception end<br>• Transmission enable | • Receive error<br>• Receive data full<br>• Transmit data empty<br>• Transmit end |
| DMA activation sources | • Reception end<br>• Transmission enable | • Receive data full<br>• Transmit data empty |

Notes: 1. It is not possible to use an external clock for UARTA3.
2. A transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12.

### 2.12.2 Usage Note

#### 2.12.2.1 0 Parity

On the V850E/MA3 it is possible to set the parity to 0 parity, but no setting corresponding to 0 parity exists on the RX651 Group.

#### 2.12.2.2 Operating Clock Differences

The operating clocks of the serial communications interface (SCIg, SCIi, and SCIh) on the RX651 Group differ according to which channel used. For details, refer to Table 37.4, Functions of SCI Channels, in RX65N Group, RX651 Group User's Manual: Hardware.

## 2.13 Clocked Serial Interface B (CSIB)

### 2.13.1 Units

Table 2.18 lists the clocked serial interface units on the V850E/MA3 and RX651 Group.

**Table 2.18 Clocked Serial Interface Units on V850E/MA3 and RX651 Group**

| Item | V850E/MA3 | RX651 |
|---|---|---|
| Clocked serial interface | Clocked serial interface B (CSIB) | • Serial peripheral interface (RSPIc)<br>• Simple SPI mode/clock synchronous mode of serial communications interface (SCIg, SCIi, SCIh) |

### 2.13.2 Comparative Specifications

Table 2.19 lists correspondences between the specifications of the clock synchronous modes of the serial peripheral interface (RSPIc) and serial communications interface (SCIg, SCIi, and SCIh) on the RX651 Group and clocked serial interface B (CSIB) on the V850E/MA3.

**Table 2.19 Clocked Serial Interface Correspondences**

| | V850E/MA3 | RX651 | |
|---|---|---|---|
| Item | CSIB | RSPIc | SCIg, SCIi, and SCIh (Simple SPI Mode/ Clock Synchronous Mode) |
| Number of channels | 3 channels | 3 channels | 13 channels |
| Communication clock frequency (max.) | Master/slave shared: 10 MHz | Master operation: 40 MHz (PCLKA = 80 MHz)<br>Slave operation: 30 MHz (PCLKA = 120 MHz) | • Simple SPI mode<br>Master operation: 7.5 MHz (PCLK = 60 MHz or 120 MHz)<br>Slave operation<br>— SCIi (SCI10 and SCI11): 20 MHz (PCLK = 120 MHz)<br>— SCIg and SCIh (channels other than the above): 10 MHz (PCLK = 60 MHz)<br>• Clock synchronous mode<br>Master operation: 7.5 MHz<br>Slave operation: 10 MHz (PCLK = 60 MHz or 120 MHz) |
| Operating modes | Master mode/slave mode | Master mode/slave mode | Master mode/slave mode |
| Serial clock and data phase switchable | Ability to switch serial clock and data phase | Ability to change phase and polarity of RSPCK | Ability to specify clock phase and polarity |
| Data length | Selectable from 8 to 16 bits. | Selectable among 8 to 16, 20, 24, and 32 bits. | 8 bits |
| Data transfer | Switchable between MSB- and LSB-first. | Switchable between MSB- and LSB-first. | Switchable between MSB- and LSB-first. |
| Transfer modes | Single transfer mode (transmission, reception, or transmission/reception mode) | Single transfer operation possible. | Single transfer operation possible. |
| | Continuous transfer mode (transmission, reception, or transmission/reception mode) | Transmission and reception buffers are both double buffer configurations, making continuous transfer possible. | Transmission and reception buffers are both double buffer configurations, making continuous transfer possible. |

| Item | V850E/MA3<br>CSIB | RX651<br>RSPIc | SCIg, SCIi, and SCIh (Simple SPI Mode/ Clock Synchronous Mode) |
|---|---|---|---|
| Pins | • Serial data output<br>• Serial data input<br>• Serial clock I/O | • Master transmit data I/O<br>• Slave transmit data I/O<br>• Clock I/O<br>• Slave-select I/O (SPI operation only) | • Clock I/O<br>• Transmit data output<br>• Receive data input<br>• I/O for transmission/ reception/chip select input pin |
| Interrupt sources | • Reception end<br>• Transmission enable<br>• Reception error | • Receive buffer full<br>• Transmit buffer empty<br>• RSPI error<br>• RSPI idle | • Reception error<br>• Receive data full<br>• Transmit data empty<br>• Transmit end |
| DMA activation sources | • Reception end<br>• Transmission enable | • Receive buffer full<br>• Transmit buffer empty | • Receive data full<br>• Transmit data empty |

### 2.13.3 Usage Note

#### 2.13.3.1 Operating Clock Differences

The operating clocks of the serial communications interface (SCIg, SCIi, and SCIh) on the RX651 Group differ according to which channel used. For details, refer to Table 37.4, Functions of SCI Channels, in RX65N Group, RX651 Group User's Manual: Hardware.

## 2.14 I²C Bus

### 2.14.1 Units

Table 2.20 lists the I²C bus function units on the V850E/MA3 and RX651 Group.

**Table 2.20 I²C Bus Function Units on V850E/MA3 and RX651 Group**

| Item | V850E/MA3 | RX651 |
|---|---|---|
| I²C function | I²C bus | • I²C-bus interface (RIICa)<br>• Simple I²C bus of serial communications interface (SCIg, SCIi, SCIh) |

### 2.14.2 Comparative Specifications

Table 2.21 lists correspondences between the specifications of the I²C bus on the V850E/MA3 and the I²C-bus interface (RIICa) and simple I²C bus mode of the serial communications interface (SCIg, SCIi, and SCIh) on the RX651 Group.

**Table 2.21 I²C Bus Correspondences**

| | V850E/MA3 | RX651 | |
|---|---|---|---|
| **Item** | **I²C Bus** | **RIICa** | **Simple I²C Bus of SCIg, SCIi, and SCIh** |
| Number of channels | 1 channel | 3 channels | 13 channels |
| Transfer rate | Standard mode:<br>Up to 100 kbps<br>High-speed mode:<br>Up to 350 kbps | Standard mode:<br>Up to 100 kbps<br>Fast mode:<br>Up to 400 kbps<br>Fast-mode Plus:<br>Up to 1 Mbps | Standard mode:<br>Up to 100 kbps<br>Fast mode:<br>Up to 350 kbps |
| Communication format | I²C bus format | • I²C bus format<br>• SMBus format | I²C bus format |
| Communication operation | • Master operation (multimaster support)<br>• Slave operation | • Master operation (multimaster support<br>• Slave operation | Master (single-master only) |
| Digital filtering | Usable in high-speed mode only | Ability to enable or disable filtering<br>Ability to adjust the width for noise cancellation | Ability to enable or disable filtering<br>Ability to adjust the width for noise cancellation |
| Reduced power consumption | Operation stop mode<br>Used when serial transfers are not performed. | Can be implemented using module stop function.<br>Can be set for each channel individually. | Can be implemented using module stop function.<br>Can be set for each channel individually. |

| Item | V850E/MA3 | RX651 | |
|---|---|---|---|
| | **I²C Bus** | **RIICa** | **Simple I²C Bus of SCIg, SCIi, and SCIh** |
| Interrupts | 1 source<br>• Fall of 8th or 9th clock pulse of serial clock<br>• Stop condition detection | 4 sources<br>• EEI interrupt<br>Transfer error or transfer event occurrence<br>Arbitration detection<br>NACK detection<br>Timeout detection<br>Start condition (including restart condition) detection<br>Stop condition detection<br>• RXI interrupt<br>Receive data full (including slave address match)<br>• TXI interrupt<br>Transmit data empty (including slave address match)<br>• TEI interrupt<br>Transmit end | 3 sources<br>• RXI interrupt<br>ACK detection/reception<br>• TXI interrupt<br>NACK detection/ transmission<br>• STI interrupt<br>Completion of generation of start condition, restart condition, or stop condition |
| DMA activation sources | Transfer end | • Receive data full<br>• Transmit data empty | • Receive interrupt<br>• Transmit interrupt |

## 2.15 DMA Functions (DMA Controller)

### 2.15.1 Comparative Specifications

Table 2.22 lists correspondences between the specifications of the DMA functions (DMA controller) on the V850E/MA3 and the DMA controller (DMACAa) on the RX651 Group.

**Table 2.22 DMA Function Correspondences**

| Item | V850E/MA3<br>DMA Function | RX651<br>DMACAa |
|---|---|---|
| Number of channels | 4 channels | 8 channels |
| Transfer mode | Single transfer mode<br>A single data transfer occurs for a single transfer request. | Can be implemented using normal transfer mode. |
| | Single-step transfer mode<br>A single data transfer occurs for a single transfer request, after which the bus is released, and operation continues until the specified transfer count is reached. | — |
| | Block transfer mode<br>A single data transfer occurs for a single transfer request, and operation continues until the specified transfer count is reached. | Can be implemented using block transfer mode. |
| Transfer unit | 1 data unit:<br>Selectable between 8 and 16 bits. | 1 data unit:<br>Selectable among 8, 16, and 32 bits.<br>Block size:<br>Can be set to 1 to 1024 data units. |
| Max. transfer count | 65,536 times | Normal transfer mode: 65,535 times<br>Block transfer mode: 64,000 times |
| Transfer requests | Requests by interrupts from on-chip peripheral I/O, requests via DMARQ0 to DMARQ3 pin input, and requests by software trigger | Interrupt requests from peripheral modules, triggers input on external interrupt input pins, and software triggers |
| Transfer targets | Memory ↔ I/O<br>Memory ↔ memory | Transfers can be made to all non-reserved memory areas. |
| Address counting method | Increment, decrement, fixed | Increment, decrement, fixed, offset calculation*1 |
| Interrupts | DMA transfer end interrupt | Transfer end interrupt, transfer escape end interrupt |

Note: 1. The offset calculation setting is supported only on DMAC0.

## 2.16 Interrupt/Exception Processing Function

### 2.16.1 Comparative Specifications

Table 2.23 lists correspondences between the specifications of the interrupt and exception processing function on the V850E/MA3 and the interrupt controller (ICUB) and exception handling on the RX651 Group.

**Table 2.23 Interrupt/Exception Handling Function Correspondences**

| Item | V850E/MA3<br>Interrupt/<br>Exception Processing Function | RX651<br>ICUB/Exception Handling |
|---|---|---|
| Interrupts | Non-maskable interrupts: 2 sources<br>• NMI pin input<br>• Watchdog timer overflow | Non-maskable interrupts: 7 sources<br>• NMI pin interrupt<br>• Oscillation stop detection interrupt<br>• WDT underflow/refresh error<br>• IWDT underflow/refresh error<br>• Voltage monitoring 1 interrupt<br>• Voltage monitoring 2 interrupt<br>• RAM error interrupt |
| | Maskable interrupts<br>• External: 25 sources<br>• On-chip peripheral function interrupts | Interrupts<br>• External pin interrupts: 16 sources<br>• Peripheral function interrupts<br>• Software interrupts: 2 sources |
| | 8 levels of programmable priority control | Ability to specify 16 levels |
| | External interrupt request noise elimination<br>• Noise eliminator using analog filter: NMI, INTPn (n = 000, 001, 004, 005,010-013, 021, 022, 050, 051, 106, 107, 114, 115, 124 to 126, 130 to 134, 137)<br>— Signal input that changes within the noise elimination interval (80 ns) is disregarded. | Noise cancellation on external interrupt request pins<br>• Digital filter: Ability to enable or disable digital filter on NMI and IRQ0 to IRQ15<br>— Only input that matches the specified level three times successively is passed through.<br>— Sampling frequency: PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 |
| | External interrupt request valid edge specification:<br>NMI, INTPn (n = 000, 001, 004, 005, 010 to 013, 021, 022, 050, 051, 106, 107, 114, 115, 124 to 126, 130 to 134, 137)<br>• Rising edge<br>• Falling edge<br>• Both edges | Ability to configure settings for external interrupt request pin interrupt detection<br>• Low level (IRQ0 to IRQ15)<br>• Rising edge (NMI, IRQ0 to IRQ15)<br>• Falling edge (NMI, IRQ0 to IRQ15)<br>• Both edges (IRQ0 to IRQ15) |
| Exceptions | Software exceptions<br>Dedicated vectors: 32 sources | Unconditional trap by INT instruction and BRK instruction<br>Unconditional trap dedicated vectors: 16 sources |
| | Exception trap: 2 sources<br>(illegal opcode exception and debug trap) | Can be implemented using undefined instruction exception and privileged instruction exception. |

### 2.16.2 Usage Note

#### 2.16.2.1 Non-maskable Interrupt Vector Area

The vector area used by non-maskable interrupts on the RX651 Group is in the exception vector table. For details, refer to 2.6, Vector Table, in RX65N Group, RX651 Group User's Manual: Hardware.

#### 2.16.2.2 Software Configurable Interrupts and Group Interrupts

The RX651 Group supports software configurable interrupt and group interrupt functions. The software configurable interrupt function allows individual peripheral module interrupt sources to be assigned to specified interrupt vector numbers. The group interrupt function allows multiple interrupt sources to be assigned to a group and treated as a single interrupt source. For details of these types of interrupts, refer to Table 15.1, ICU Specifications, in RX65N Group, RX651 Group User's Manual: Hardware.

## 2.17 Standby Function

### 2.17.1 Comparative Specifications

Table 2.24 lists correspondences between the specifications of the standby function on the V850E/MA3 and the low power consumption functions on the RX651 Group.

**Table 2.24 Standby Function Correspondences**

| Item | V850E/MA3<br>Standby Function | RX651<br>Low Power Consumption Function |
|---|---|---|
| HALT mode | Mode in which only the operating clock of the CPU is stopped<br><br>< Cancellation sources ><br>• Non-maskable interrupt request signals (NMI pin input and non-maskable interrupt request signals generated by overflow)<br>• Unmasked maskable interrupt request signals<br>• Reset signals (reset signals generated by RESET pin input or watchdog timer overflow) | Can be implemented using sleep mode.<br><br>< Cancellation sources ><br>• Non-maskable interrupts<br>• Unmasked maskable interrupts<br>• Resets (RES# pin resets, power-on resets, voltage monitoring resets, and independent watchdog timer resets) |
| IDLE mode | Mode in which operation of all internal circuits except for the oscillator is stopped However, it is possible to implement operation equivalent to the CSIB operating in slave mode or the UARTA operating when an external clock is selected.<br><br>< Cancellation sources ><br>• Non-maskable interrupt request signals (NMI pin input)<br>• Unmasked external interrupt request signals (INTPn pin input)<br>• Unmasked internal interrupt request signals from peripheral functions capable of operating while in IDLE mode (CSIB-related interrupt request signals when in slave mode and UARTA-related interrupt request signals when an external clock is selected)<br>• Reset signals (RESET pin input) | Can be implemented using sleep mode and module stop function.<br><br>< Cancellation sources ><br>• Non-maskable interrupt<br>• Unmasked maskable interrupts<br>• Resets (RES# pin resets, power-on resets, voltage monitoring resets, and independent watchdog timer resets) |

| Item | V850E/MA3<br>Standby Function | RX651<br>Low Power Consumption Function |
|---|---|---|
| Software STOP mode | Mode in which operation of all internal circuits is stopped<br>However, it is possible to implement operation equivalent to the CSIB operating in slave mode or the UARTA operating when an external clock is selected.<br><br>< Cancellation sources ><br>• Non-maskable interrupt request signals (NMI pin input)<br>• Unmasked external interrupt request signals (INTPn pin input)<br>• Unmasked internal interrupt request signals from peripheral functions capable of operating while in software STOP mode (CSIB-related interrupt request signals when in slave mode and UARTA-related interrupt request signals when an external clock is selected)<br>• Reset signals (RESET pin input) | Can be implemented using software standby mode.<br>However, it is not possible to implement operation equivalent to the CSIB operating in slave mode or the UARTA operating when an external clock is selected.<br><br>< Cancellation sources ><br>• External pin interrupts (NMI, IRQ0 IQR15)<br>• Peripheral function interrupts (RTC alarm, RTC periodic, IWDT, USB suspend/resume, voltage monitoring 1, and voltage monitoring 2)<br>• Resets (RES# pin resets, power-on resets, voltage monitoring resets, and independent watchdog timer resets) |

Note: n = 000, 001, 004, 005, 010-013, 021,022, 050, 051, 106, 107, 114, 115, 124-126, 130-134, and 137

**Table 2.25 Operating Status after Transition to Each Mode**

| Function | V850E/MA3 | | | RX651 | | | |
|---|---|---|---|---|---|---|---|
| | HALT Mode | IDLE Mode | Software STOP Mode | Sleep Mode | All-Module Clock Stop Mode | Software Standby Mode | Deep Software Standby Mode |
| Clock generator | ○ | ○ | × | — | — | — | — |
| Main clock | — | — | — | ○ | ○ | ○ | ○ |
| PLL | ○ | ○ | × | ○ | ○ | × | × |
| Subclock | — | — | — | ○ | ○ | ○ | ○ |
| High-speed on-chip oscillator | — | — | — | ○ | ○ | × | × |
| Low-speed on-chip oscillator | — | — | — | ○ | ○ | × | × |
| IWDT-dedicated on-chip oscillator | — | — | — | ○*1 | ○*1 | ○*1 | × |
| CPU | × (Retained) | × (Retained) | × (Retained) | × (Retained) | × (Retained) | × (Retained) | × (Undefined) |
| DMA | ○ | × | × | ○*2 | × (Retained) | × (Retained) | × (Undefined) |
| Interrupt controller | ○ | × | × | ○ | × | × | × |
| Watchdog timer | ○ | × | × | ○*3 | ○*3 | ○*3 | × (Undefined) |
| Other peripheral modules | *4 | *4 | *4 | ○ | *4 | *4 | *4 |
| Ports | Retained | Retained | Retained | ○ | Retained*5 | Retained*5 | Retained *5*6 |
| RAM | Retained | Retained | Retained | ○ | × (Retained) | × (Retained) | ×*7 (Retained/ undefined) |

○: operating possible, ×: operation stopped, —: no equivalent function

“Retained” means that internal register values are retained and internal operations are suspended.

“Undefined” means that internal register values are undefined and power is not supplied to the internal circuits.

Notes: 1. Whether IWDT count operation continues or stops when transitioning to low power consumption mode is selectable. For details, refer to Table 11.2, Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, in RX65N Group, RX651 Group User’s Manual: Hardware.

2. Writing to system control–related registers is prohibited when in sleep mode. For details, refer to Table 5.1, List of I/O Registers (Address Order), in RX65N Group, RX651 Group User’s Manual: Hardware.
3. WDTA operation is stopped.
4. The conditions and modules for which operation is possible differ depending on the mode. For details, refer to chapter 21, Standby Function, in V850E/MA3 User’s Manual: Hardware, and to section 11, Low Power Consumption, in RX65N Group, RX651 Group User’s Manual: Hardware.
5. If pin P53 is being used for the BCLK signal, operation continues with the output of BCLK unmodified. When the 8-bit timer and RTC are operating, operation of related pins continues.

6. Retention of levels or placement in the high-impedance state can be selected for the address bus and bus control signals by setting the output port enable bit in the standby control register.
7. Retention or undefined can be selected by setting the deep cut bits in the deep standby control register.

# 3. Sample Code

The distribution package containing this application note includes sample programs that reproduce in software functions of the V850E/MA3 that are not implemented in hardware on the RX651 Group.

The latest versions of the sample programs are available on the Renesas Electronics website.

## 3.1 Operation Confirmation Conditions

Table 3.1 shows the environment on which the operation of the sample programs has been confirmed.

**Table 3.1 Operation Confirmation Conditions**

| Item | Description |
|---|---|
| MCU used | R5F565NEDDFC |
| Operating frequencies | • Main clock: 24 MHz<br>• PLL: 240 MHz (main clock divided by 1 and multiplied by 10)<br>• System clock (ICLK): 120 MHz (PLL divided by 2)<br>• Peripheral module clock A (PCLKA): 120 MHz (PLL divided by 2)<br>• Peripheral module clock B (PCLKB): 60 MHz (PLL divided by 4)<br>• Peripheral module clock C (PCLKC): 60 MHz (PLL divided by 4)<br>• Peripheral module clock D (PCLKD): 60 MHz (PLL divided by 4)<br>• FlashIF clock (FCLK): 60 MHz (PLL divided by 4)<br>• External bus clock (BCLK): 120 MHz (PLL divided by 2) |
| Operating voltage | 3.3 V |
| Integrated development environment | Renesas Electronics<br>e$^2$ studio Version 2021-10 |
| Compiler | Renesas Electronics<br>C/C++ Compiler Package for RX Family V.3.03.00 |
| | Default settings of integrated development environment |
| iodefine.h version | V2.30 |
| Endian order | Little endian |
| Operating mode | Single-chip mode |
| Processor mode | Supervisor mode |
| Sample program version | Version 1.00 |
| Board used | Renesas Starter Kit for RX65N-2MB<br>(product No.: RTK500565N2SxxxxxBE) |

## 3.2 Project Structure

Table 3.2 lists the sample projects accompanying this application note, and Table 3.3 lists files in which changes were made to source code generated by the code generation function.

**Table 3.2 Projects**

| Function | Project Name | Description |
|---|---|---|
| External trigger PWM output function | external_input_RX651 | This project reproduces the functionality on the V850E/MA3 for using external trigger input to initiate count start and PWM output on the RX651 Group using the IRQ external input interrupt*1 and the multi-function timer pulse unit in PWM mode 1. |
| One-shot pulse output function | one_shot_pulse_RX651 | This project reproduces the functionality on the V850E/MA3 for using external trigger input to initiate count start and one-shot pulse output on the RX651 Group using the IRQ external input interrupt*1 and the multi-function timer pulse unit in PWM mode 1. |

Note: 1. Connected to SW1 (tactile switch) on the RSK board.

**Table 3.3 Changes to Files Generated by Code Generation Function**

| Project | Folder | File Name | Description |
|---|---|---|---|
| external_input_RX651 | Config_ICU | Config_ICU_user.c | User-implemented interrupt handling |
| one_shot_pulse_RX651 | Config_ICU | Config_ICU_user.c | User-implemented interrupt handling |
| | Config_MTU | Config_MTU0_user.c | User-implemented interrupt handling |

Note: For details of the added processing, refer to 3.5, Flowcharts. Source code generated by the code generation function of Smart Configurator that has not been modified is omitted.

## 3.3 Functions

Table 3.4 lists the functions used by the sample programs.

**Table 3.4 Functions Used by Sample Programs**

| Function Name | Description |
|---|---|
| main | Main processing routine |
| r_Config_ICU_irq11_interrupt | External interrupt handler |
| r_Config_MTU0_tgib0_interrupt | MTU0 compare match interrupt processing<br>(only used by one-shot pulse output function sample program) |

Note: Source code generated by the code generation function of Smart Configurator that has not been modified is omitted.

## 3.4 Function Specifications

The sample code function specifications are listed below.

| main | |
|---|---|
| Outline | Main processing routine |
| Header | None |
| Declaration | void main (void) |
| Description | Makes initial settings. |
| Arguments | None |
| Return Value | None |

| r_Config_ICU_irq11_interrupt | |
|---|---|
| Outline | IRQ11 interrupt handler |
| Header | Config_ICU.h |
| Declaration | static void r_Config_ICU_irq11_interrupt (void) |
| Description | Handles the IRQ11 interrupt.<br>The IRQ interrupt handler starts count operation on MTU0. |
| Arguments | None |
| Return Value | None |
| Remarks | This function is generated by the code generation function of Smart Configurator. |

| r_Config_MTU0_tgib0_interrupt | |
|---|---|
| Outline | MTU0 compare match B interrupt processing |
| Header | Config_MTU0.h |
| Declaration | static void r_Config_MTU0_tgib0_interrupt (void) |
| Description | Handles the MTU0 compare match interrupt.<br>The MTU0 compare match interrupt handler stops count operation on MTU0. |
| Arguments | None |
| Return Value | None |
| Remarks | This function is generated by the code generation function of Smart Configurator.<br>This function is only used by one_shot_pulse_rx651. |

## 3.5 Flowcharts

The sample programs make use of the code generation function. This section contains flowcharts of functions containing changes to the program code generated by e$^2$ studio and that are used to reproduce the hardware functionality of the V850E/MA3. For details of other peripheral functions, etc., refer to the setting screens in Smart Configurator and the generated code.

### 3.5.1 Main Processing

Figure 3.1 is a flowchart of the main processing routine.

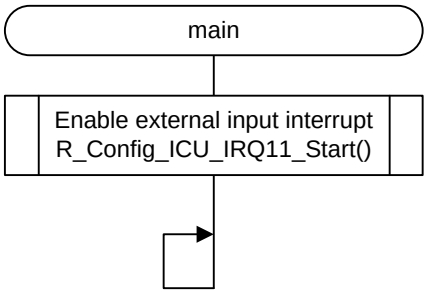
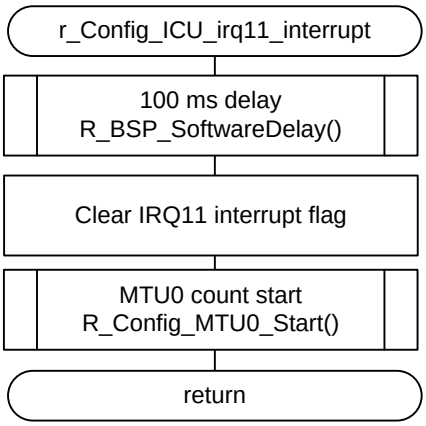



**Figure 3.1 Main Processing Routine**

### 3.5.2 External Input Interrupt Handler

Figure 3.2 is a flowchart of the external interrupt handler.




Note: The 100 ms delay is to accommodate chattering by SW1 (tactile switch).

**Figure 3.2 External Input Interrupt Handler**

### 3.5.3 MTU0 Interrupt Handler of One-Shot Pulse Output Function

Figure 3.3 is a flowchart of the MTU0 interrupt handler used by the one-shot pulse output function.

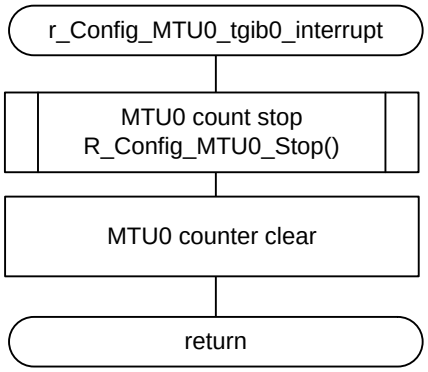



**Figure 3.3 MTU0 Interrupt Handler**

# 4. Importing a Project

The sample programs are distributed in e² studio project format. This section shows how to import a project into e² studio. After importing a project, check the build and debug settings.

## 4.1 Procedure in e² studio

To use sample programs in e² studio, follow the steps below to import them into e² studio. (Note that depending on the version of e² studio you are using, the interface may appear somewhat different from the screenshots below.)

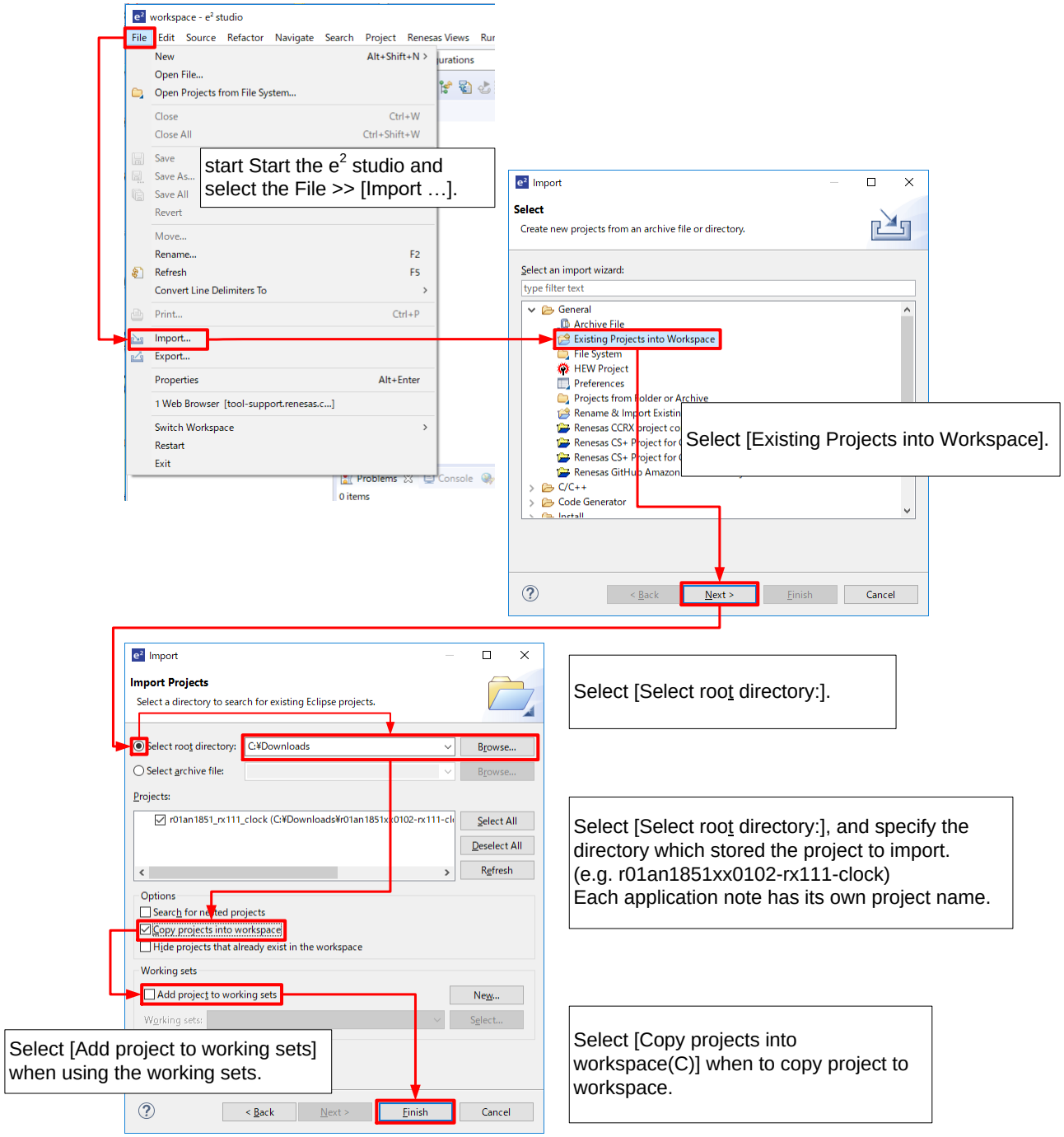



**Figure 4.1 Importing a Project into e² studio**

Notes: In projects managed by e² studio, do not use space codes, multibyte characters, and symbols such as "$", "#", "%" in folder names or paths to them.

## 4.2 Procedure in CS+

To use sample programs in CS+, follow the steps below to import them into CS+. (Note that depending on the version of CS+ you are using, the interface may appear somewhat different from the screenshots below.)

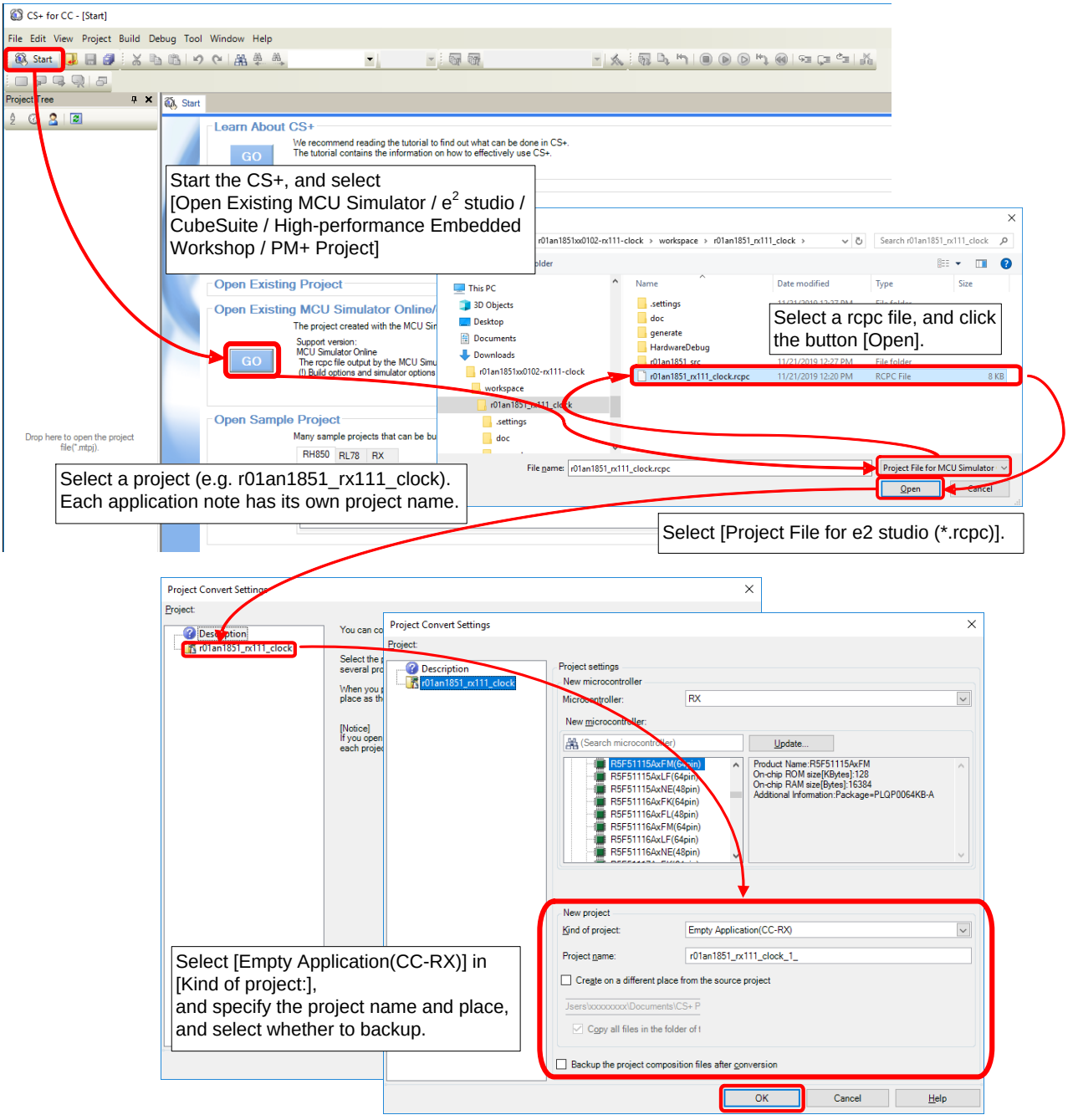



**Figure 4.2 Importing a Project into CS+**

Notes: In projects managed by CS +, do not use space codes, multibyte characters, and symbols such as "$", "#", "%" in folder names or paths to them.

## 5. Reference Documents

User's Manual: Hardware

RX65N Group, RX651 Group User's Manual: Hardware (R01UH0590)
V850E/MA3 User's Manual: Hardware (U16397EJ4V0UD)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Updates/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

User's Manual: Development Tools

CC-RX Compiler User's Manual (R20UT3248)
(The latest version can be downloaded from the Renesas Electronics website.)

## Revision History

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Dec. 29.21 | — | First edition issued |
| | | | |

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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