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Preliminary Application Note

V850E/IF3, V850E/IG3

32-bit Single-Chip Microcontrollers

Sample Programs for Timer AB

V850E/IF3: μ PD70F3451 μ PD70F3452 V850E/IG3: μ PD70F3453 μ PD70F3454

Document No. U18731EJ1V0AN00 (1st edition) Date Published September 2007 N

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[MEMO]

NOTES FOR CMOS DEVICES —

1 VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{\rm IL}$ (MAX) and $V_{\rm IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{\rm IL}$ (MAX) and $V_{\rm IH}$ (MIN).

(2) HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

6 INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M5 02.11-1

INTRODUCTION

- Cautions 1. This Application Note explains a case where the V850E/IG3 is used as a representative microcontroller. Use this Application Note for your reference when using the V850E/IF3.
 - 2. Download the program used in this manual from the page of Programming Examples (http://www.necel.com/micro/en/designsupports/sampleprogram/index.html) in the NEC Electronics Website (http://www.necel.com/).
 - 3. The sample programs are provided for reference purposes only and operations are therefore not subject to guarantee by NEC Electronics Corporation. When using sample programs, customers are advised to sufficiently evaluate this product based on their systems, before use.
 - 4. When using sample programs, reference the following startup routine and link directive file and adjust them if necessary.

Startup routine: ig3_start.sLink directive file: ig3_link.dir

Target Readers

This Application Note is intended for users who understand the functions of the V850E/IF3 (μ PD70F3451, 70F3452), and V850E/IG3 (μ PD70F3453, 70F3454), and who design application systems that use these microcontrollers.

Purpose

This manual is intended to give users an understanding of the basic functions of the V850E/IF3 and V850E/IG3, using the application programs.

How to Use This Manual

It is assumed that the reader of this Application Note has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

For details of hardware functions (especially register functions, setting methods, etc.) and electrical specifications

→ See the V850E/IF3, V850E/IG3 Hardware User's Manual.

For details of instruction functions

→ See the **V850E1 Architecture User's Manual**.

Conventions

Data significance: Higher digits on the left and lower digits on the right

Active low representation: \overline{xxx} (overscore over pin or signal name)

Memory map address: Higher addresses on the top and lower addresses on

the bottom

Note: Footnote for item marked with **Note** in the text

Caution: Information requiring particular attention

Remark: Supplementary information Numeric representation: Binary ... xxxx or xxxxB

Decimal ... xxxx

Hexadecimal ... xxxxH

Prefix indicating the power

of 2 (address space,

memory capacity): K (kilo): $2^{10} = 1,024$

M (mega): $2^{20} = 1,024^2$ G (giga): $2^{30} = 1,024^3$ The function lists are structured as follows.

Theme

[Function] Function description [Function name] Name of sample function [Argument(s)] Type and overview of argument(s) [Processing content] Processing content of sample function [SFR(s) used] Register name and setting content [call function(s)] Name and function of call function(s) [Variable(s)] Type, name, and overview of variable(s) used in sample function [Interrupt(s)] Name of function [Interrupt source(s)] Name [File name] Name of corresponding sample program file [Caution(s)] Caution(s) upon function usage

Interrupt function

[Function name]	Name of interrupt function
[Overview]	Servicing content
[Source(s)]	Name of interrupt and conditions for occurrence
[call function(s)]	None
[Variable(s)]	Name of variable, function
[File name]	Name of corresponding sample program file
[Caution(s)]	None

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850E/IF3 and V850E/IG3

Document Name	Document No.
V850E1 Architecture User's Manual	U14559E
V850E/IF3, V850E/IG3 Hardware User's Manual	U18279E
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTA) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTB) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (CSIB) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (I ² C) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for DMA Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer M Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Watchdog Timer Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer AA Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer AB Application Note	This manual
V850E/IF3, V850E/IG3 Sample Programs for Timer T Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Port Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Clock Generator Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Standby Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Interrupt Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for A/D Converters 0 and 1 Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for A/D Converter 2 Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Low-Voltage Detector (LVI) Function Application Note	To be prepared
V850E/IF3, V850E/IG3 6-Phase PWM Output Control by Timer AB, Timer Q Option, Timer AA, A/D Converters 0 and 1 Application Note	U18717E

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CHAPTER 1 INTERVAL TIMER MODE

[Function] Starts 16-bit counter operation by setting the TAB0CTL0.TAB0CE bit to 1.

Outputs an interrupt request signal (INTTB0CC0) at an interval set by the TAB0CCR0

register.

Inverts the TOB00 pin output when the value set by the CCR0 buffer register and the

count value of the 16-bit counter match.

Inverts the TOB01 pin output when the value set by the CCR1 buffer register and the

count value of the 16-bit counter match.

Can be implemented with TAB0 and TAB1.

[Function name] main

[Argument] None

[Processing content] Performs count operation of an fxx/32 count clock, generates an interrupt by inverting the

TOB00 pin output upon the count subsequent to the count whose value matches the

value of the CCR0 buffer register, and clears the 16-bit counter.

Generates an interrupt by inverting the TOB01 pin output upon the count subsequent to

the count whose value matches the value of the CCR1 buffer register.

TOB00 and TOB01 pins start output at high level.

[SFR used] None

[call function] timerab_interval_ini, timerab_interval_st

[Variable] None

[Interrupts] timerab_TAB0CC0_int

timerab_TAB0CC1_int

[Interrupt sources] INTTB0CC0

INTTB0CC1

[File name] timerab_interval\MAIN.C

[Caution] None

The interval time can be calculated by the following formula.

Interval = (Set value of TAB0CCR0 register + 1) \times Count clock cycle

[Function name] timerab_interval_ini

[Argument] None

[Processing content] Sets operation and interrupts of TAB0.

[SFRs used] TAB0CTL0.TAB0CE: 0 (Disables TAB0 operation.)

PFC1: 0x00 (TOB00 output pin, TOB01 output pin)
PFCE1: 0x01 (TOB00 output pin, TOB01 output pin)
PMC1: 0x81 (TOB00 output pin, TOB01 output pin)

IMR1.TB0CCMK0: 0 (Enables INTTB0CC0 interrupt.)
 IMR1.TB0CCMK1: 0 (Enables INTTB0CC1 interrupt.)
 IMR1.TB0CCMK2: 1 (Disables INTTB0CC2 interrupt.)
 IMR1.TB0CCMK3: 1 (Disables INTTB0CC3 interrupt.)

[call function] timerab_interval

[Variable] None

[File name] timerab_interval\timerab_1.c

[Caution] None

[Function name] timerab_interval

[Argument] None

[Processing content] Sets TAB0 control register.

[SFRs used] TABOCTL0: 0x05 (Sets count clock to fxx/32.)

TAB0CTL1: 0x00 (Sets interval timer mode.)

TAB0IOC0: 0xA5 (Sets TOB00 pin and TOB01 pin output to high-level start,

enables timer output.

Sets TOB02 pin and TOB03 pin output to low-level start,

disables timer output.)

TAB0CCR0: 4999 (Compare register of 16-bit counter)
TAB0CCR1: 2499 (Compare register of 16-bit counter)
TAB0CCR2: 0xFFFF (Compare register of 16-bit counter)
TAB0CCR3: 0xFFFF (Compare register of 16-bit counter)

[call function] None

[Variable] None

[File name] timerab_interval\timerab_1.c

[Caution] • When the TABOCCR2 and TABOCCR3 registers are not used, it is recommended to set

the TABOCCR2 and TABOCCR3 registers to FFFFH. Mask the interrupt mask flag

(IMR1.TB0CCMK2, IMR1.TB0CCMK3).

[Function name] timerab_interval_st

[Argument] None

[Processing content] Starting function of timerab_interval.

[Starting method] Call this function after the timerab_interval function.

[SFR used] TAB0CTL0.TAB0CE:1 (Enables TAB0 operation.)

[call function] None
[Variable] None

[File name] timerab_interval\timerab_1.c

[Caution] None

Interrupt function

[Function name] timerab_TAB0CC0_int

[Overview] Defined by the user.

[Source] INTTB0CC0 Match between the count value of the 16-bit counter and CCR0

buffer register

[call function] None

[Variable] None

[File name] timerab_interval\timerab_1.c

[Caution] None

[Function name] timerab_TAB0CC1_int

[Overview] Defined by the user.

[Source] INTTB0CC1 Match between the count value of the 16-bit counter and CCR1

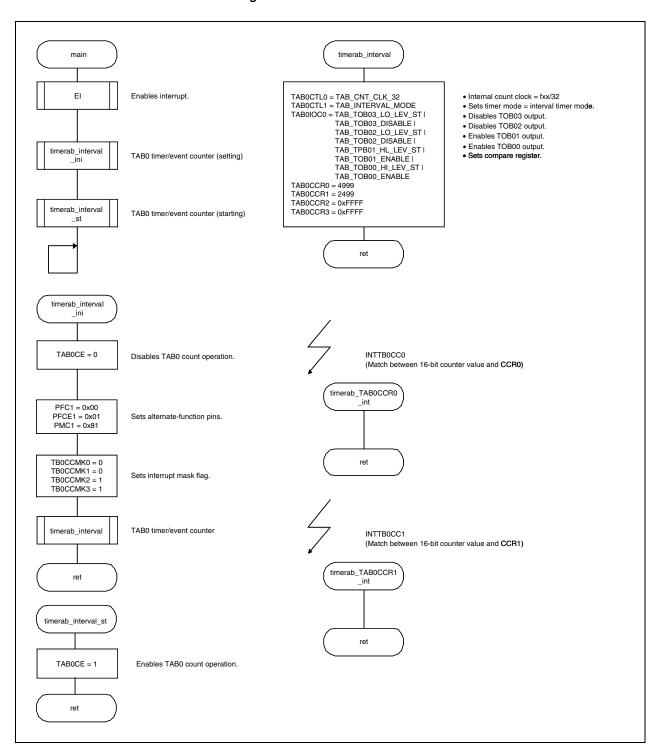
buffer register

[call function] None

[Variable] None

[File name] timerab_interval\timerab_1.c

Figure 1-1. Interval Timer Mode



CHAPTER 2 EXTERNAL EVENT COUNT MODE

[Function] Counts the valid edge of the external event count input (EVTB0 pin) and generates an

interrupt request signal (INTTB0CC0) each time the count reaches the count value set by

the TABOCCR0 register. (Clears the 16-bit counter simultaneously.)

Generates an interrupt request signal (INTTB0CC1) when the value set by the CCR1 buffer

register and the count value of the 16-bit counter match.

Can be implemented with TAB0 and TAB1.

[Function name] main

[Argument] None

[Processing content] Counts the valid edge of the external event count input, generates an interrupt upon the

count subsequent to the count whose value matches the value of the CCR0 buffer register,

and clears the 16-bit counter.

Generates an interrupt upon the count subsequent to the count whose value matches the

value of the CCR1 buffer register.

[SFR used] None

[call function] timerab_event_count_ini, timerab_event_count_st

[Variable] None

[Interrupts] timerab_TAB0CC0_int

timerab_TAB0CC1_int

[Interrupt sources] INTTB0CC0

INTTB0CC1

[File name] timerab_event_count\MAIN.C

[Function name] timerab_event_count_ini

[Argument] None

[Processing content] Sets the TABO operation and interrupts, and sets the alternate-function of the P14 pin to

the EVTB0 input pin.

[SFR used] TAB0CTL0.TAB0CE:0 (Disables TAB0 operation.)

PFC1: 0x10 (Sets EVTB0 input pin.)
PFCE1: 0x00 (Sets EVTB0 input pin.)
PMC1: 0x10 (Sets EVTB0 input pin.)
IMR1.TB0CCMK0: 0 (Enables INTTB0CC0 interrupt.)
IMR1.TB0CCMK1: 0 (Enables INTTB0CC1 interrupt.)
IMR1.TB0CCMK2: 1 (Disables INTTB0CC2 interrupt.)

IMR1.TB0CCMK3: 1 (Disables INTTB0CC3 interrupt.)

[call function] timerab_event_count

[Variable] None

[File name] timerab_event_count\timerab_2.c

[Caution] None

[Function name] timerab_event_count

[Argument] None

[Processing content] Sets TAB0 control register.

[SFR used] TAB0CTL0: 0x00 (Sets count clock.)

TAB0CTL1: 0x01 (Sets external event count mode.)

TAB0IOC2: 0x08 (Sets valid edge of the external event count input signal

(EVTB0 pin) to falling edge detection.)

TAB0CCR0: 40 (Compare register of 16-bit counter)
TAB0CCR1: 20 (Compare register of 16-bit counter)
TAB0CCR2: 0xFFFF (Compare register of 16-bit counter)
TAB0CCR3: 0xFFFF (Compare register of 16-bit counter)

[call function] None

[Variable] None

[File name] timerab_event_count\timerab_2.c

• When the TABOCCR2 and TABOCCR3 registers are not used, it is recommended to set

the TABOCCR2 and TABOCCR3 registers to FFFFH. Mask the interrupt mask flag

(IMR1.TB0CCMK2, IMR1.TB0CCMK3).

• The following caution is required to set register.

Set TAB0IOC0 to 0x00.

CHAPTER 2 EXTERNAL EVENT COUNT MODE

[Function name] timerab_event_count_st

[Argument] None

[Processing content] Starting function of timerab_event_count.

[Starting method] Call this function after calling the timerab_event_count function.

[SFR used] TAB0CTL0.TAB0CE:1 (Enables TAB0 operation.)

[call function] None
[Variable] None

[File name] timerab_event_count\timerab_2.c

[Caution] None

Interrupt function

[Function name] timerab_TAB0CC0_int

[Overview] Defined by the user.

[Source] INTTB0CC0 Match between the count value of the 16-bit counter and CCR0 buffer

register

[call function] None

[Variable] None

[File name] timerab_event_count\timerab_2.c

[Caution] None

[Function name] timerab_TAB0CC1_int

[Overview] Defined by the user.

[Source] INTTB0CC1 Match between the count value of the 16-bit counter and CCR1 buffer

register

[call function] None

[Variable] None

[File name] timerab_event_count\timerab_2.c

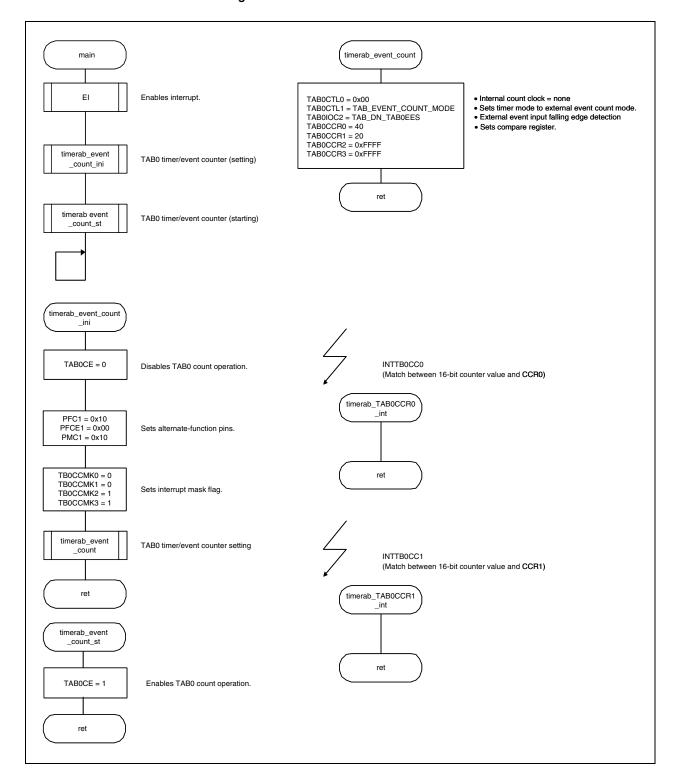


Figure 2-1. External Event Count Mode

CHAPTER 3 EXTERNAL TRIGGER PULSE OUTPUT MODE

[Function] Starts operation of the 16-bit counter by detecting the valid edge of the external event

count input (EVTB0 pin) when the valid edge of the external trigger input (TRGB0 pin) is

detected.

Inverters TOB00 pin output upon a match between the CCR0 buffer register value and the

16-bit counter value, and clears the 16-bit counter.

Inverts the TOB01 pin output upon a match between the CCR1 buffer register value and

the 16-bit counter value.

Inverts the TOB01 pin output when the 16-bit counter is cleared.

Can be implemented with TAB0 and TAB1.

[Function name] main

[Argument] None

[Processing content] Starts count operation by detecting the valid edge of the external event count input when

the valid edge of the external trigger input is detected, generates an interrupt by inverting the TOB00 pin output upon the count subsequent to the count whose value matches the

value of the CCR0 buffer register, and clears the 16-bit counter.

Generates an interrupt by inverting the TOB01 pin output upon a match between the count

value and the CCR1 buffer register value.

TOB00 and TOB01 pins start output at high level.

[SFR used] None

[call function] timerab_trigger_pulse_ini, timerab_trigger_pulse_st

[Variable] None

[Interrupts] timerab_TAB0CC0_int

timerab_TAB0CC1_int

[Interrupt sources] INTTB0CC0

INTTB0CC1

[File name] timerab_trigger_pulse\MAIN.C

[Caution] None

The active level width, cycle and duty factor of the PWM waveform can be calculated by the following formulas.

Active level width = (Set value of TAB0CCR1 register) \times Count clock cycle

Cycle = (Set value of TAB0CCR0 register + 1) × Count clock cycle

Duty factor = (Set value of TAB0CCR1 register) / (Set value of TAB0CCR0 register + 1)

[Function name] timerab_trigger_pulse_ini

[Argument] None

[Processing content] Sets the TABO operation and interrupts, and sets the alternate function of the P10 pin to

the TOB01 output, the P14 pin to the EVTB0 input, the P15 pin to the TRGB0 input, and

the P17 pin to the TOB00 output.

[SFRs used] TAB0CTL0.TAB0CE: 0 (Disables TAB0 operation.)

PFC1: 0x30 (Sets TOB01 output pin, EVTB0 input pin,

TRGB0 input pin, TOB00 output pin.)

PFCE1: 0x01 (Sets TOB01 output pin, EVTB0 input pin,

TRGB0 input pin, TOB00 output pin.)

PMC1: 0xB1 (Sets TOB01 output pin, EVTB0 input pin,

TRGB0 input pin, TOB00 output pin.)

IMR1.TB0CCMK0: 0 (Enables INTTB0CC0 interrupt.)
 IMR1.TB0CCMK1: 0 (Enables INTTB0CC1 interrupt.)
 IMR1.TB0CCMK2: 1 (Disables INTTB0CC2 interrupt.)
 IMR1.TB0CCMK3: 1 (Disables INTTB0CC3 interrupt.)

[call function] timerab_trigger_pulse

[Variable] None

[File name] timerab_trigger_pulse\timerab_3.c

[Function name] timerab_trigger_pulse

[Argument] None

[Processing content]

Sets TAB0 control register.

[SFRs used]

TAB0CTL0: 0x00 (Sets count clock.)

TABOCTL1: 0x62 (Enables operation with the external event count input signal

(EVTB0 pin), sets external trigger pulse output mode.)

TAB0IOC0: 0xA5 (Sets TOB00 and TOB01 pins' output to high-level start, enables

timer output, sets TOB02 and TOB03 pins' output to low-level

start, disables timer output.)

TABIOC2: 0x0A (Sets valid edges of the external event count input signal (EVTB0

pin) and external trigger input signal (TRGB0 pin) to falling edge

detection.)

TAB0CCR0: 40 (Compare register of 16-bit counter)
TAB0CCR1: 10 (Compare register of 16-bit counter)
TAB0CCR2: 0xFFFF (Compare register of 16-bit counter)
TAB0CCR3: 0xFFFF (Compare register of 16-bit counter)

[call function] None
[Variable] None

[File name] timerab_trigger_pulse\timerab_3.c

[Cautions]

The compare registers are rewritten in the batch write mode.
 To rewrite the compare register value during timer operation, rewrite the TABOCCR1 register last.

 When the TAB0CCR2 and TAB0CCR3 registers are not used, it is recommended to set the TAB0CCR2 and TAB0CCR3 registers to FFFFH. Mask with the interrupt mask flag (IMR1.TB0CCMK2, IMR1.TB0CCMK3). [Function name] timerab_trigger_pulse_st

[Argument] None

[Processing content] Starting function of timerab_trigger_pulse

[Starting method] Call this function after calling the timerab_trigger_pulse function.

[SFR used] TAB0CTL0.TAB0CE:1 (Enables TAB0 operation.)

[call function] None
[Variable] None

[File name] timerab_trigger_pulse\timerab_3.c

[Caution] None

Interrupt function

[Function name] timerab_TAB0CCR0_int

[Overview] Defined by the user.

[Source] INTTB0CC0 Match between the count value of the 16-bit counter and CCR0 buffer

register

[call function] None

[Variable] None

[File name] timerab_trigger_pulse\timerab_3.c

[Caution] None

[Function name] timerab_TAB0CC1_int

[Overview] Defined by the user.

[Source] INTTB0CC1 Match between the count value of the 16-bit counter and CCR1 buffer

register

[call function] None

[Variable] None

[File name] timerab_trigger_pulse\timerab_3.c

main timerab_trigger_pulse ΕI Enables interrupt. TABOCTL0 = 0x00 TABOCTL1 = TAB_EXT_TRIGGER | • Internal count clock = none TAB_EVENT_COUNT
TAB_TRIGGER_PULSE MODE • Enables external event count input. Sets timer mode to external trigger pulse TABOIOCO = TAB_TOBO3_LO_LEV_ST |
TAB_TOBO3_DISABLE |
TAB_TOBO2_LO_LEV_ST | output mode. timerab_trigger _pulse_ini Disables TOB03 output.Disables TOB02 output. TAB0 timer/event counter (setting) TAB_TOB02_DISABLE |
TAB_TPB01_HL_LEV_ST |
TAB_TOB01_ENABLE |
TAB_TOB00_HI_LEV_ST | Enables TOB01 output. • Enables TOB00 output. • External event count input, TAB_TOB00_ENABLE
TABOIOC2= TAB_DN_TABOEES |
TAB_DN_TABOETS external trigger input falling edge detection timerab trigger TAB0 timer/event counter (starting) Sets compare register. _pulse_st TABOCCR0 = 40 TABOCCR1 = 10 TABOCCR2 = 0xFFFF TABOCCR3 = 0xFFFF ret timerab_trigger_ TAB0CE = 0 Disables TAB0 count operation. INTTB0CC0 (Match between 16-bit counter value and CCR0) PFC1 = 0x30 PFCE1 = 0x01 PMC1 = 0xB1 Sets alternate-function pins. timerab_TAB0CC0_int TB0CCMK0 = 0 TB0CCMK1 = 0 TB0CCMK2 = 1 TB0CCMK3 = 1 Sets interrupt mask flag. timerab_trigger _pulse TAB0 timer/event counter setting INTTB0CC1 (Match between 16-bit counter value and CCR1) ret timerab_TAB0CC1_int timermt trigger TAB0CE = 1 Enables TAB0 count operation. ret

Figure 3-1. External Trigger Pulse Output Mode

CHAPTER 4 ONE-SHOT PULSE OUTPUT MODE

[Function] Starts operation of the 16-bit counter by detecting the valid edge of the external event

count input (EVTB0 pin) when the valid edge of the external trigger input (TRGB0 pin) is

detected.

Inverts the TOB00 pin output upon a match between the CCR0 buffer register value and

the 16-bit counter value, and clears the 16-bit counter to stop count operation.

Inverts the TOB01 pin output upon a match between the CCR1 buffer register value and

the 16-bit counter value.

Inverts the TOB01 pin output when the 16-bit counter is cleared.

Can be implemented with TAB0 and TAB1.

[Function name] main

[Argument] None

[Processing content] Starts count operation by detecting the valid edge of the external event count input when

the valid edge of the external trigger input is detected, generates an interrupt by inverting the TOB00 pin output upon the count subsequent to the count whose value matches the value of the CCR0 buffer register, and clears the 16-bit counter to stop the count operation. Generates an interrupt by inverting the TOB01 pin output upon the count subsequent to the

count whose value matches the value of the CCR1 buffer register.

TOB00 and TOB01 pins start output at high level.

[SFR used] None

[call function] timerab_1shot_pulse_ini, timerab_1shot_pulse_st

[Variable] None

[Interrupts] timerab_TAB0CC0_int

timerab_TAB0CC1_int

[Interrupt sources] INTTB0CC0

INTTB0CC1

[File name] timerab_1shot_pulse\MAIN.C

[Caution] None

The output delay time and active level width of one-shot pulse can be calculated by the following formulas.

Output delay time = (Set value of TAB0CCR1 register) × Count clock cycle

Active level width = (Set value of TAB0CCR0 register - Set value of TAB0CCR1 register + 1) × Count clock cycle

[Function name] timerab_1shot_pulse_ini

[Argument] None

[Processing content] Sets the TABO operation and interrupts, and sets the alternate function of the P10 pin to

the TOB01 output, the P14 pin to the EVTB0 input, the P15 pin to the TRGB0 input, and

the P17 pin to the TOB00 output.

[SFRs used] TAB0CTL0.TAB0CE: 0 (Disables TAB0 operation.)

PFC1: 0x30 (Sets TOB01 output pin, EVTB0 input pin,

TRGB0 input pin, TOB00 output pin.)

PFCE1: 0x01 (Sets TOB01 output pin, EVTB0 input pin,

TRGB0 input pin, TOB00 output pin.)

PMC1: 0xB1 (Sets TOB01 output pin, EVTB0 input pin,

TRGB0 input pin, TOB00 output pin.)

IMR1.TB0CCMK0: 0 (Enables INTTB0CC0 interrupt.)
 IMR1.TB0CCMK1: 0 (Enables INTTB0CC1 interrupt.)
 IMR1.TB0CCMK2: 1 (Disables INTTB0CC2 interrupt.)
 IMR1.TB0CCMK3: 1 (Disables INTTB0CC3 interrupt.)

[call function] timerab_1shot_pulse

[Variable] None

[File name] timerab_1shot_pulse\timerab_4.c

[Function name] timerab_1shot_pulse

[Argument] None

[Processing content] Sets TAB0 control register.

[SFRs used] TAB0CTL0: 0x00 (Sets count clock.)

TAB0CTL1: 0x23 (Enables operation with the external event count input signal

(EVTB0 pin), sets one-shot pulse output mode.)

TAB0IOC0: 0xA5 (Sets TOB00 and TOB01 pins' output to high-level start,

enables timer output,

sets TOB02 and TOB03 pins' output to low-level start, disables

timer output.)

TAB0IOC2: 0x0A (Sets valid edges of the external event count input signal

(EVTB0 pin) and the external trigger input signal (TRGB0 pin)

to falling edge detection.)

TAB0CCR0: 40 (Compare register of 16-bit counter)
TAB0CCR1: 20 (Compare register of 16-bit counter)
TAB0CCR2: 0xFFFF (Compare register of 16-bit counter)
TAB0CCR3: 0xFFFF (Compare register of 16-bit counter)

[call function] None

[Variable] None

[File name] timerab_1shot_pulse\timerab_4.c

[Caution] • When the TABOCCR2 and TABOCCR3 registers are not used, it is recommended to set

the TAB0CCR2 and TAB0CCR3 registers to FFFFH. Mask with the interrupt mask flag

(IMR1.TB0CCMK2, IMR1.TB0CCMK3).

[Function name] timerab_1shot_pulse_st

[Argument] None

[Processing content] Starting function of timerab_1shot_pulse

[Starting method] Call this function after calling the timerab_1shot_pulse function.

[SFR used] TABOCTL0.TABOCE:1 (Enables TABO operation.)

[call function] None
[Variable] None

[File name] timerab_1shot_pulse\timerab_4.c

[Caution] None

Interrupt function

[Function name] timerab_TAB0CC0_int

[Overview] Defined by the user.

[Source] INTTB0CC0 Match between the count value of the 16-bit counter and CCR0 buffer

register

[call function] None

[Variable] None

[File name] timerab_1shot_pulse\timerab_4.c

[Caution] None

[Function name] timerab_TAB0CC1_int

[Overview] Defined by the user.

[Source] INTTB0CC1 Match between the count value of the 16-bit counter and CCR1 buffer

register

[call function] None

[Variable] None

[File name] timerab_1shot_pulse\timerab_4.c

main timerab_1shot_pulse ΕI Enables interrupt. TAB0CTL0 = 0x00 TAB0CTL1 = TAB_EXT_TRIGGER | TAB_EVENT_COUNT |
TAB_ISHOT_PULSE_MODE
TABOIOCO = TAB_TOB03_LO_LEV_ST | • Internal count clock = none • Enables external event count input. • Sets timer mode to one-shot pulse output mode. TAB_TOB03_DISABLE | TAB_TOB02_LO_LEV_ST | timerab 1shot • Disables TOB03 output. TAB0 timer/event counter (setting) _pulse_ini TAB_TOB02_DISABLE I Disables TOB02 output. TAB_TOB01_HL_LEV_ST |
TAB_TOB01_ENABLE |
TAB_TOB00_HI_LEV_ST |
TAB_TOB00_ENABLE • Enables TOB01 output. Enables TOB00 output. External event count input, external trigger input falling edge detection. timerab_1shot TABOIOC2= TAB_DN_TABOEES I TAB_DN_TABOETS TAB0 timer/event counter (starting) Sets compare register. _pulse_st TAB0CCR0 = 40 TAB0CCR1 = 20 TAB0CCR2 = 0xFFFF TAB0CCR3 = 0xFFFF ret timerab_1shot pulse ini TAB0CE = 0 Disables TAB0 count operation. INTTB0CC0 (Match between 16-bit counter value and CCR0) PFC1 = 0x30PFCE1 = 0x01 PMC1 = 0xB1 Sets alternate-function pins. timerab_TAB0CC0_int TB0CCMK0 = 0 TB0CCMK1 = 0 Sets interrupt mask flag. TB0CCMK2 = 1 TB0CCMK3 = 1 ret timerab_1shot TAB0 timer/event counter setting _pulse INTTB0CC1 (Match between 16-bit counter value and CCR1) ret timerab_TAB0CC1_int timerab_1shot _pulse_st TAB0CE = 1 Enables TAB0 count operation. ret ret

Figure 4-1. One-Shot Pulse Output Mode

CHAPTER 5 PWM OUTPUT MODE

[Function] Starts operation of the 16-bit counter by setting the TAB0CTL0.TAB0CE bit to 1.

Outputs a PWM waveform with a 50% duty factor whose half cycle is equal to the set value of the TABOCCR0 register + 1, by clearing the 16-bit counter upon a match with the CCR0

buffer register value and inverting the TOB00 pin output.

Inverts the TOB01 pin output upon a match between the CCR1 buffer register value and

the 16-bit counter value.

Inverts the TOB01 pin output when the 16-bit counter is cleared.

Can be implemented with TAB0 and TAB1.

[Function name] main

[Argument] None

[Processing content] Performs count operation of an fxx/32 count clock, generates an interrupt by inverting the

TOB00 pin output upon the count subsequent to the count whose value matches the value

of the CCR0 buffer register, and clears the 16-bit counter.

Generates an interrupt by inverting the TOB01 pin output upon the count subsequent to the

count whose value matches the value of the CCR1 buffer register.

Both TOB00 pin and TOB01 pin start output at high level.

[SFR used] None

[call function] timerab_pwm_output_ini, timerab_pwm_output_st

[Variable] None

[Interrupts] timerab_TAB0CC0_int

timerab_TAB0CC1_int

[Interrupt sources] INTTB0CC0

INTTB0CC1

[File name] timerab_pwm_output\MAIN.C

[Caution] None

The active level width, cycle, and duty factor of the PWM waveform output from the TOB01 pin can be calculated by the following formulas.

Active level width = (Set value of TAB0CCR1 register) × Count clock cycle

Cycle = (Set value of TAB0CCR0 register + 1) × Count clock cycle

Duty factor = (Set value of TAB0CCR1 register) / (Set value of TAB0CCR0 register + 1)

[Function name] timerab_pwm_output_ini

[Argument] None

[Processing content] Sets the TAB0 operation and interrupts, sets the alternate function of the P10 pin to TOB01

output, and sets the alternate function of the P17 pin to TOB00 output.

[SFRs used] TAB0CTL0.TAB0CE: 0 (Disables TAB0 operation.)

PFC1: 0x00 (Sets TOB00 output pin, TOB01 output pin.)
PFCE1: 0x01 (Sets TOB00 output pin, TOB01 output pin.)
PMC1: 0x81 (Sets TOB00 output pin, TOB01 output pin.)

IMR1.TB0CCMK0: 0 (Enables INTTB0CC0 interrupt.)
 IMR1.TB0CCMK1: 0 (Enables INTTB0CC1 interrupt.)
 IMR1.TB0CCMK2: 1 (Disables INTTB0CC2 interrupt.)
 IMR1.TB0CCMK3: 1 (Disables INTTB0CC3 interrupt.)

[call function] timerab_pwm_output

[Variable] None

[File name] timerab_pwm_output\timerab_5.c

[Function name] timerab_pwm_output

[Argument] None

[Processing content] Sets TAB0 control register.

[SFRs used] TAB0CTL0: 0x05 (Sets count clock to fxx/32.)

TAB0CTL1: 0x04 (Sets PWM output mode.)

TAB0IOC0: 0xA5 (Sets TOB00 and TOB01 pins' output to high-level start, enables

timer output, sets TOB02 and TOB03 pins' output to low-level

start, disables timer output.)

TAB0IOC2: 0x00 (Sets valid edge of the external event count input signal (EVTB0

pin) to no edge detection.)

TAB0CCR0: 4999 (Compare register of 16-bit counter)
TAB0CCR1: 1249 (Compare register of 16-bit counter)
TAB0CCR2: 0xFFFF (Compare register of 16-bit counter)
TAB0CCR3: 0xFFFF (Compare register of 16-bit counter)

[call function] None
[Variable] None

[File name] timerab_pwm_output\timerab_5.c

[Cautions] • The compare registers are rewritten in the batch write mode.

To rewrite the compare register value during timer operation, rewrite the TAB0CCR1

register value last.

• When the TAB0CCR2 and TAB0CCR3 registers are not used, it is recommended to set

the TAB0CCR2 and TAB0CCR3 registers to FFFFH.

Mask with the interrupt mask flag (IMR1.TB0CCMK2, IMR1.TB0CCMK3).

[Function name] timerab_pwm_output_st

[Argument] None

[Processing content] Starting function of timerab_pwm_output

[Starting method] Call this function after calling the timerab_pwm_output function.

[SFR used] TAB0CTL0.TAB0CE: 1 (Enables TAB0 operation.)

[call function] None
[Variable] None

[File name] timerab_pwm_output\timerab_5.c

Interrupt function

[Function name] timerab_TAB0CC0_int [Overview] Defined by the user. INTTB0CC0 Match between the count value of the 16-bit counter and CCR0 buffer [Source] register [call function] None [Variable] None [File name] timerab_pwm_output\timerab_5.c [Caution] None

[Function name] timerab_TAB0CC1_int [Overview] Defined by the user.

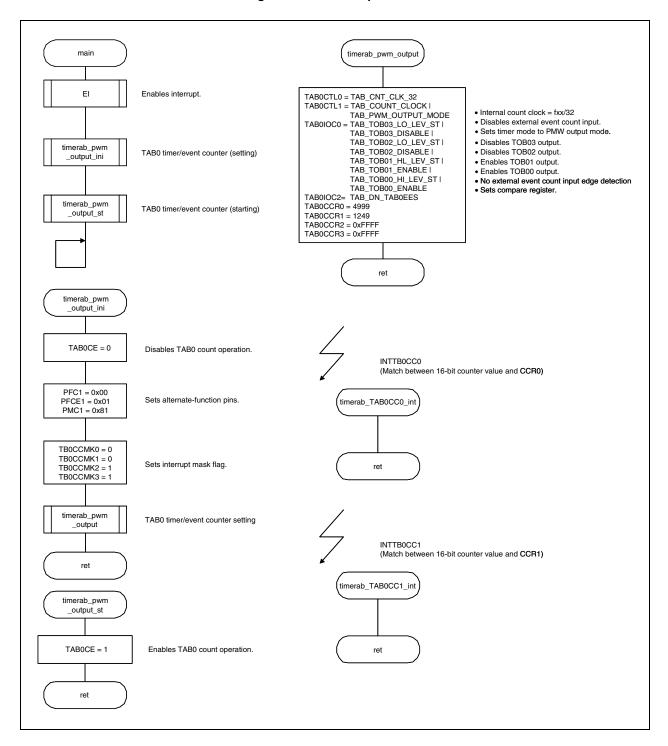
[Source] INTTB0CC1 Match between the count value of the 16-bit counter and CCR1 buffer

register

[call function] None
[Variable] None

[File name] timerab_pwm_output\timerab_5.c

Figure 5-1. PWM Output Mode



CHAPTER 6 FREE-RUNNING TIMER MODE

[Function] Starts operation of the 16-bit counter by setting the TAB0CTL0.TAB0CE bit to 1.

Inverts the TOB00 pin output upon a match between the CCR0 buffer register and the

count value of the 16-bit counter (compare function).

Stores the count value of the 16-bit counter in the TABOCCR1 register when the valid edge

of the capture trigger input (TIB01 pin) is detected (capture function).

After counting up to FFFFH, generates an overflow interrupt request signal (INTTB0OV) at

the next clock and clears to 0000H to continue counting.

The compare function and capture function can be implemented with TAB0 and TAB1.

[Function name] main

[Argument] None

[Processing content] Performs count operation of an fxx/32 count clock, generates an interrupt by inverting the

TOB00 pin output upon the count subsequent to the count whose value matches the value

of the CCR0 buffer register, and clears the 16-bit counter.

Generates an interrupt by capturing the counter value to the TABOCCR1 register when a

valid edge is detected from the TIB01 pin.

Generates an INTTB0OV interrupt when a counter overflow is detected.

The TOB00 pin start output at high level.

[SFR used] None

[call function] timerab_free_running_ini, timerab_free_running_st

[Variable] None

[Interrupts] timerab_TAB0CC0_int

timerab_TAB0CC1_int timerab_TAB0OV_int

[Interrupt sources] INTTB0CC0

INTTB0CC1 INTTB0OV

[File name] timerab_free_running \MAIN.C

CHAPTER 6 FREE-RUNNING TIMER MODE

[Function name] timerab_free_running_ini

[Argument] None

[Processing content] Sets the TAB0 operation and interrupts, and sets the alternate function of the P10 pin to

the TIB01 input, and the P17 pin to the TOB00 output.

[SFRs used] TAB0CTL0.TAB0CE: 0 (Disables TAB0 operation.)

PFC1: 0x01 (Sets TOB00 output pin, TIB01 input pin.)
PFCE1: 0x00 (Sets TOB00 output pin, TIB01 input pin.)
PMC1: 0x81 (Sets TOB00 output pin, TIB01 input pin.)

IMR1.TB0CCMK0: 0 (Enables INTTB0CC0 interrupt.)
 IMR1.TB0CCMK1: 0 (Enables INTTB0CC1 interrupt.)
 IMR1.TB0CCMK2: 1 (Disables INTTB0CC2 interrupt.)
 IMR1.TB0CCMK3: 1 (Disables INTTB0CC3 interrupt.)
 IMR1.TB0OVMK: 0 (Enables INTTB0OV interrupt.)

[call function] timerab_free_running

[Variable] None

[File name] timerab_free_running\timerab_6.c

[Function name] timerab_free_running

[Argument] None

[Processing content] Sets TAB0 control register.

[SFRs used] TAB0CTL0: 0x05 (Sets count clock to fxx/32.)

TAB0CTL1: 0x05 (Sets free-running timer mode.)

TAB0IOC0: 0xA9 (Sets TOB00 pin output to high-level start, enables timer output,

sets TOB01 to TOB03 pins' output to low-level start, disables

timer output.)

TAB0IOC1: 0x08 (Sets valid edge of the capture trigger input signal (TIB01 pin) to

falling edge detection.)

TAB0IOC2: 0x00 (Sets valid edge of the external event count input signal (EVTB0

pin) to no edge detection.)

TAB0OPT0: 0x20 (Sets TAB0CCR0, TAB0CCR2, and TAB0CCR3 as compare

registers, and TAB0CCR1 as capture register.)

TAB0CCR0: 4999 (Compare register of 16-bit counter)
TAB0CCR2: 0xFFFF (Compare register of 16-bit counter)
TAB0CCR3: 0xFFFF (Compare register of 16-bit counter)

[call function] None
[Variable] None

[File name] timerab_free_running\timerab_6.c

[Caution] • When the TAB0CCR2 and TAB0CCR3 registers

When the TABOCCR2 and TABOCCR3 registers are not used, it is recommended to set

the TAB0CCR2 and TAB0CCR3 registers to FFFFH. Mask with the interrupt mask flag

(IMR1.TB0CCMK2, IMR1.TB0CCMK3).

[Function name] timerab_free_running_st

[Argument] None

[Processing content] Starting function of timerab_free_running

[Starting method] Call this function after calling the timerab_free_running function.

[SFR used] TAB0CTL0.TAB0CE: 1 (Enables TAB0 operation.)

[call function] None
[Variable] None

[File name] timerab_free_running\timerab_6.c

Interrupt function

[Function name] timerab_TAB0CC0_int

[Overview] Defined by the user.

[Source] INTTB0CC0 Match between the count value of the 16-bit counter and CCR0 buffer

register

[call function] None
[Variable] None

[File name] timerab_free_running\timerab_6.c

[Caution] None

[Function name] timerab_TAB0CC1_int

[Overview] Defined by the user.

[Source] INTTB0CC1 Detects valid edge of the TIB01 pin input.

[call function] None
[Variable] None

[File name] timerab_free_running\timerab_6.c

[Caution] None

[Function name] timerab_TAB0OV_int

[Overview] Defined by the user.

[Source] INTTB0OV 16-bit counter overflow occurrence

[call function] None
[Variable] None

[File name] timerab_free_running\timerab_6.c

timerab_free main running TABOCTL0 = TAB_CNT_CLK_32
TABOCTL1 = TAB_COUNT_CLOCK |
TAB_FREE_RUNNING_MODE • Internal count clock = fxx/32 ΕI Enables interrupt. • Disables external event count input. · Sets timer mode to TAB0IOC0 = TAB_TOB03_LO_LEV_ST | free-running timer mode TAB_TOB03_DISABLE |
TAB_TOB02_LO_LEV_ST |
TAB_TOB02_DISABLE |
TAB_TOB01_LO_LEV_ST | • Disables TOB03 output. • Disables TOB02 output. timerab_free TAB0 timer/event counter (setting) • Disables TOB01 output. _running_ini • Enables TOB00 output. TAB_TOB01_DISABLE |
TAB_TOB00_HI_LEV_ST |
TAB_TOB00_ENABLE
= TAB_DIS_TIB03 | Capture trigger input (TIB01) falling edge detection. No external event count input edge detection timerab_free_ TAB0IOC1 TAB0 timer/event counter (starting) • TAB0CCR1 = capture register TAB_DIS_TIB02 | TAB_DN_TIB01 | running_st • TAB0CCR0, TAB0CCR2, TAB0CCR3 = TAB_DIS_TIB00
TAB0IOC2= TAB_DIS_TAB0EES compare registers
• Sets compare register. TABOOPTO = TAB_COMPARE_TABOCCR3 | TAB_COMPARE_TABOCCR2 | TAB0OVF is 1? TAB_CAPTURE_TAB0CCR1 | Yes TAB_CMPARE_TAB0CCR0 TAB0CCR0 = 4999 TAB0OVF = 0 Clears overflow flag. TAB0CCR2 = 0xFFFF TAB0CCR3 = 0xFFFF ret timerab free running_ini INTTB00V (16-bit counter overflow occurrence) TAB0CE = 0 Disables TAB0 count operation. timerab_TAB0OV_int PFC1 = 0x01PFCE1 = 0x00Sets alternate-function pins. PMC1 = 0x81 TB0CCMK0 = 0 ret TB0CCMK1 = 0 TB0CCMK2 = 1 Sets interrupt mask flag. INTTB0CC0 (Match between 16-bit counter value and TB0CCMK3 = 1TB0OVMK = 0 CCR0) timerab_TAB0CC0 timerab_free_ running TAB0 timer/event counter setting ret INTTB0CC1 (TIB01 pin falling edge detection) timerab_free _running_st timerab_TAB0CC1 TAB0CE = 1 Enables TAB0 count operation.

Figure 6-1. Free-Running Timer Mode

ret

ret

CHAPTER 7 PULSE WIDTH MEASUREMENT MODE

[Function] Starts operation of the 16-bit counter by setting the TABOCTL0.TABOCE bit to 1.

Stores the count value to the TABOCCR0 register when the valid edge of the capture

trigger input (TIB00 pin) is detected, and clears the 16-bit counter.

Measures the valid edge interval of the TIB00 pin by generating an interrupt when the valid

edge of the TIB00 pin input is detected and reading the TAB0CCR0 register value.

Can be implemented with TAB0 and TAB1.

[Function name] main

[Argument] None

[Processing content] Performs count operation of an fxx/32 count clock, generates an interrupt by storing the

count value of the 16-bit counter to the TABOCCR0 register when the valid edge of the

TIB00 pin input is detected, and clears the 16-bit counter.

Generates an INTTB0OV interrupt when a 16-bit counter overflow is detected.

[SFR used] None

[call function] timerab_pulse_measure_ini, timerab_pulse_measure_st

[Variable] None

[Interrupts] timerab_TAB0CC0_int

timerab_TAB0OV_int

[Interrupt sources] INTTB0CC0

INTTB0OV

[File name] timerab_pulse_measure\MAIN.C

[Caution] None

The pulse width can be calculated by the following formula.

Pulse width = captured value × Count clock cycle

The pulse width when the 16-bit counter overflow is detected can be calculated by the following formula.

Pulse width = (10000H × number of times the TAB0OVF bit is set + captured value) × count clock cycle

[Function name] timerab_pulse_measure_ini

[Argument] None

[Processing content] Sets the TAB0 operation and interrupts, sets the alternate function of the P13 pin to TIB00

input.

[SFRs used] TAB0CTL0.TAB0CE: 0 (Disables TAB0 operation.)

PFC1: 0x08 (Sets TIB00 input pin.) PFCE1: 0x00 (Sets TIB00 input pin.) PMC1: 0x08 (Sets TIB00 input pin.) IMR1.TB0CCMK0: 0 (Enables INTTB0CC0 interrupt.) IMR1.TB0CCMK1: 1 (Disables INTTB0CC1 interrupt.) IMR1.TB0CCMK2: 1 (Disables INTTB0CC2 interrupt.) IMR1.TB0CCMK3: 1 (Disables INTTB0CC3 interrupt.) IMR1.TB0OVMK: 0 (Enables INTTB0OV interrupt.)

[call function] timerab_pulse_measure

[Variable] None

[File name] timerab_pulse_measure\timerab_7.c

[Caution] None

[Function name] timerab_pulse_measure

[Argument] None

[Processing content] Sets TAB0 control register.

[SFRs used] TAB0CTL0: 0x05 (Sets count clock to fxx/32.)

TAB0CTL1: 0x06 (Sets pulse width measurement mode.)

TAB0IOC1: 0x02 (Sets valid edge of the capture trigger input signal (TIB00 pin) to

falling edge detection.)

TAB0IOC2: 0x00 (Sets valid edge of the external event count input signal (EVTB0

pin) to no edge detection.)

TAB0OPT0: 0x00 (Sets to the initial value.)

[call function] None

[Variable] None

[File name] timerab_pulse_measure\timerab_7.c

CHAPTER 7 PULSE WIDTH MEASUREMENT MODE

[Function name] timerab_pulse_measure_st

[Argument] None

[Processing content] Starting function of timerab_pulse_measure

[Starting method] Call this function after calling the timerab_pulse_measure function.

[SFR used] TAB0CTL0.TAB0CE: 1 (Enables TAB0 operation.)

[call function] None
[Variable] None

[File name] timerab_pulse_measure\timerab_7.c

[Caution] None

Interrupt function

[Function name] timerab_TAB0CC0_int

[Overview] Defined by the user.

[Source] INTTB0CC0 TIB00 pin input valid edge detection

[call function] None
[Variable] None

[File name] timerab_pulse_measure\timerab_7.c

[Caution] None

[Function name] timerab_TAB0OV_int

[Overview] Defined by the user.

[Source] INTTB0OV 16-bit counter overflow occurrence

[call function] None

[Variable] None

[File name] timerab_pulse_measure\timerab_7.c

timerab_pulse main measure • Internal count clock = fxx/32 TABOCTL0 = TAB_CNT_CLK_32
TABOCTL1 = TAB_COUNT_CLOCK |
TAB_PULSE_MAASURE_MODE
TABOIC1 = TAB_DIS_TIB03 |
TAB_DIS_TIB02 |
TAB_DIS_TIB02 |
TAB_DIS_TIB03 | ΕI Enables interrupt. • Disables external event count input. • Sets timer mode to pulse width measure mode Capture trigger input (TIB00) falling edge detection TAB DIS TIB01 I timerab_pulse TAB0 timer/event counter (setting) • No external event count input edge detection TAB_DN_TIB00

TABOIOC2= TAB_DIS_TAB0EES timerab_pulse TAB0 timer/event counter (starting) _measure_st ret No TAB0OVF is 1? Yes Clears overflow flag. TAB0OVF = 0 INTTB0CC0 INTTB0OV (16-bit counter overflow occurrence) (TIB00 pin falling edge detection) timerab_pulse timerab_TAB0CC0 timerab_TAB0OV_int _measure_ini TAB0CE = 0 Disables TAB0 count operation. PFC1 = 0x08 PFCE1 = 0x00 PMC1 = 0x08 Sets alternate-function pins. TB0CCMK0 = 0 TB0CCMK1 = 1 TB0CCMK2 = 1 Sets interrupt mask flag. TB0CCMK3 = 1 TB0OVMK = 0 timerab_pulse TAB0 timer/event counter setting measure timerab pulse TAB0CE = 1 Enables TAB0 count operation. ret

Figure 7-1. Pulse Width Measurement Mode

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