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RENESAS

Preliminary Application Note

V850E/IF3, V850E/IG3

32-bit Single-Chip Microcontrollers

Sample Programs for Timer AA

V850E/IF3:
- μPD70F3451
- μPD70F3452

V850E/IG3:
- μPD70F3453
- μPD70F3454

Document No. U18730EJ1V0AN00 (1st edition)
Date Published September 2007 N

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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INTRODUCTION

Cautions 1. This Application Note explains a case where the V850E/IG3 is used as a representative microcontroller. Use this Application Note for your reference when using the V850E/IF3.

2. Download the program used in this manual from the page of Programming Examples (http://www.necel.com/micro/en/designsupports/sampleprogram/index.html) in the NEC Electronics Website (http://www.necel.com/).

3. The sample programs are provided for reference purposes only and operations are therefore not subject to guarantee by NEC Electronics Corporation. When using sample programs, customers are advised to sufficiently evaluate this product based on their systems, before use.

4. When using sample programs, reference the following startup routine and link directive file and adjust them if necessary.

- **Startup routine: ig3_start.s**
- **Link directive file: ig3_link.dir**

Target Readers

This Application Note is intended for users who understand the functions of the V850E/IF3 (μPD70F3451, 70F3452), and V850E/IG3 (μPD70F3453, 70F3454), and who design application systems that use these microcontrollers.

Purpose

This manual is intended to give users an understanding of the basic functions of the V850E/IF3 and V850E/IG3, using the application programs.

How to Use This Manual

It is assumed that the reader of this Application Note has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

For details of hardware functions (especially register functions, setting methods, etc.) and electrical specifications

→ See the **V850E/IF3, V850E/IG3 Hardware User's Manual**.

For details of instruction functions

→ See the **V850E1 Architecture User's Manual**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)
Memory map address:	Higher addresses on the top and lower addresses on the bottom
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB Decimal ... xxxx Hexadecimal ... xxxxH
Prefix indicating the power of 2 (address space, memory capacity):	K (kilo): $2^{10} = 1,024$ M (mega): $2^{20} = 1,024^2$ G (giga): $2^{30} = 1,024^3$

The function lists are structured as follows.

Theme

[Function]	Function description
[Function name]	Name of sample function
[Argument(s)]	Type and overview of argument(s)
[Processing content]	Processing content of sample function
[SFR(s) used]	Register name and setting content
[call function(s)]	Name and function of call function(s)
[Variable(s)]	Type, name, and overview of variable(s) used in sample function
[Interrupt(s)]	Name of function
[Interrupt source(s)]	Name
[File name]	Name of corresponding sample program file
[Caution(s)]	Caution(s) upon function usage

Interrupt function

[Function name]	Name of interrupt function
[Overview]	Servicing content
[Source(s)]	Name of interrupt and conditions for occurrence
[call function(s)]	None
[Variable(s)]	Name of variable, function
[File name]	Name of corresponding sample program file
[Caution(s)]	None

Product Differences The differences between the V850E/IG3 and the V850E/IF3, in relation to 16-bit timer/event counter AA (TAA), are shown below.

Item	V850E/IG3	V850E/IF3
TIA30, TIA31, TOA30, TOA31 pins	Provided	None

Item	TAA0	TAA1	TAA2	TAA3	TAA4
Interval timer	Provided	Provided	Provided	Provided	Provided
External event counter	None	None	Provided	**Note 1**	Provided
External trigger pulse output	None	None	Provided	**Note 1**	Provided
One-shot pulse output	None	None	Provided	**Note 1**	Provided
PWM output	None	None	Provided	**Note 1**	Provided
Free-running timer	Provided[Note 2]	Provided[Note 2]	Provided	Provided[Note 3]	Provided
Pulse width measurement	None	None	Provided	**Note 1**	Provided
Timer sychronous operation function	Provided (TAB0)	Provided (TAB1)	None	None	None

Notes 1. V850E/IF3: Not provided
V850E/IG3: Provided

2. Compare function only

3. Compare function only in V850E/IF3

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850E/IF3 and V850E/IG3

Document Name	Document No.
V850E1 Architecture User's Manual	U14559E
V850E/IF3, V850E/IG3 Hardware User's Manual	U18279E
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTA) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTB) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (CSIB) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (I^2C) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for DMA Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer M Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Watchdog Timer Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer AA Application Note	This manual
V850E/IF3, V850E/IG3 Sample Programs for Timer AB Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer T Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Port Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Clock Generator Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Standby Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Interrupt Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for A/D Converters 0 and 1 Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for A/D Converter 2 Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Low-Voltage Detector (LVI) Function Application Note	To be prepared
V850E/IF3, V850E/IG3 6-Phase PWM Output Control by Timer AB, Timer Q Option, Timer AA, A/D Converters 0 and 1 Application Note	U18717E

CONTENTS

[Function]	Starts 16-bit counter operation by setting the TAA2CTL0.TAA2CE bit to 1. Outputs an interrupt request signal (INTTA2CC0) at an interval set by the TAA2CCR0 register. Inverts the TOA20 pin output when the value set by the CCR0 buffer register and the count value of the 16-bit counter match. Inverts the TOA21 pin output when the value set by the CCR1 buffer register and the count value of the 16-bit counter match. Can be implemented with TAA0 to TAA4.
[Function name]	main
[Argument]	None
[Processing content]	Performs count operation of an fxx/64 count clock, generates an interrupt by inverting the TOA20 pin output upon the count subsequent to the count whose value matches the value of the CCR0 buffer register, and clears the 16-bit counter. Generates an interrupt by inverting the TOA21 pin output upon the count subsequent to the count whose value matches the value of the CCR1 buffer register. TOA20 and TOA21 pins start output at high level.
[SFR used]	None
[call function]	timeraa_interval_ini, timeraa_interval_st
[Variable]	None
[Interrupts]	timeraa_TAA2CC0_int timeraa_TAA2CC1_int
[Interrupt sources]	INTTA2CC0 INTTA2CC1
[File name]	timeraa_interval\MAIN.C
[Caution]	None

The interval time can be calculated by the following formula.

Interval = (Set value of TAA2CCR0 register + 1) × Count clock cycle

[Function name]	timeraa_interval_ini	
[Argument]	None	
[Processing content]	Sets the TAA2 operation and interrupts.	
[SFRs used]	TAA2CTL0.TAA2CE:	0 (Disables TAA2 operation.)
	PFC0:	0x00 (Sets TOA20 output pin, TOA21 output pin.)
	PFCE0:	0x00 (Sets TOA20 output pin, TOA21 output pin.)
	PMC0:	0x03 (Sets TOA20 output pin, TOA21 output pin.)
	IMR3.TA2CCMK0:	0 (Enables INTTA2CC0 interrupt.)
	IMR3.TA2CCMK1:	0 (Enables INTTA2CC1 interrupt.)
[call function]	timeraa_interval	
[Variable]	None	
[File name]	timeraa_interval\timeraa_1.c	
[Caution]	None	

[Function name]	timeraa_interval	
[Argument]	None	
[Processing content]	Sets TAA2 control register.	
[SFRs used]	TAA2CTL0:	0x04 (Sets count clock to fxx/64.)
	TAA2CTL1:	0x00 (Sets interval timer mode.)
	TAA2IOC0:	0x0F (Sets TOA20 and TOA21 pins' output to high-level start, enables timer output.)
	TAA2CCR0:	2499 (Compare register of 16-bit counter)
	TAA2CCR1:	1249 (Compare register of 16-bit counter)
[call function]	None	
[Variable]	None	
[File name]	timeraa_interval\timeraa_1.c	
[Caution]	None	

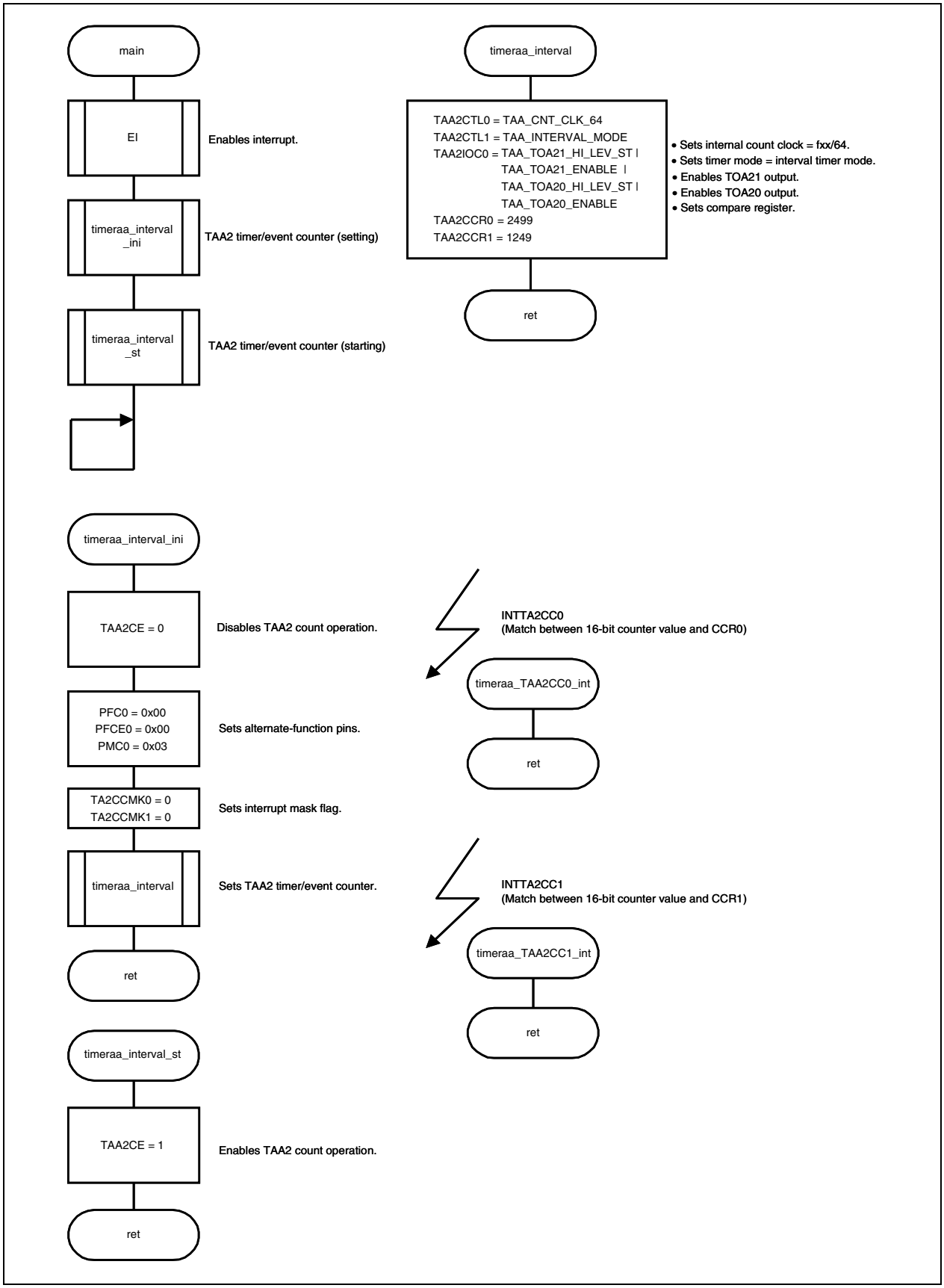
[Function name]	timeraa_interval_st
[Argument]	None
[Processing content]	Starting function of timeraa_interval
[Starting method]	Call this function after calling the timeraa_interval function.
[SFR used]	TAA2CTL0.TAA2CE: 1 (Enables TAA2 operation.)
[call function]	None
[Variable]	None
[File name]	timeraa_interval\timeraa_1.c
[Caution]	None

Interrupt function

[Function name]	timeraa_TAA2CC0_int	
[Overview]	Defined by the user.	
[Source]	INTTA2CC0	Match between the count value of the 16-bit counter and CCR0 buffer register
[call function]	None	
[Variable]	None	
[File name]	timeraa_interval\timeraa_1.c	
[Caution]	None	

[Function name]	timeraa_TAA2CC1_int	
[Overview]	Defined by the user.	
[Source]	INTTA2CC1	Match between the count value of the 16-bit counter and CCR1 buffer register
[call function]	None	
[Variable]	None	
[File name]	timeraa_interval\timeraa_1.c	
[Caution]	None	

Figure 1-1. Interval Timer Mode



CHAPTER 2 EXTERNAL EVENT COUNT MODE

[Function]	Counts the valid edge of the external event count input (TIA20 pin) and generates an interrupt request signal (INTTA2CC0) each time the count reaches the count value set by the TAA2CCR0 register. (Clears the 16-bit counter simultaneously.) Generates an interrupt request signal (INTTA2CC1) when the value set by the CCR1 buffer register and the count value of the 16-bit counter match. Can be implemented with TAA2 to TAA4.
[Function name]	main
[Argument]	None
[Processing content]	Counts the valid edge of the external event count input, generates an interrupt upon the count subsequent to the count whose value matches the value of the CCR0 buffer register, and clears the 16-bit counter. Generates an interrupt at the timing subsequent to the count whose value matches the value of the CCR1 buffer register.
[SFR used]	None
[call function]	timeraa_event_count_ini, timeraa_event_count_st
[Variable]	None
[Interrupts]	timeraa_TAA2CC0_int timeraa_TAA2CC1_int
[Interrupt sources]	INTTA2CC0 INTTA2CC1
[File name]	timeraa_event_count\MAIN.C
[Caution]	None

[Function name]	timeraa_event_count_ini	
[Argument]	None	
[Processing content]	Sets the TAA2 operation and interrupts, and sets the alternate function of the P00 pin to TIA20 input.	
[SFRs used]	TAA2CTL0.TAA2CE:	0 (Disables TAA2 operation.)
	PFC0:	0x01 (Sets TIA20 input pin.)
	PFCE0:	0x00 (Sets TIA20 input pin.)
	PMC0:	0x01 (Sets TIA20 input pin.)
	IMR3.TA2CCMK0:	0 (Enables INTTA2CC0 interrupt.)
	IMR3.TA2CCMK1:	0 (Enables INTTA2CC1 interrupt.)
[call function]	timeraa_event_count	
[Variable]	None	
[File name]	timeraa_event_count\timeraa_2.c	
[Caution]	None	

[Function name]	timeraa_event_count	
[Argument]	None	
[Processing content]	Sets TAA2 control register.	
[SFRs used]	TAA2CTL0:	0x00 (Sets count clock.)
	TAA2CTL1:	0x01 (Sets external event count mode.)
	TAA2IOC2:	0x08 (Sets valid edge of the external event count input signal (TIA20 pin) to falling edge detection.)
	TAA2CCR0:	40 (Compare register of 16-bit counter)
	TAA2CCR1:	20 (Compare register of 16-bit counter)
[call function]	None	
[Variable]	None	
[File name]	timeraa_event_count\timeraa_2.c	
[Caution]	The following caution is required to set the register. Set TAA2IOC0 to 0x00.	

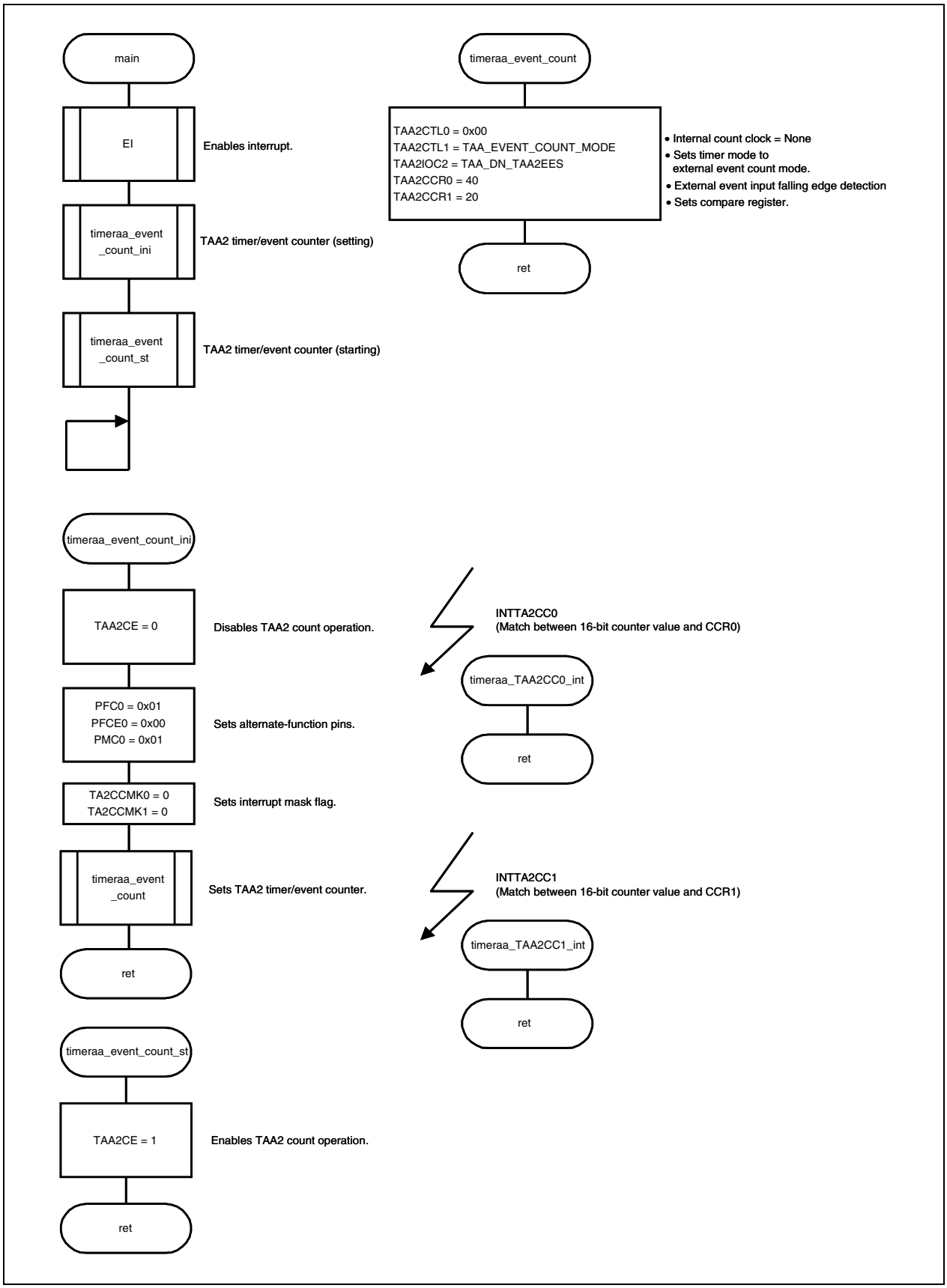
[Function name]	timeraa_event_count_st
[Argument]	None
[Processing content]	Starting function of timeraa_event_count
[Starting method]	Call this function after calling the timeraa_event_count function.
[SFR used]	TAA2CTL0.TAA2CE: 1 (Enables TAA2 operation.)
[call function]	None
[Variable]	None
[File name]	timeraa_event_count\timeraa_2.c
[Caution]	None

Interrupt function

[Function name]	timeraa_TAA2CC0_int	
[Overview]	Defined by the user.	
[Source]	INTTA2CC0	Match between the count value of the 16-bit counter and CCR0 buffer register
[call function]	None	
[Variable]	None	
[File name]	timeraa_event_count\timeraa_2.c	
[Caution]	None	

[Function name]	timeraa_TAA2CC1_int	
[Overview]	Defined by the user.	
[Source]	INTTA2CC1	Match between the count value of the 16-bit counter and CCR1 buffer register
[call function]	None	
[Variable]	None	
[File name]	timeraa_event_count\timeraa_2.c	
[Caution]	None	

Figure 2-1. External Event Count Mode



CHAPTER 3 EXTERNAL TRIGGER PULSE OUTPUT MODE

[Function]	Starts operation of the 16-bit counter when the valid edge of the external trigger input (TIA20 pin) is detected. Clears the 16-bit counter upon a match with the CCR0 buffer register. Inverts the TOA21 pin upon a match between the CCR1 buffer register value and the 16-bit counter value. Inverts the TOA21 pin when the 16-bit counter is cleared. Can be implemented with TAA2 to TAA4.
[Function name]	main
[Argument]	None
[Processing content]	Starts count operation of an fxx/64 count clock when the valid edge of the external trigger input is detected, generates an interrupt upon the count subsequent to the count whose value matches the value of the CCR0 buffer register, and clears the 16-bit counter. Generates an interrupt by inverting the TOA21 pin output upon a match between the CCR1 buffer register value and the 16-bit counter value. TOA21 pin starts output at high level.
[SFR used]	None
[call function]	timeraa_trigger_pulse_ini, timeraa_trigger_pulse_st
[Variable]	None
[Interrupts]	timeraa_TAA2CC0_int timeraa_TAA2CC1_int
[Interrupt sources]	INTTA2CC0 INTTA2CC1
[File name]	timeraa_trigger_pulse\MAIN.C
[Caution]	None

The active level width, cycle, and duty factor of the PWM waveform can be calculated by the following formula.

Active level width = (Set value of TAA2CCR1 register) × Count clock cycle

Cycle = (Set value of TAA2CCR0 register + 1) × Count clock cycle

Duty factor = (Set value of TAA2CCR1 register)/(Set value of TAA2CCR0 register + 1)

[Function name]	timeraa_trigger_pulse_ini	
[Argument]	None	
[Processing content]	Sets the TAA2 operation and interrupts, sets the alternate function of the P00 pin to TIA20 input, and sets alternate function of the P01 pin to TOA21 output.	
[SFRs used]	TAA2CTL0.TAA2CE:	0 (Disables TAA2 operation.)
	PFC0:	0x01 (Sets TIA20 input pin, TOA21 output pin.)
	PFCE0:	0x00 (Sets TIA20 input pin, TOA21 output pin.)
	PMC0:	0x03 (Sets TIA20 input pin, TOA21 output pin.)
	IMR3.TA2CCMK0:	0 (Enables INTTA2CC0 interrupt.)
	IMR3.TA2CCMK1:	0 (Enables INTTA2CC1 interrupt.)
[call function]	timeraa_trigger_pulse	
[Variable]	None	
[File name]	timeraa_trigger_pulse\timeraa_3.c	
[Caution]	None	

[Function name]	timeraa_trigger_pulse	
[Argument]	None	
[Processing content]	Sets TAA2 control register.	
[SFRs used]	TAA2CTL0:	0x04 (Sets count clock.)
	TAA2CTL1:	0x42 (Sets external trigger pulse output mode.)
	TAA2IOC0:	0x04 (Sets TOA21 pin output to high-level start, disables timer output, enables timer output.)
	TAA2IOC2:	0x02 (Sets valid edge of the external trigger input signal (TIA20 pin) to falling edge detection.)
	TAA2CCR0:	2499 (Compare register of 16-bit counter)
	TAA2CCR1:	1249 (Compare register of 16-bit counter)
[call function]	None	
[Variable]	None	
[File name]	timeraa_trigger_pulse\timeraa_3.c	
[Caution]	The compare registers are rewritten in the batch write mode. To rewrite the compare register during timer operation, rewrite the TAA2CCR1 register last.	

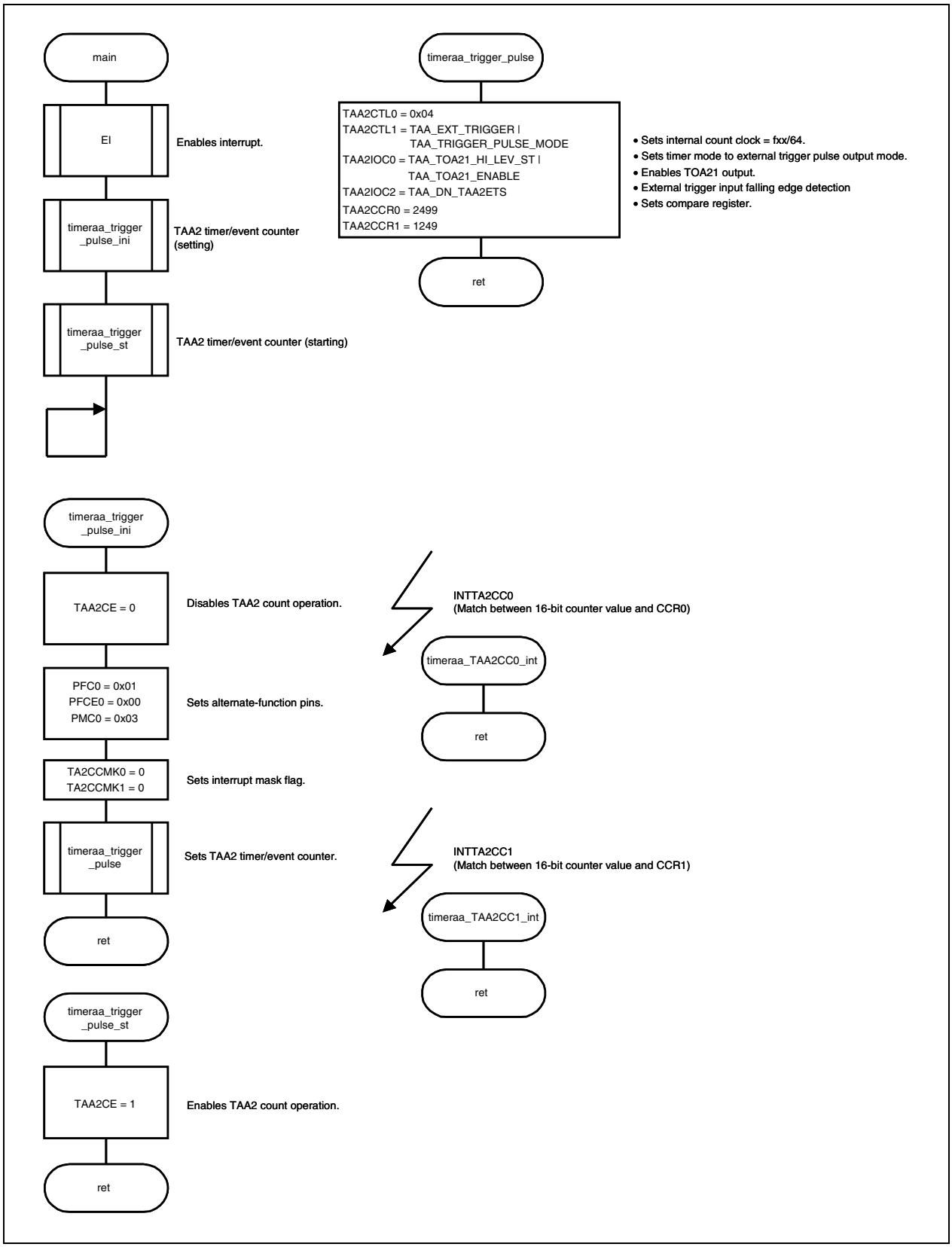
[Function name]	timeraa_trigger_pulse_st
[Argument]	None
[Processing content]	Starting function of timeraa_trigger_pulse
[Starting method]	Call this function after calling the timeraa_trigger_pulse function.
[SFR used]	TAA2CTL0.TAA2CE: 1 (Enables TAA2 operation.)
[call function]	None
[Variable]	None
[File name]	timeraa_trigger_pulse\timeraa_3.c
[Caution]	None

Interrupt function

[Function name]	timeraa_TAA2CC0_int	
[Overview]	Defined by the user.	
[Source]	INTTA2CC0	Match between the count value of the 16-bit counter and CCR0 buffer register
[call function]	None	
[Variable]	None	
[File name]	timeraa_trigger_pulse\timeraa_3.c	
[Caution]	None	

[Function name]	timeraa_TAA2CC1_int	
[Overview]	Defined by the user.	
[Source]	INTTA2CC1	Match between the count value of the 16-bit counter and CCR1 buffer register
[call function]	None	
[Variable]	None	
[File name]	timeraa_trigger_pulse\timeraa_3.c	
[Caution]	None	

Figure 3-1. External Trigger Pulse Output Mode



CHAPTER 4 ONE-SHOT PULSE OUTPUT MODE

[Function]	Starts operation of the 16-bit counter when the valid edge of the external trigger input (TIA20 pin) is detected. Clears the 16-bit counter upon a match with the CCR0 buffer register, and stops count operation. Inverts the TOA21 pin upon a match between the CCR1 buffer register value and the 16-bit counter value. Inverts the TOA21 pin when the 16-bit counter is cleared. Can be implemented with TAA2 to TAA4.
[Function name]	main
[Argument]	None
[Processing content]	Starts count operation of an fxx/64 count clock when the valid edge of the external trigger input is detected, generates an interrupt upon the count subsequent to the count whose value matches the value of the CCR0 buffer register, and clears the 16-bit counter to stop the count operation. Generates an interrupt by inverting the TOA21 pin output upon the count subsequent to the count whose value matches the value of the CCR1 buffer register. TOA21 pin starts output at high level.
[SFR used]	None
[call function]	timeraa_1shot_pulse_ini, timeraa_1shot_pulse_st
[Variable]	None
[Interrupts]	timeraa_TAA2CC0_int timeraa_TAA2CC1_int
[Interrupt sources]	INTTA2CC0 INTTA2CC1
[File name]	timeraa_1shot_pulse\MAIN.C
[Caution]	None

The output delay time and active level width of one-shot pulse can be calculated by the following formula.

Output delay time = (Set value of TAA2CCR1 register) × Count clock cycle

Active level width = (Set value of TAA2CCR0 register − Set value of TAA2CCR1 register + 1) × Count clock cycle

[Function name]	timeraa_1shot_pulse_ini	
[Argument]	None	
[Processing content]	Sets the TAA2 operation and interrupts, sets the alternate function of the P00 pin to TIA20 input, and sets the alternate function of the P01 pin to TOA21 output.	
[SFRs used]	TAA2CTL0.TAA2CE:	0 (Disables TAA2 operation.)
	PFC0:	0x01 (Sets TIA20 input pin, TOA21 output pin.)
	PFCE0:	0x00 (Sets TIA20 input pin, TOA21 output pin.)
	PMC0:	0x03 (Sets TIA20 input pin, TOA21 output pin.)
	IMR3.TA2CCMK0:	0 (Enables INTTA2CC0 interrupt.)
	IMR3.TA2CCMK1:	0 (Enables INTTA2CC1 interrupt.)
[call function]	timeraa_1shot_pulse	
[Variable]	None	
[File name]	timeraa_1shot_pulse\timeraa_4.c	
[Caution]	None	

[Function name]	timeraa_1shot_pulse	
[Argument]	None	
[Processing content]	Sets TAA2 control register.	
[SFRs used]	TAA2CTL0:	0x04 (Sets count clock.)
	TAA2CTL1:	0x43 (Sets one-shot pulse output mode.)
	TAA2IOC0:	0x04 (Sets TOA21 pin output to high-level start, enables timer output.)
	TAA2IOC2:	0x02 (Sets valid edge of the external trigger input signal (TIA20 pin) to falling edge detection.)
	TAA2CCR0:	2499 (Compare register of 16-bit counter)
	TAA2CCR1:	1249 (Compare register of 16-bit counter)
[call function]	None	
[Variable]	None	
[File name]	timeraa_1shot_pulse\timeraa_4.c	
[Caution]	None	

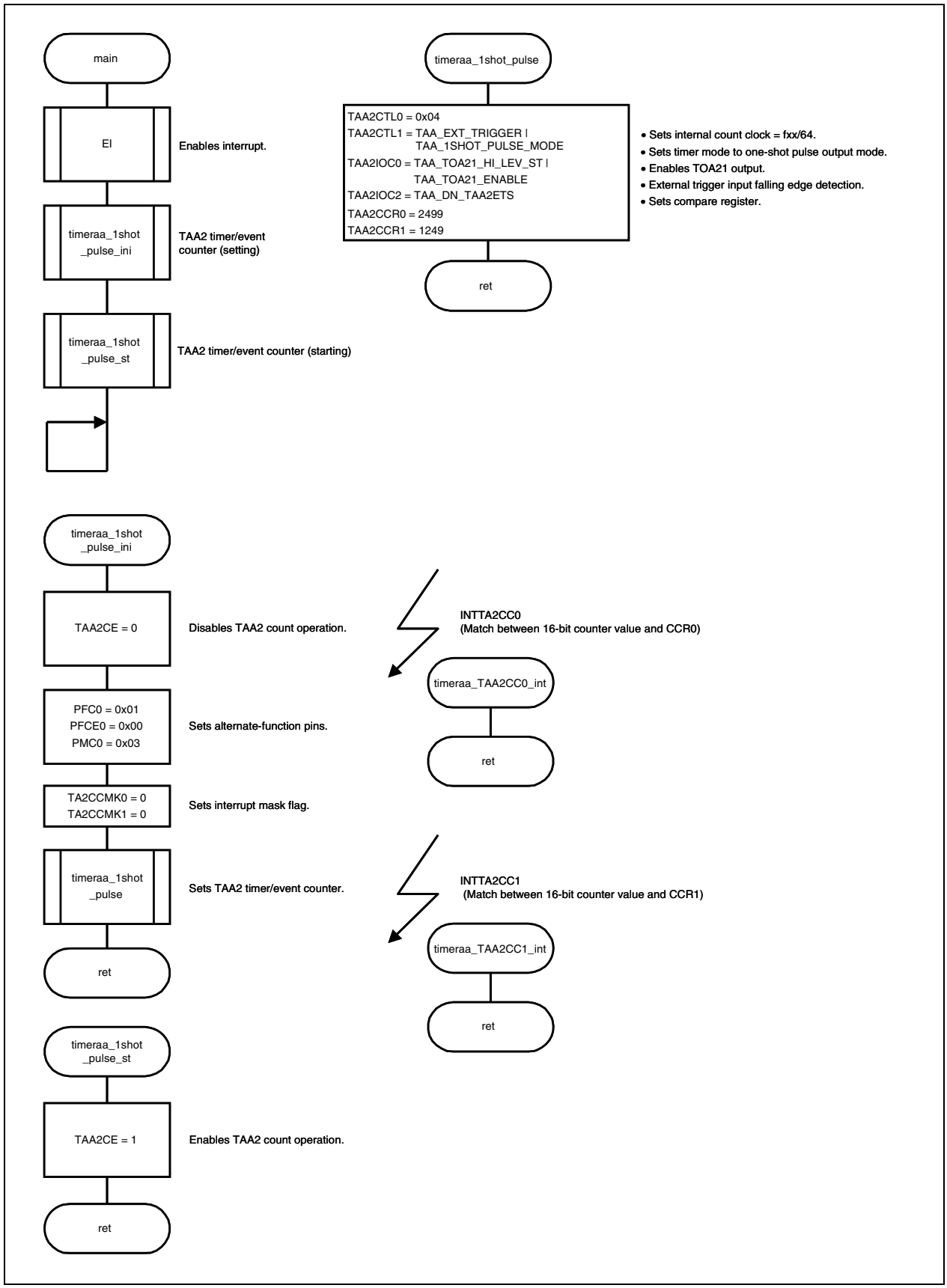
[Function name]	timeraa_1shot_pulse_st	
[Argument]	None	
[Processing content]	Starting function of timeraa_1shot_pulse	
[Starting method]	Call this function after calling the timeraa_1shot_pulse function.	
[SFR used]	TAA2CTL0.TAA2CE:	1 (Enables TAA2 operation.)
[call function]	None	
[Variable]	None	
[File name]	timeraa_1shot_pulse\timeraa_4.c	
[Caution]	None	

Interrupt function

[Function name]	timeraa_TAA2CC0_int	
[Overview]	Defined by the user.	
[Source]	INTTA2CC0	Match between the count value of the 16-bit counter and CCR0 buffer register
[call function]	None	
[Variable]	None	
[File name]	timeraa_1shot_pulse\timeraa_4.c	
[Caution]	None	

[Function name]	timeraa_TAA2CC1_int	
[Overview]	Defined by the user.	
[Source]	INTTA2CC1	Match between the count value of the 16-bit counter and CCR1 buffer register
[call function]	None	
[Variable]	None	
[File name]	timeraa_1shot_pulse\timeraa_4.c	
[Caution]	None	

Figure 4-1. One-Shot Pulse Output Mode



CHAPTER 5 PWM OUTPUT MODE

[Function]	Starts operation of the 16-bit counter by setting the TAA2CTL0.TAA2CE bit to 1. Clears the 16-bit counter upon a match with the CCR0 buffer register value, inverts the TOA20 pin output, and outputs a PWM waveform with a 50% duty factor whose half cycle is equal to the set value of the TAA2CCR0 register + 1. Inverts the TOA21 pin output upon a match between the CCR1 buffer register value and the 16-bit counter value. Inverts the TOA21 pin output when the 16-bit counter is cleared. Can be implemented with TAA2 to TAA4.
[Function name]	main
[Argument]	None
[Processing content]	Performs count operation of an fxx/64 count clock, generates an interrupt by inverting the TOA20 pin output upon the count subsequent to the count whose value matches the value of the CCR0 buffer register, and clears the 16-bit counter. Generates an interrupt by inverting the TOA21 pin output upon a match between the CCR1 buffer register value and the 16-bit counter value. Both TOA20 pin and TOA21 pin start output at high level.
[SFR used]	None
[call function]	timeraa_pwm_output_ini, timeraa_pwm_output_st
[Variable]	None
[Interrupts]	timeraa_TAA2CC0_int timeraa_TAA2CC1_int
[Interrupt sources]	INTTA2CC0 INTTA2CC1
[File name]	timeraa_pwm_output\MAIN.C
[Caution]	None

The active level width, cycle, and duty factor of the PWM waveform output from the TOA21 pin can be calculated by the following formula.

Active level width = (Set value of TAA2CCR1 register) × Count clock cycle

Cycle = (Set value of TAA2CCR0 register + 1) × Count clock cycle

Duty factor = (Set value of TAA2CCR1 register) / (Set value of TAA2CCR0 register + 1)

[Function name]	timeraa_pwm_output_ini	
[Argument]	None	
[Processing content]	Sets the TAA2 operation and interrupts, sets the alternate function of the P00 pin to TOA20 output, and sets alternate function of the P01 pin to TOA21 output.	
[SFRs used]	TAA2CTL0.TAA2CE:	0 (Disables TAA2 operation.)
	PFC0:	0x00 (Sets TOA20 output pin, TOA21 output pin.)
	PFCE0:	0x00 (Sets TOA20 output pin, TOA21 output pin.)
	PMC0:	0x03 (Sets TOA20 output pin, TOA21 output pin.)
	IMR3.TA2CCMK0:	0 (Enables INTTA2CC0 interrupt.)
	IMR3.TA2CCMK1:	0 (Enables INTTA2CC1 interrupt.)
[call function]	timeraa_pwm_output	
[Variable]	None	
[File name]	timeraa_pwm_output\timeraa_5.c	
[Caution]	None	

[Function name]	timeraa_pwm_output	
[Argument]	None	
[Processing content]	Sets TAA2 control register.	
[SFRs used]	TAA2CTL0:	0x04 (Sets count clock to fxx/64.)
	TAA2CTL1:	0x04 (Sets PWM output mode.)
	TAA2IOC0:	0x05 (Sets TOA20 and TOA21 pins' output to high-level start, enables timer output.)
	TAA2IOC2:	0x00 (Sets valid edge of the external event count input signal (TIA20 pin) to no edge detection.)
	TAA2CCR0:	2499 (Compare register of 16-bit counter)
	TAA2CCR1:	1999 (Compare register of 16-bit counter)
[call function]	None	
[Variable]	None	
[File name]	timeraa_pwm_output\timeraa_5.c	
[Caution]	The compare registers are rewritten in the batch write mode. To rewrite the compare register during timer operation, rewrite the TAA2CCR1 register last.	

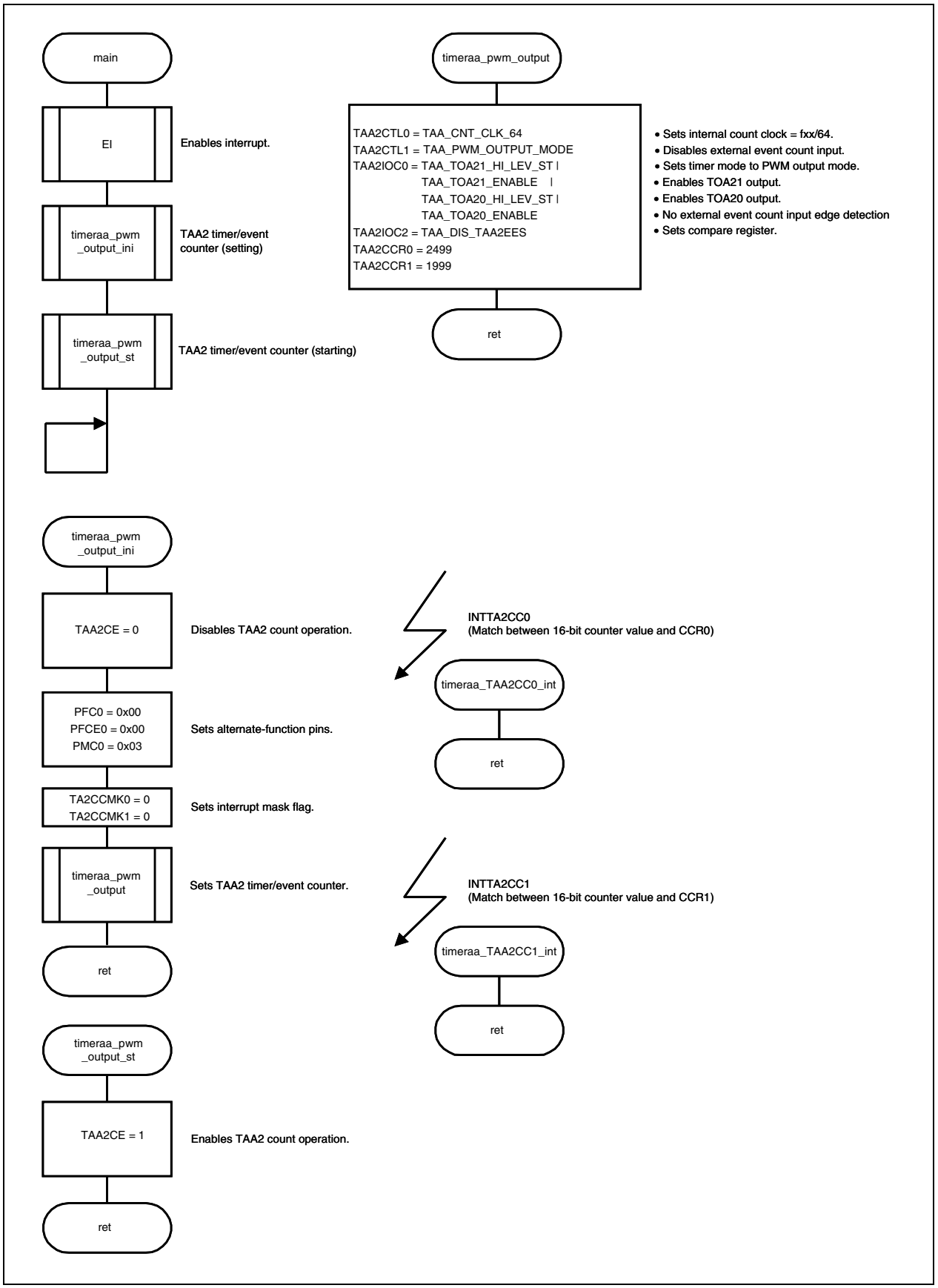
[Function name]	timeraa_pwm_output_st
[Argument]	None
[Processing content]	Starting function of timeraa_pwm_output
[Starting method]	Call this function after calling the timeraa_pwm_output function.
[SFR used]	TAA2CTL0.TAA2CE: 1 (Enables TAA2 operation.)
[call function]	None
[Variable]	None
[File name]	timeraa_pwm_output\timeraa_5.c
[Caution]	None

Interrupt function

[Function name]	timeraa_TAA2CC0_int	
[Overview]	Defined by the user.	
[Source]	INTTA2CC0	Match between the count value of the 16-bit counter and CCR0 buffer register
[call function]	None	
[Variable]	None	
[File name]	timeraa_pwm_output\timeraa_5.c	
[Caution]	None	

[Function name]	timeraa_TAA2CC1_int	
[Overview]	Defined by the user.	
[Source]	INTTA2CC1	Match between the count value of the 16-bit counter and CCR1 buffer register
[call function]	None	
[Variable]	None	
[File name]	timeraa_pwm_output\timeraa_5.c	
[Caution]	None	

Figure 5-1. PWM Output Mode



CHAPTER 6 FREE-RUNNING TIMER MODE

[Function]	Starts operation of the 16-bit counter by setting the TAA2CTL0.TAA2CE bit to 1. Inverts the TOA20 pin output upon a match between the CCR0 buffer register and the count value of the 16-bit counter (compare function). Stores the count value of the 16-bit counter in the TAA2CCR1 register when the valid edge of the capture trigger input (TIA21 pin) is detected (capture function). After counting up to FFFFH, generates an overflow interrupt request signal (INTTA2OV) at the next clock and clears to 0000H to continue counting. The compare function can be implemented with TAA0 to TAA4, and the capture function can be implemented with TAA2 to TAA4.
[Function name]	main
[Argument]	None
[Processing content]	Performs count operation of an fxx/64 count clock, generates an interrupt by inverting the TOA20 pin output upon the count subsequent to the count whose value matches the value of the CCR0 buffer register, and clears the 16-bit counter. Generates an interrupt by capturing the counter value to the TAA2CCR1 register when a valid edge is detected from the TIA21 pin. Generates an INTTA2OV interrupt when a counter overflow is detected. The TOA20 pin starts output at high level.
[SFR used]	None
[call function]	timeraa_free_running_ini, timeraa_free_running_st
[Variable]	None
[Interrupts]	timeraa_TAA2CC0_int timeraa_TAA2CC1_int timeraa_TAA2OV_int
[Interrupt sources]	INTTA2CC0 INTTA2CC1 INTTA2OV
[File name]	timeraa_free_running\MAIN.C
[Caution]	None

[Function name]	timeraa_free_running_ini	
[Argument]	None	
[Processing content]	Sets the TAA2 operation and interrupts, sets the alternate function of the P00 pin to TOA20 output, and sets the alternate function of the P01 pin to TIA21 input.	
[SFRs used]	TAA2CTL0.TAA2CE:	0 (Disables TAA2 operation.)
	PFC0:	0x02 (Sets TOA20 output pin, TIA21 input pin.)
	PFCE0:	0x00 (Sets TOA20 output pin, TIA21 input pin.)
	PMC0:	0x03 (Sets TOA20 output pin, TIA21 input pin.)
	IMR3.TA2CCMK0:	0 (Enables INTTA2CC0 interrupt.)
	IMR3.TA2CCMK1:	0 (Enables INTTA2CC1 interrupt.)
	IMR3.TA2OVMK:	0 (Enables INTTA2OV interrupt.)
[call function]	timeraa_free_running	
[Variable]	None	
[File name]	timeraa_free_running\timeraa_6.c	
[Caution]	None	

[Function name]	timeraa_free_running	
[Argument]	None	
[Processing content]	Sets TAA2 control register.	
[SFRs used]	TAA2CTL0:	0x04 (Sets count clock to fxx/64.)
	TAA2CTL1:	0x05 (Sets free-running timer mode.)
	TAA2IOC0:	0x01 (Sets TOA20 pin output to high-level start, enables timer output.)
	TAA2IOC1:	0x08 (Sets valid edge of the capture trigger input signal (TIA21 pin) to falling edge detection.)
	TAA2IOC2:	0x00 (Sets valid edge of the external event count input signal (TIA20 pin) to no edge detection.)
	TAA2OPT0:	0x20 (Sets TAA2CCR0 as compare register, and TAA2CCR1 as capture register.)
	TAA2CCR0:	2499 (Compare register of 16-bit counter)
[call function]	None	
[Variable]	None	
[File name]	timeraa_free_running\timeraa_6.c	
[Caution]	None	

[Function name]	timeraa_free_running_st	
[Argument]	None	
[Processing content]	Starting function of timeraa_free_running	
[Starting method]	Call this function after calling the timeraa_free_running function.	
[SFR used]	TAA2CTL0.TAA2CE:	1 (Enables TAA2 operation.)
[call function]	None	
[Variable]	None	
[File name]	timeraa_free_running\timeraa_6.c	
[Caution]	None	

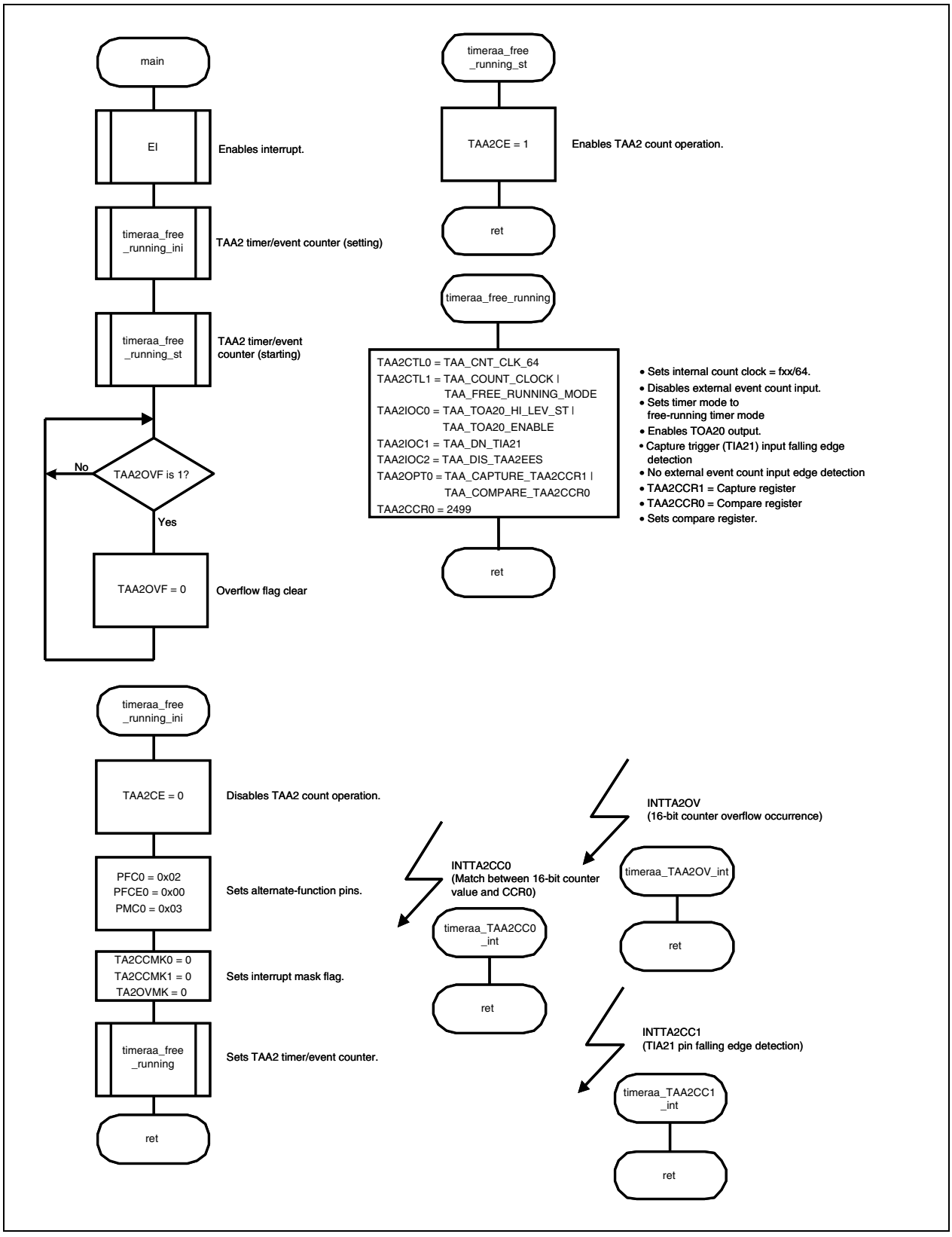
Interrupt function

[Function name]	timeraa_TAA2CC0_int	
[Overview]	Defined by the user.	
[Source]	INTTA2CC0	Match between the count value of the 16-bit counter and CCR0 buffer register
[call function]	None	
[Variable]	None	
[File name]	timeraa_free_running\timeraa_6.c	
[Caution]	None	

[Function name]	timeraa_TAA2CC1_int	
[Overview]	Defined by the user.	
[Source]	INTTA2CC1	TIA21 pin input valid edge detection
[call function]	None	
[Variable]	None	
[File name]	timeraa_free_running\timeraa_6.c	
[Caution]	None	

[Function name]	timeraa_TAA2OV_int	
[Overview]	Defined by the user.	
[Source]	INTTA2OV	16-bit counter overflow occurrence
[call function]	None	
[Variable]	None	
[File name]	timeraa_free_running\timeraa_6.c	
[Caution]	None	

Figure 6-1. Free-Running Timer Mode



CHAPTER 7 PULSE WIDTH MEASUREMENT MODE

[Function]	Starts operation of the 16-bit counter by setting the TAA2CTL0.TAA2CE bit to 1. Stores the count value to the TAA2CCR0 register when the valid edge of the capture trigger input (TIA20 pin) is detected, and clears the 16-bit counter. Measures the valid edge interval of the TIA20 pin by generating an interrupt when the valid edge of the TIA20 pin input is detected and reading the TAA2CCR0 register value. Can be implemented with TAA2 to TAA4.
[Function name]	main
[Argument]	None
[Processing content]	Performs count operation of an fxx/64 count clock, generates an interrupt by storing the count value of the 16-bit counter to the TAA2CCR0 register when the valid edge of the TIA20 pin input is detected, and clears the 16-bit counter. Generates an INTTA2OV interrupt when a counter overflow is detected.
[SFR used]	None
[call function]	timeraa_pulse_measure_ini, timeraa_pulse_measure_st
[Variable]	None
[Interrupts]	timeraa_TAA2CC0_int timeraa_TAA2OV_int
[Interrupt sources]	INTTA2CC0 INTTA2OV
[File name]	timeraa_pulse_measure\MAIN.C
[Caution]	None

The pulse width can be calculated by the following formula.

Pulse width = captured value × Count clock cycle

The pulse width when the 16-bit counter overflow is detected can be calculated by the following formula.

Pulse width = (10000H × number of times the TAA2OVF bit is set to 1 + captured value) × count clock cycle

[Function name]	timeraa_pulse_measure_ini	
[Argument]	None	
[Processing content]	Sets operation and interrupts of TAA2, and sets the alternate function of the P00 pin to TIA20 input.	
[SFRs used]	TAA2CTL0.TAA2CE:	0 (Disables TAA2 operation.)
	PFC0:	0x01 (Sets TIA20 input pin.)
	PFCE0:	0x00 (Sets TIA20 input pin.)
	PMC0:	0x01 (Sets TIA20 input pin.)
	IMR3.TA2CCMK0:	0 (Enables INTTA2CC0 interrupt.)
	IMR3.TA2OVMK:	0 (Enables INTTA2OV interrupt.)
[call function]	timeraa_pulse_measure	
[Variable]	None	
[File name]	timeraa_pulse_measure\timeraa_7.c	
[Caution]	None	

[Function name]	timeraa_pulse_measure	
[Argument]	None	
[Processing content]	Sets TAA2 control register.	
[SFRs used]	TAA2CTL0:	0x04 (Sets count clock to fxx/64.)
	TAA2CTL1:	0x06 (Sets pulse width measurement mode.)
	TAA2IOC1:	0x02 (Sets valid edge of the capture trigger input signal (TIA20 pin) to falling edge detection.)
	TAA2IOC2:	0x00 (Sets valid edge of the external event count input signal (TIA20 pin) to no edge detection.)
	TAA2OPT0:	0x00 (Sets to the initial value.)
[call function]	None	
[Variable]	None	
[File name]	timeraa_pulse_measure\timeraa_7.c	
[Caution]	None	

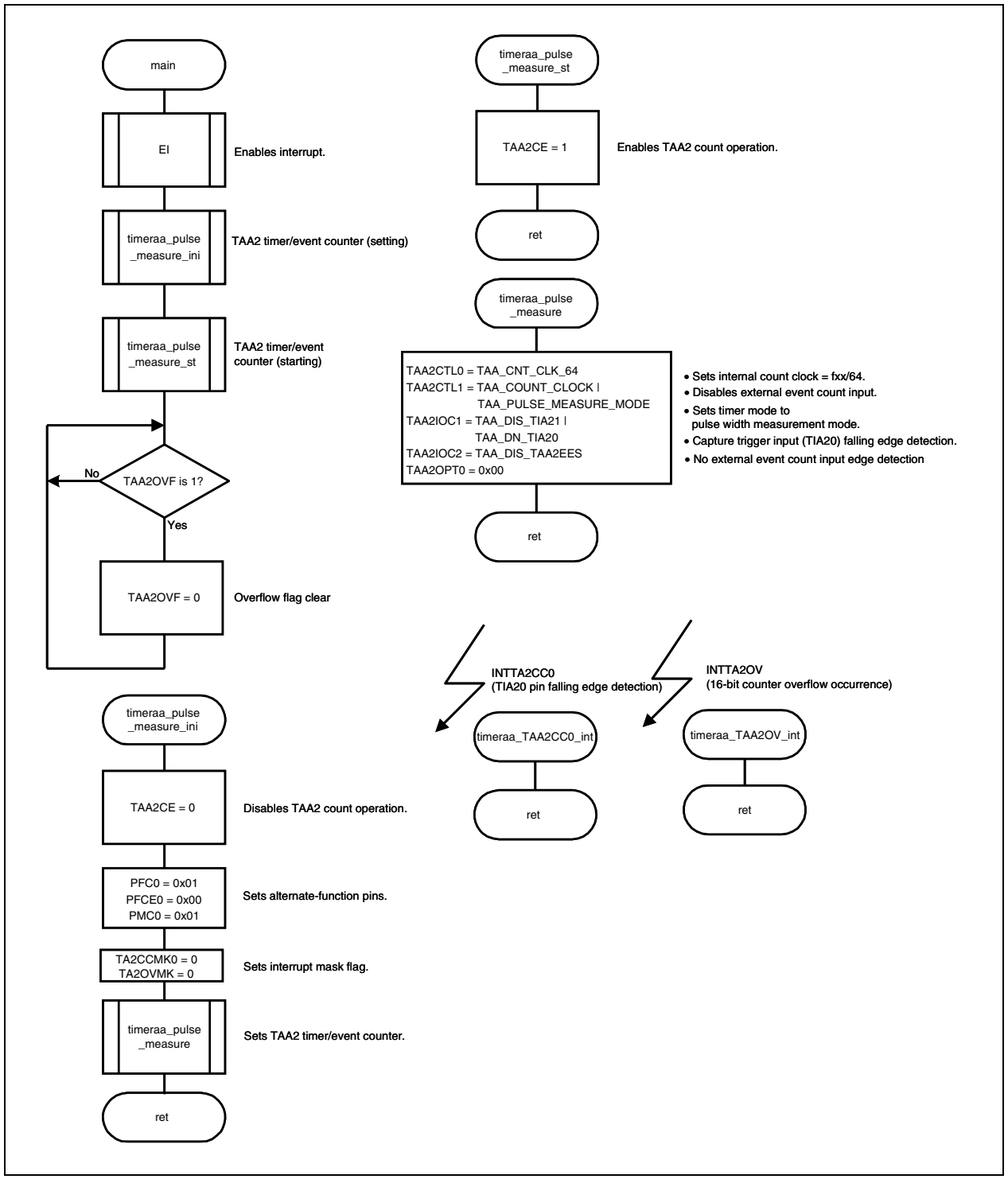
[Function name]	timeraa_pulse_measure_st
[Argument]	None
[Processing content]	Starting function of timeraa_pulse_measure
[Starting method]	Call this function after calling the timeraa_pulse_measure function.
[SFR used]	TAA2CTL0.TAA2CE: 1 (Enables TAA2 operation.)
[call function]	None
[Variable]	None
[File name]	timeraa_pulse_measure\timeraa_7.c
[Caution]	None

Interrupt function

[Function name]	timeraa_TAA2CC0_int	
[Overview]	Defined by the user.	
[Source]	INTTA2CC0	TIA20 pin input valid edge detection
[call function]	None	
[Variable]	None	
[File name]	timeraa_pulse_measure\timeraa_7.c	
[Caution]	None	

[Function name]	timeraa_TAA2OV_int	
[Overview]	Defined by the user.	
[Source]	INTTA2OV	16-bit counter overflow occurrence
[call function]	None	
[Variable]	None	
[File name]	timeraa_pulse_measure\timeraa_7.c	
[Caution]	None	

Figure 7-1. Pulse Width Measurement Mode



For further information,
please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
http://www.eu.necel.com/

Hanover Office
Podbielskistrasse 166 B
30177 Hannover
Tel: 0 511 33 40 2-0

Munich Office
Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

Succursale Française
9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cédex
France
Tel: 01-3067-5800

Sucursal en España
Juan Esplandiu, 15
28007 Madrid, Spain
Tel: 091-504-2787

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands
Steijgerweg 6
5616 HS Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
Tel: 010-8235-1155
http://www.cn.necel.com/

Shanghai Branch
Room 2509-2510, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai, P.R.China P.C:200120
Tel:021-5888-5400
http://www.cn.necel.com/

Shenzhen Branch
Unit 01, 39/F, Excellence Times Square Building,
No. 4068 Yi Tian Road, Futian District, Shenzhen,
P.R.China P.C:518048
Tel:0755-8282-9800
http://www.cn.necel.com/

NEC Electronics Hong Kong Ltd.
Unit 1601-1613, 16/F., Tower 2, Grand Century Place,
193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: 2886-9318
http://www.hk.necel.com/

NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-8175-9600
http://www.tw.necel.com/

NEC Electronics Singapore Pte. Ltd.
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/

NEC Electronics Korea Ltd.
11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul, 135-080, Korea
Tel: 02-558-3737
http://www.kr.necel.com/

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