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April 1\textsuperscript{st}, 2010  
Renesas Electronics Corporation

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Preliminary Application Note

V850E/IF3, V850E/IG3
32-bit Single-Chip Microcontrollers
Sample Programs for A/D Converters 0 and 1

V850E/IF3:
  μPD70F3451
  μPD70F3452
V850E/IG3:
  μPD70F3453
  μPD70F3454
NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN
Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

② HANDLING OF UNUSED INPUT PINS
Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD
A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION
Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE
In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.
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INTRODUCTION

Cautions 1. This Application Note explains a case where the V850E/IG3 is used as a representative microcontroller. Use this Application Note for your reference when using the V850E/IF3.


3. The sample programs are provided for reference purposes only and operations are therefore not subject to guarantee by NEC Electronics Corporation. When using sample programs, customers are advised to sufficiently evaluate this product based on their systems, before use.

4. When using sample programs, reference the following startup routine and link directive file and adjust them if necessary.
   • Startup routine: ig3_start.s
   • Link directive file: ig3_link.dir

Target Readers
This Application Note is intended for users who understand the functions of the V850E/IF3 (μPD70F3451, 70F3452), and V850E/IG3 (μPD70F3453, 70F3454), and who design application systems that use these microcontrollers.

Purpose
This manual is intended to give users an understanding of the basic functions of the V850E/IF3 and V850E/IG3, using the application programs.

How to Use This Manual
It is assumed that the reader of this Application Note has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

   For details of hardware functions (especially register functions, setting methods, etc.) and electrical specifications

   For details of instruction functions
       → See the V850E1 Architecture User’s Manual.

Conventions
   Data significance: Higher digits on the left and lower digits on the right
   Active low representation: xxx (overscore over pin or signal name)
   Memory map address: Higher addresses on the top and lower addresses on the bottom
   Note: Footnote for item marked with Note in the text
   Caution: Information requiring particular attention
   Remark: Supplementary information
   Numeric representation: Binary ... xxxx or xxxxB
      Decimal ... xxxx
      Hexadecimal ... xxxxH
   Prefix indicating the power of 2 (address space, memory capacity):
      K (kilo): \( 2^{10} = 1,024 \)
      M (mega): \( 2^{20} = 1,024^2 \)
      G (giga): \( 2^{30} = 1,024^3 \)
The function lists are structured as follows.

### Theme

<table>
<thead>
<tr>
<th>[Function]</th>
<th>Function description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Function name]</td>
<td>Name of sample function</td>
</tr>
<tr>
<td>[Argument(s)]</td>
<td>Type and overview of argument(s)</td>
</tr>
<tr>
<td>[Processing content]</td>
<td>Processing content of sample function</td>
</tr>
<tr>
<td>[SFR(s) used]</td>
<td>Register name and setting content</td>
</tr>
<tr>
<td>[call function(s)]</td>
<td>Name and function of call function(s)</td>
</tr>
<tr>
<td>[Variable(s)]</td>
<td>Type, name, and overview of variable(s) used in sample function</td>
</tr>
<tr>
<td>[Interrupt(s)]</td>
<td>Name of function</td>
</tr>
<tr>
<td>[Interrupt source(s)]</td>
<td>Name</td>
</tr>
<tr>
<td>[File name]</td>
<td>Name of corresponding sample program file</td>
</tr>
<tr>
<td>[Caution(s)]</td>
<td>Caution(s) upon function usage</td>
</tr>
</tbody>
</table>

### Interrupt function

<table>
<thead>
<tr>
<th>[Function name]</th>
<th>Name of interrupt function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Servicing content]</td>
<td>Servicing content of interrupt function</td>
</tr>
<tr>
<td>[SFR(s) used]</td>
<td>Name of interrupt and conditions for occurrence</td>
</tr>
<tr>
<td>[call function(s)]</td>
<td>None</td>
</tr>
<tr>
<td>[Variable(s)]</td>
<td>Name of variable, function</td>
</tr>
<tr>
<td>[File name]</td>
<td>Name of corresponding sample program file</td>
</tr>
<tr>
<td>[Caution(s)]</td>
<td>None</td>
</tr>
</tbody>
</table>
The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

**Documents related to V850E/IF3 and V850E/IG3**

<table>
<thead>
<tr>
<th>Document Name</th>
<th>Document No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>V850E1 Architecture User's Manual</td>
<td>U14559E</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTA) Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTB) Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (CSIB) Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (I$^3$C) Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for DMA Function Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for Timer M Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for Watchdog Timer Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for Timer AA Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for Timer AB Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for Timer T Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for Port Function Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for Clock Generator Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for Standby Function Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for Interrupt Function Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for A/D Converters 0 and 1 Application Note</td>
<td>This manual</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for A/D Converter 2 Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 Sample Programs for Low-Voltage Detector (LVI) Function Application Note</td>
<td>To be prepared</td>
</tr>
<tr>
<td>V850E/IF3, V850E/IG3 6-Phase PWM Output Control by Timer AB, Timer Q Option, Timer AA, A/D Converters 0 and 1 Application Note</td>
<td>U18717E</td>
</tr>
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# CHAPTER 1 NORMAL OPERATION MODE

## 1.1 A/D Trigger Mode (1 Channel Conversion)

<table>
<thead>
<tr>
<th>[Function]</th>
<th>Performs A/D conversion by setting the A/D conversion operation start timing to A/D trigger mode of the normal operation mode.</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Function name]</td>
<td>ad0_software_main</td>
</tr>
<tr>
<td>[Argument]</td>
<td>None</td>
</tr>
<tr>
<td>[Processing content]</td>
<td>Starts A/D conversion by setting the AD0SCM.AD0CE bit to 1. Stores the A/D conversion results to buf[] by performing A/D conversion to ANI00 pin. An A/D0 conversion end interrupt request signal (INTAD0) occurs upon every completion of A/D conversion. Performs A/D conversion for 10 times.</td>
</tr>
<tr>
<td>[SFR used]</td>
<td>AD0IC: 0x07 (Clears A/D0 conversion end interrupt request signal (INTAD0), releases mask, sets to priority level 7.)</td>
</tr>
<tr>
<td>[call function]</td>
<td>ad_port_set, ad_set, ad_start, ad_stop</td>
</tr>
<tr>
<td>[Variables]</td>
<td>unsigned short int buf[]: Conversion data storing buffer \n volatile unsigned char count: Conversion count variable \n unsigned int wait_co: WAIT variable</td>
</tr>
<tr>
<td>[Interrupt]</td>
<td>ad0_int</td>
</tr>
<tr>
<td>[Interrupt source]</td>
<td>INTAD0</td>
</tr>
<tr>
<td>[File name]</td>
<td>ad01_software_trigger.c</td>
</tr>
<tr>
<td>[Caution]</td>
<td>None</td>
</tr>
</tbody>
</table>
[Function name] ad_set


[SFRs used] AD0OCKS: 0x12 (Sets input clock as fxx/4.)
AD0SCM: 0x0082 (Sets A/D trigger mode.)
AD0CTC: 0x0C (Sets the number of conversion clocks to 32 (2 μs).)
OP0CTL0: 0x10 (Enables operational amplifier 0 operation.)
OP1CTL0: 0x00
CMP0CTL0: 0x00 (Disables comparator 0 operation.)
CMP1CTL0: 0x00

[call function] None

[Variable] unsigned int wait_co: WAIT variable

[File name] ad01_software_trigger.c

[Caution] A stabilization time of 10 μs is required after operation of the operational amplifier is enabled.

[Function name] ad_port_set

[Processing content] Sets analog input pin.

[SFR used] AD0CHEN: 0x0001 (Sets analog input pin to AN100 pin.)

[call function] None

[Variable] None

[File name] ad01_software_trigger.c

[Caution] None

[Function name] ad_start

[Processing content] Start A/D conversion operation.

[SFR used] AD0SCM.AD0CE: 1 (Enables A/D conversion operation.)

[call function] None

[Variable] None

[File name] ad01_software_trigger.c

[Caution] None
### [Function name] ad_stop

**[Processing content]** Stops A/D conversion operation.

**[SFR used]** AD0SCM.AD0CE: 0 (Stops A/D conversion operation.)

**[call function]** None

**[Variable]** None

**[File name]** ad01_software_trigger.c

**[Caution]** None

### Interrupt function

<table>
<thead>
<tr>
<th>[Function name]</th>
<th>ad0_int</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>[Servicing content]</strong></td>
<td>Stores A/D conversion result data to buffer.</td>
</tr>
<tr>
<td><strong>[SFR used]</strong></td>
<td>AD0CR0  A/D0 conversion result register 0</td>
</tr>
<tr>
<td><strong>[call function]</strong></td>
<td>None</td>
</tr>
<tr>
<td><strong>[Variable]</strong></td>
<td>unsigned short int buf [ ]; Convert data storing buffer</td>
</tr>
<tr>
<td></td>
<td>volatile unsigned char count: Convert count variable</td>
</tr>
<tr>
<td><strong>[File name]</strong></td>
<td>ad01_software_trigger.c</td>
</tr>
<tr>
<td><strong>[Caution]</strong></td>
<td>None</td>
</tr>
</tbody>
</table>
Figure 1-1. A/D Trigger Mode (1 Channel Conversion) (1/2)

```
ad0_software_main

DI

count = 0

ad_set

ad_port_set

AD0IC = 0x07

EI

ad_start

count >= RX_SIZE

ad_stop

Disables maskable interrupt request.

Initializes conversion count.

A/D control register setting function

Analog input pin setting function

Clears INTAD0 interrupt request signal, releases mask, sets to priority level 7.

Enables maskable interrupt request.

A/D conversion operation start function

Checks conversion count.

A/D conversion operation stop function
```
Figure 1-1. A/D Trigger Mode (1 Channel Conversion) (2/2)
1.2 A/D Trigger Mode (Multi-Channel Conversion)

- **Function**: Performs A/D conversion by setting the A/D conversion operation start timing to A/D trigger mode of the normal operation mode.

- **Function name**: ad0_software1_main

- **Argument**: None

- **Processing content**: Starts A/D conversion by setting the AD0SCM.AD0CE bit to 1. Stores the A/D conversion results to buf[ ], buf_1[ ], buf_2[ ], and buf_3[ ] which correspond to the analog input pins, by selecting pins in the order of ANI00 pin, ANI01 pin, ANI02 pin, and ANI03 pin which have been specified by the AD0CHEN register, and continuously performing A/D conversion.

  An A/D0 conversion end interrupt request signal (INTAD0) occurs upon completion of conversion operation of the specified analog input pins.

  Performs A/D conversion for 10 times.

- **SFR used**: AD0IC: 0x07 (Clears A/D0 conversion end interrupt request signal (INTAD0), releases mask, sets to priority level 7.)

- **Call function**: ad_port_set, ad_set, ad_start, ad_stop

- **Variables**:
  - unsigned short int buf[ ]: Conversion data storing buffer
  - unsigned short int buf_1[ ]: Conversion data storing buffer
  - unsigned short int buf_2[ ]: Conversion data storing buffer
  - unsigned short int buf_3[ ]: Conversion data storing buffer
  - volatile unsigned char count: Conversion count variable

- **Interrupt**: ad0_int

- **Interrupt source**: INTAD0

- **File name**: ad01_software1_trigger.c

- **Caution**: None
[Function name] ad_set
[SFRs used] AD0OCKS: 0x12 (Sets input clock to fx/4.)
AD0SCM: 0x0082 (Sets A/D trigger mode.)
AD0CTC: 0x0C (Sets the number of conversion clocks to 32 (2 μs).)
OP0CTL0: 0x00 (Enables operational amplifier 0 operation.)
OP1CTL1: 0x00
CMP0CTL0: 0x00 (Disables comparator 0 operation.)
CMP1CTL0: 0x00
[call function] None
[Variable] None
[File name] ad01_software1_trigger.c
[Caution] None

[Function name] ad_port_set
[Processing content] Sets analog input pin.
[SFRs used] AD0CHEN: 0x000F (Sets analog input pin to ANI00 pin, ANI01 pin, ANI02 pin, and ANI03 pin.)
[call function] None
[Variable] None
[File name] ad01_software1_trigger.c
[Caution] None

[Function name] ad_start
[Processing content] Starts A/D convert operation.
[SFR used] AD0SCM.AD0CE: 1 (Enables A/D conversion operation.)
[call function] None
[Variable] None
[File name] ad01_software1_trigger.c
[Caution] None
### Normal Operation Mode

**Function name:** ad_stop

**Processing content:** Stops A/D conversion operation.

**SFR used:**
- AD0SCM.AD0CE: 0 (Stops A/D conversion operation.)

**Call function:** None

**Variable:** None

**File name:** ad01_software1_trigger.c

**Caution:** None

### Interrupt function

**Function name:** ad0_int

**Servicing content:** Stores A/D conversion result data to buffer.

**SFR used:**
- AD0CR0: A/D0 conversion result register 0
- AD0CR1: A/D0 conversion result register 1
- AD0CR2: A/D0 conversion result register 2
- AD0CR3: A/D0 conversion result register 3

**Call function:** None

**Variables:**
- unsigned short int buf [ ]: Conversion data storing buffer
- unsigned short int buf _1[ ]: Conversion data storing buffer
- unsigned short int buf _2[ ]: Conversion data storing buffer
- unsigned short int buf _3[ ]: Conversion data storing buffer
- volatile unsigned char count: Conversion count variable

**File name:** ad01_software1_trigger.c

**Caution:** None
Figure 1-2. A/D Trigger Mode (Multi-Channel Conversion) (1/2)

```
ad0_software1_main

DI

count = 0

ad_set

ad_port_set

AD0IC = 0x07

EI

ad_start

No

count >= RX_SIZE

ad_stop

Yes

Checks conversion count.

A/D conversion operation stop function

A/D control register setting function

Analog input pin setting function

Disables maskable interrupt request.

Initializes conversion count.

Enables maskable interrupt request.

Clears INTAD0 interrupt request signal, releases mask, sets to priority level 7.
Figure 1-2. A/D Trigger Mode (Multi-Channel Conversion) (2/2)

Analog input pin setting function
- `ad_port_set`
  - `AD0CHEN = 0x0001`
  - `ret`

Analog input pin to ANI00

A/D conversion operation start function
- `ad_start`
  - `AD0CE = 1`
  - `ret`

Enables A/D conversion operation.

A/D conversion operation stop function
- `ad_stop`
  - `AD0CE = 0`
  - `ret`

Stops A/D conversion operation.

A/D control register setting function
- `ad_set`
  - `AD0OCKS = 0x12`
  - `WAIT1 μs`
  - `AD0CTC = 0x0C`
  - `OP0CTL0 = 0x00`
  - `OP1CTL0 = 0x00`
  - `CMP0CTL0 = 0x00`
  - `CMP1CTL0 = 0x00`
  - `ret`

Sets operation mode to A/D trigger mode.

Sets input clock to fXX/4.

Waits for 1 μs.

Sets number of conversion clocks to 32 (2 μs).

Disables operational amplifier operation.

Disables comparator operation.

INTAD0 interrupt

INTAD0 interrupt function
- `ad0_int`
  - `buf[count] = AD0CR0`
  - `buf_1[count] = AD0CR1`
  - `buf_2[count] = AD0CR2`
  - `buf_3[count] = AD0CR3`
  - `count++`
  - `reти`

Stores conversion result to buffer.

Stores conversion result to buffer.

Stores conversion result to buffer.

Stores conversion result to buffer.

Increments conversion count.
### 1.3 Hardware Trigger Mode (ITRG1)

<table>
<thead>
<tr>
<th>Function</th>
<th>Performs A/D conversion by setting the A/D conversion operation start timing to hardware trigger mode of the normal operation mode.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function name</td>
<td>ad0_external_main</td>
</tr>
<tr>
<td>Argument</td>
<td>None</td>
</tr>
<tr>
<td>Processing content</td>
<td>Starts A/D conversion when the trigger is input from the ADTRG0 pin. Stores the A/D conversion results to buf[ ], buf_1[ ], buf_2[ ], and buf_3[ ] which correspond to the analog input pins, by selecting pins in the order of ANI00 pin, ANI01 pin, ANI02 pin, and ANI03 pin which have been specified by the AD0CHEN register, and continuously performing A/D conversion. An A/D0 conversion end interrupt request signal (INTAD0) occurs upon completion of conversion operation of the specified analog input pins. Performs A/D conversion for 10 times.</td>
</tr>
<tr>
<td>SFRs used</td>
<td>AD0IC: 0x07 (Clears A/D0 conversion end interrupt request signal (INTAD0), releases mask, sets to priority level 7.)</td>
</tr>
<tr>
<td>Call function</td>
<td>ad_trigger_port_set, ad_port_set, ad_set, ad_start, ad_stop</td>
</tr>
<tr>
<td>Variables</td>
<td><strong>buf[ ]</strong>: Conversion data storing buffer</td>
</tr>
<tr>
<td></td>
<td>volatile unsigned char count: Conversion count variable</td>
</tr>
<tr>
<td>Interrupt</td>
<td>ad0_int</td>
</tr>
<tr>
<td>Interrupt source</td>
<td>INTAD0</td>
</tr>
<tr>
<td>File name</td>
<td>ad01_external_trigger.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
<tr>
<td>Function name</td>
<td>ad_set</td>
</tr>
<tr>
<td>---------------</td>
<td>--------</td>
</tr>
<tr>
<td>Processing content</td>
<td>Sets A/D conversion control register.</td>
</tr>
<tr>
<td>SFRs used</td>
<td>AD0OCKS: 0x12 (Sets input clock to fxx/4.)</td>
</tr>
<tr>
<td></td>
<td>AD0SCM: 0x0182 (Sets hardware trigger mode.)</td>
</tr>
<tr>
<td></td>
<td>ADTR: 0x00 (Sets to falling edge.)</td>
</tr>
<tr>
<td></td>
<td>ADTF: 0x01 (Sets to falling edge.)</td>
</tr>
<tr>
<td></td>
<td>AD0CTC: 0x0C (Sets the number of conversion clocks to 32 (2 (\mu)s).)</td>
</tr>
<tr>
<td></td>
<td>OP0CTL0: 0x00 (Enables operational amplifier 0 operation.)</td>
</tr>
<tr>
<td></td>
<td>OP1CTL0: 0x00</td>
</tr>
<tr>
<td></td>
<td>CMP0CTL0: 0x00 (Disables comparator 0 operation.)</td>
</tr>
<tr>
<td></td>
<td>CMP1CTL0: 0x00</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>ad01_external_trigger.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Function name</th>
<th>ad_trigger_port_set</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processing content</td>
<td>Sets alternate-function pin.</td>
</tr>
<tr>
<td>SFRs used</td>
<td>PFC1: 0x40 (Specifies to ADTRG0 input pin.)</td>
</tr>
<tr>
<td></td>
<td>PFCE1: 0x00 (Specifies to ADTRG0 input pin.)</td>
</tr>
<tr>
<td></td>
<td>PMC1: 0x40 (Specifies to ADTRG0 input pin.)</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>ad01_external_trigger.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Function name</th>
<th>ad_port_set</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processing content</td>
<td>Sets analog input pin.</td>
</tr>
<tr>
<td>SFR used</td>
<td>AD0CHEN: 0x000F (Sets analog input pin to ANI00 pin, ANI01 pin, ANI02 pin, and ANI03 pin.)</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>ad01_external_trigger.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>
CHAPTER 1 NORMAL OPERATION MODE

[Function name] ad_start

[Processing content] Enables A/D conversion operation.

[SFR used] AD0SCM.AD0CE: 1 (Enables A/D conversion operation.)

[call function] None

[Variable] None

[File name] ad01_external_trigger.c

[Caution] None

[Function name] ad_stop

[Processing content] Stops A/D conversion operation.

[SFR used] AD0SCM.AD0CE: 0 (Stop A/D conversion operation.)

[call function] None

[Variable] None

[File name] ad01_external_trigger.c

[Caution] None

Interrupt function

[Function name] ad0_int

[Servicing content] Stores A/D conversion result data to buffer.

[SFRs used] AD0CR0  A/D0 conversion result register 0
AD0CR1  A/D0 conversion result register 1
AD0CR2  A/D0 conversion result register 2
AD0CR3  A/D0 conversion result register 3

[call function] None

[Variables] unsigned short int buf [ ]; Conversion data storing buffer
unsigned short int buf _1[ ]; Conversion data storing buffer
unsigned short int buf _2[ ]; Conversion data storing buffer
unsigned short int buf _3[ ]; Conversion data storing buffer
volatile unsigned char count: Conversion count variable

[File name] ad01_external_trigger.c

[Caution] None
Figure 1-3. Hardware Trigger Mode (ITRG1) (1/2)

ad0_external_main

DI

count = 0

ad_set

ad_trigger_port_set

ad_port_set

ADOIC = 0x07

EI

ad_start

count >= RX_SIZE

No

Yes

ad_stop

Checks conversion count.

A/D conversion operation stop function

Disables maskable interrupt request.

Initializes conversion count.

A/D control register setting function

Alternate-function pin setting function

Analog input pin setting function

Clears INTA0 interrupt request signal, releases mask, sets to priority level 7.

Enables maskable interrupt request.

A/D convert operation enable function
Figure 1-3. Hardware Trigger Mode (ITRG1) (2/2)
1.4  Hardware Trigger Mode (ITRG2 to ITRG4)

<table>
<thead>
<tr>
<th>[Function]</th>
<th>Performs A/D conversion by setting the A/D conversion operation start timing to hardware trigger mode of the normal operation mode.</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Function name]</td>
<td>ad0_timer_main</td>
</tr>
<tr>
<td>[Argument]</td>
<td>None</td>
</tr>
<tr>
<td>[Processing content]</td>
<td>Starts A/D conversion when the A/D conversion start trigger signal of a timer (motor control function) is input. Stores the A/D conversion results to buf[] by performing A/D conversion of ANI00 pin. An A/D0 conversion end interrupt request signal (INTAD0) occurs upon every completion of A/D conversion. Performs A/D conversion for 10 times.</td>
</tr>
<tr>
<td>[SFR used]</td>
<td>AD0IC: 0x07 (Clears A/D0 conversion end interrupt request signal (INTAD0), releases mask, sets to priority level 7.)</td>
</tr>
<tr>
<td>[call function]</td>
<td>ad_port_set, ad_set, ad_start, ad_timer_trigger, ad_stop</td>
</tr>
<tr>
<td>[Variables]</td>
<td>unsigned short int buf[]: Conversion data storing buffer volatile unsigned char count: Conversion count variable unsigned int wait_co: WAIT variable</td>
</tr>
<tr>
<td>[Interrupt]</td>
<td>ad01_int</td>
</tr>
<tr>
<td>[Interrupt source]</td>
<td>INTAD0</td>
</tr>
<tr>
<td>[File name]</td>
<td>ad01_timer_trigger.c</td>
</tr>
<tr>
<td>[Caution]</td>
<td>None</td>
</tr>
</tbody>
</table>
### CHAPTER 1 NORMAL OPERATION MODE

<table>
<thead>
<tr>
<th>Function name</th>
<th>ad_set</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processing content</td>
<td>Sets A/D conversion control register.</td>
</tr>
<tr>
<td>SFRs used</td>
<td>AD0OCKS: 0x12 (Sets input clock to fXX/4.)</td>
</tr>
<tr>
<td></td>
<td>AD0SCM: 0x0182 (Sets hardware trigger mode.)</td>
</tr>
<tr>
<td></td>
<td>AD0CTC: 0x0C (Sets the number of conversion clocks to 32 (2 μs).)</td>
</tr>
<tr>
<td></td>
<td>OP0CTL0: 0x10 (Enables operational amplifier 0 operation.)</td>
</tr>
<tr>
<td></td>
<td>OP1CTL0: 0x00</td>
</tr>
<tr>
<td></td>
<td>CMP0CTL0: 0x10 (Enables comparator 0 (full-range) operation)</td>
</tr>
<tr>
<td></td>
<td>CMP1CTL0: 0x00</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>unsigned int wait_co: WAIT variable</td>
</tr>
<tr>
<td>File name</td>
<td>ad01_timer_trigger.c</td>
</tr>
<tr>
<td>Caution</td>
<td>A stabilization time of 10 μs is required after operation of the operational amplifier or comparator is enabled.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Function name</th>
<th>ad_port_set</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processing content</td>
<td>Sets analog input pin.</td>
</tr>
<tr>
<td>SFR used</td>
<td>AD0CHEN: 0x0001 (Sets analog input pin to ANI00 pin.)</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>ad01_timer_trigger.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Function name</th>
<th>ad_start</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processing content</td>
<td>Enables A/D conversion operation.</td>
</tr>
<tr>
<td>SFR used</td>
<td>AD0SCM.AD0CE: 1 (Enables A/D conversion operation.)</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>ad01_timer_trigger.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>
### CHAPTER 1 NORMAL OPERATION MODE

<table>
<thead>
<tr>
<th>Function name</th>
<th>ad_timer_trigger</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processing content</td>
<td>Sets the timer trigger of the A/D conversion.</td>
</tr>
<tr>
<td>SFRs used</td>
<td>TAA0CTL0.TAA0CE: 1 (Starts TAA0 operation.)</td>
</tr>
<tr>
<td></td>
<td>TAB0CTL0.TAB0CE: 1 (Starts TAB0 operation.)</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>ad01_timer_trigger.c</td>
</tr>
<tr>
<td>Caution</td>
<td>Omitted due to the same settings as the int_taa_init, int_tab_init, int_tmq_op_init functions in interrupt.c. For details of interrupt.c, refer to V850E/IF3, V850E/IG3 Sample Programs for Interrupt Function Application Note (U18736E).</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Function name</th>
<th>ad_stop</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processing content</td>
<td>Stops A/D convert operation.</td>
</tr>
<tr>
<td>SFR used</td>
<td>AD0SCM.AD0CE: 0 (Stops A/D conversion operation.)</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>ad01_timer_trigger.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>

**Interrupt function**

<table>
<thead>
<tr>
<th>Function name</th>
<th>ad0_int</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processing content</td>
<td>Stores A/D conversion result data to buffer.</td>
</tr>
<tr>
<td>SFR used</td>
<td>AD0CR0 A/D0 conversion result register 0</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variables</td>
<td>unsigned short int buf [ ]: Conversion data storing buffer</td>
</tr>
<tr>
<td></td>
<td>volatile unsigned char count: Conversion count variable</td>
</tr>
<tr>
<td>File name</td>
<td>ad01_timer_trigger.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>
Figure 1-4. Hardware Trigger Mode (ITRG2 to ITRG4) (1/3)

```
ad0_timer_main

DI

count = 0

ad_set

A/D control register setting function

ad_port_set

Analog input pin setting function

AD0IC = 0x07

Enables maskable interrupt request.

EI

A/D conversion operation enable function

ad_start

A/D conversion operation stop function

ad_timer_trigger

Timer trigger setting function of A/D conversion

count>=RX_SIZE

Checks conversion count.

No

Yes

ad_stop

Disables maskable interrupt request.

Initializes conversion count.

Cleans INTAD0 interrupt request signal, releases mask, sets to priority level 7.
CHAPTER 1 NORMAL OPERATION MODE

Figure 1-4. Hardware Trigger Mode (ITRG2 to ITRG4) (2/3)

Analog input pin setting function

Ad_port_set

AD0CHEN = 0x0001

Sets analog input pin to ANI00 + operational amp.

Ret

A/D conversion operation enable function

Ad_start

AD0CE = 1

Enables A/D conversion operation.

Ret

A/D conversion operation stop function

Ad_stop

AD0CE = 0

Stops A/D conversion operation.

Ret

A/D control register setting function

Ad_set

AD0OCKS = 0x212

Sets clock to fxx/4.

AD0SCM = 0x0182

Sets operation mode to hardware trigger mode.

WAIT1 μs

Waits for 1 μs.

AD0CTC = 0x0C

Sets the number of conversion clocks to 32 (2 μs).

OP0CTL0 = 0x10

OP1CTL0 = 0x00

Sets operational amplifier to enable operational amplifier 0 operation.

CMP0CTL0 = 0x10

CMP1CTL0 = 0x00

Enables comparator 0 (full-range) operation.

WAIT 10 μs

Waits for 10 μs.

INTAD0 interrupt function

Ad0_int

buf[count] = AD0CR0

Stores conversion result to buffer.

Count++

Increment conversion count.

Ret
Figure 1-4. Hardware Trigger Mode (ITRG2 to ITRG4) (3/3)

Timer trigger setting function of A/D conversion

ad_timer_trigger

Refer to Interrupt.c.

TAA0CE = 1

Enables TAA0 operation.

TAB0CE = 1

Enables TAB0 operation.

ret

Note For details of interrupt.c, refer to V850E/IF3, V850E/IG3 Sample Programs for Interrupt Function Application Note (U18736E).
CHAPTER 2 EXTENDED OPERATION MODE

2.1 Conversion Channel Specification Mode

| [Function] | Performs A/D conversion by setting the A/D conversion operation start timing to conversion channel specification mode of the extended operation mode. |
| [Function name] | ad0_change_channel_main |
| [Argument] | None |
| [Processing content] | Starts the A/D conversion when the ITRG1 signal is generated by setting the AD0CE bit to 1 and entering into the trigger wait status. Performs the A/D conversion of AN101 pin for four times and stores the A/D conversion results to buf[ ], buf_1[ ], buf_2[ ], and buf_3[ ]. An A/D0 conversion end interrupt request signal (INTAD0) occurs upon every completion of A/D conversion. Performs A/D conversion for 10 times. |
| [SFR used] | AD0IC: 0x07 (Clears A/D0 conversion end interrupt request signal (INTAD0), releases mask, sets to priority level 7.) |
| [call function] | ad_port_set, ad_set, ad_start, ad_stop |
| [Variables] | unsigned short int buf[ ]: Conversion data storing buffer |
| | unsigned short int buf_1[ ]: Conversion data storing buffer |
| | unsigned short int buf_2[ ]: Conversion data storing buffer |
| | unsigned short int buf_3[ ]: Conversion data storing buffer |
| | volatile unsigned char count: Conversion count variable |
| [Interrupt] | ad0_int |
| [Interrupt source] | INTAD0 |
| [File name] | ad01_change_channel.c |
| [Caution] | None |
### Function: ad_set

**Processing content:** Sets A/D conversion control register.

**SFRs used:**
- **AD0OCKS:** 0x12 (Sets input clock to fXX/4.)
- **AD0SCM:** 0x0182 (Sets hardware trigger mode.)
- **AD0TSEL:** 0x00 (Specifies ITRG1 as trigger.)
- **AD0CTC:** 0x02 (Sets to conversion channel specification mode.)
- **OP0CTL0:** 0x0C (Sets the number of conversion clocks to 32 (2 μs).)
- **OP0CTL0:** 0x00 (Disables operational amplifier 0 operation.)
- **OP1CTL0:** 0x00
- **CMP0CTL0:** 0x00 (Disables comparator 0 operation.)
- **CMP1CTL0:** 0x00

**Call function:** None

**Variable:** None

**File name:** ad01_change_channel.c

**Caution:** None

### Function: ad_port_set

**Processing content:** Sets analog input pin.

**SFRs used:**
- **AD0CHEN:** 0x000F (Sets the number of conversions to 4 times.)
- **AD0CH1:** 0x11 (Sets analog input pin to ANI01 pin.)

**Call function:** None

**Variable:** None

**File name:** ad01_change_channel.c

**Caution:** None

### Function: ad_start

**Processing content:** Enables A/D conversion operation.

**SFR used:**
- **AD0SCM.AD0CE:** 1 ( Enables A/D conversion operation.)

**Call function:** None

**Variable:** None

**File name:** ad01_change_channel.c

**Caution:** None
### CHAPTER 2 EXTENDED OPERATION MODE

<table>
<thead>
<tr>
<th>Function name</th>
<th>ad_stop</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processing content</td>
<td>Stops A/D conversion operation.</td>
</tr>
<tr>
<td>SFR used</td>
<td>AD0SCM.AD0CE: 0 (Stops A/D conversion operation.)</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>ad01_change_channel.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>

#### Interrupt function

<table>
<thead>
<tr>
<th>Function name</th>
<th>ad0_int</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processing content</td>
<td>Stores A/D conversion result data to buffer.</td>
</tr>
</tbody>
</table>
| SFRs used          | AD0CR0: A/D0 conversion result register 0
|                    | AD0CR1: A/D0 conversion result register 1
|                    | AD0CR2: A/D0 conversion result register 2
|                    | AD0CR3: A/D0 conversion result register 3 |
| call function      | None                    |
| Variables          | unsigned short int buf [:] Conversion data storing buffer
|                    | unsigned short int buf _1[ ]: Conversion data storing buffer
|                    | unsigned short int buf _2[ ]: Conversion data storing buffer
|                    | unsigned short int buf _3[ ]: Conversion data storing buffer
|                    | volatile unsigned char count: Conversion count variable |
| File name          | ad01_change_channel.c    |
| Caution            | None                    |
Preliminary Application Note U18737EJ1V0AN

Figure 2-1. Conversion Channel Specification Mode (1/2)

- **ad0_change**
  - DI: Disables maskable interrupt request.
  - count = 0: Initializes conversion count.
- **ad_set**
  - A/D control register setting function
- **ad_port_set**
  - Analog input pin setting function
- **AD0IC = 0x07**
  - Clears INTAD0 interrupt request signal, releases mask, sets to priority level 7.
- **EI**
  - Enables maskable interrupt request.
- **ad_start**
  - A/D conversion operation enable function
- **count >= RX_SIZE**
  - Checks conversion count.
  - Yes: A/D conversion operation stop function
  - No: ad_change
- **ad_stop**
  - A/D conversion operation stop function
Figure 2-1. Conversion Channel Specification Mode (2/2)

```
Analog input pin setting function
  ad_port_set

AD0CHEN = 0x000F
AD0CH1 = 0x11

ret

A/D control register setting function
  ad_set

AD0OCKS = 0x12
AD0SCM = 0x0182

WAIT1 μs

AD0TSEL = 0x00
AD0CTL0 = 0x00
AD0CTC = 0x0C

OP0CTL0 = 0x00
OP1CTL0 = 0x00

CMP0CTL0 = 0x00
CMP1CTL0 = 0x00

ret

A/D conversion operation enable function
  ad_start

AD0CE = 1

ret

INTAD0 interrupt function
  ad0_int

buf[count] = AD0CR0

buf_1[count] = AD0CR1

buf_2[count] = AD0CR2

buf_3[count] = AD0CR3

count++

ret

A/D conversion operation stop function
  ad_stop

AD0CE = 0

ret
```

Sets conversion count to 4 times.
Sets analog input pin to AN01.

Sets input clock to fXX/4.

Sets operation mode to hardware trigger mode.

Waits for 1 μs.

Specifies trigger to ITRG1.
Specifies conversion channel specification mode.

Sets the number of conversion clocks to 32 (2 μs).

Disables operational amplifier operation.

Disables comparator operation.

Stops A/D conversion operation.

Enables A/D conversion operation

INTAD0 interrupt

Stores conversion result to buffer.

Stores conversion result to buffer.

Stores conversion result to buffer.

Increments conversion count.
### 2.2 Extension Buffer Mode

**[Function]** Performs A/D conversion by setting the A/D conversion operation start timing to extension buffer mode of the extended operation mode.

**[Function name]** ad0_extension_buffer_main

**[Argument]** None

**[Processing content]**
- Starts A/D conversion when the ITRG1 and ITRG2 signals are generated by setting the AD0CE bit to 1 and entering into the trigger wait status.
- Performs the A/D conversion every time the ITRG1 signal occurs, by switching the analog input pins in the order of ANI05 pin and ANI00 pin, and stores the A/D conversion results to the A/D0 conversion result extension buffer registers 0 to 2.
- Generates an A/D0 conversion end interrupt request signal (INTAD0) upon every completion of A/D conversion.
- Stores the values of the A/D0 conversion result extension buffer registers 0 to 2 to buf[ ] when the LDTRG1 signal is generated.
- Performs the A/D conversion every time the ITRG2 signal occurs, by switching the analog input pins in the order of ANI03 pin and ANI02 pin, and stores the A/D conversion results to the A/D0 conversion result extension buffer registers 3 and 4.
- Generates an A/D0 conversion end interrupt request signal (INTAD0) occurs upon every completion of A/D conversion. Stores the values of the A/D0 conversion result extension buffer registers 3 and 4 to buf[ ] when the LDTRG2 signal occurs. Performs A/D conversion once.

**[SFRs used]**
- AD0IC: 0x07 (Clears A/D0 conversion end interrupt request signal (INTAD0), releases mask, sets to priority level 7.)
- TB0OVIC: 0x07 (Clears TAB0 overflow interrupt request signal (INTTB0OV), releases mask, sets to priority level 7.)
- TB0CCIC0: 0x07 (Clears TAB0 capture interrupt request signal, releases mask, sets to priority level 7.)

**[call function]** ad_port_set, ad_set, ad_start, ad_stop

**[Variable]**
- unsigned short int buf[ ]: Conversion data storing buffer

**[Interrupt]**
- ad0_int, ad0_int_tabcc0, ad0_int_tab0ov

**[Interrupt source]**
- INTAD0, INTTB0CC0, INTTB0OV

**[File name]** ad01_extension_buffer.c

**[Caution]** None
[Function name] ad_set


[SFRs used] 
- AD0OCKS: 0x12 (Sets input clock to fxx/4.)
- AD0SCM: 0x0182 (Sets hardware trigger mode.)
- AD0TSEL: 0x90 (Sets selection trigger 1 to ITRG1, selection load trigger 1 to LDTRG1, selection trigger 2 to ITRG2, and selection load trigger 2 to LDTRG2.
- AD0CTL0: 0x03 (Sets extension buffer mode.)
- AD0CTC: 0x0C (Sets the number of conversion clocks to 32 (2 μs).)
- ADLTS1: 0x00 (Specifies TABTIOV0 as input signal to LDTRG1.)
- ADLTS2: 0x00 (Specifies TABTICC0 as input signal to LDTRG2.)
- OP0CTL0: 0x00 (Disables operational amplifier 0 operation.)
- OP1CTL0: 0x00
- CMP0CTL0: 0x00 (Disables comparator 0 operation.)
- CMP1CTL0: 0x00

[call function] None

[Variable] None

[File name] ad01_extension_buffer.c

[Caution] None

---

[Function name] ad_port_set

[Processing content] Sets analog input pin.

[SFRs used] 
- AD0CHEN: 0x0001
- AD0CH1: 0x05 (Sets analog input pin corresponding to selection trigger 1 to ANI05 pin and ANI00 pin.)
- AD0CH2: 0x23 (Sets analog input pin corresponding to selection trigger 2 to ANI03 pin and ANI02 pin.)

[call function] None

[Variable] None

[File name] ad01_extension_buffer.c

[Caution] None
Function name: ad_start

Processing content: Enables A/D conversion operation.

SFR used: AD0SCM.AD0CE: 1 (Enables A/D conversion operation.)

call function: None

Variable: None

File name: ad01_extension_buffer.c

Caution: None

Function name: ad_stop

Processing content: Stops A/D conversion operation.

SFR used: AD0SCM.AD0CE: 0 (Stops A/D conversion operation.)

call function: None

Variable: None

File name: ad01_extension_buffer.c

Caution: None

Interrupt function

Function name: ad0_int

Processing content: None

SFR used: None

call function: None

Variable: None

File name: ad01_extension_buffer.c

Caution: None
### [Function] ad0_int_tab0ov

**[Processing content]** Stores A/D conversion result data to buffer.

**[SFRs used]**
- AD0ECR0: A/D0 conversion result extension register 0
- AD0ECR1: A/D0 conversion result extension register 1
- AD0ECR2: A/D0 conversion result extension register 2

**[call function]** None

**[Variable]**
- unsigned short int buf [ ]: Conversion data storing buffer

**[File name]** ad01_extension_buffer.c

**[Caution]** None

---

### [Function] ad0_int_tabcc0

**[Processing content]** Stores A/D conversion result data to buffer.

**[SFRs used]**
- AD0ECR3: A/D0 conversion result extension register 3
- AD0ECR4: A/D0 conversion result extension register 4

**[call function]** ad_stop

**[Variable]**
- unsigned short int buf [ ]: Conversion data storing buffer

**[File name]** ad01_extension_buffer.c

**[Caution]** None
Figure 2-2. Extension Buffer Mode (1/3)

- **DI**
  - Disables maskable interrupt request.

- **ad_port_set**
  - Analog input pin setting function

- **AD0IC = 0x07**
  - Clears INTAD0 interrupt request signal, releases mask, sets to priority level 7.

- **TB0OVIC = 0x07**
  - Clears INTTB0OV interrupt request signal, releases mask, sets to priority level 7.

- **TB0CCIC0 = 0x07**
  - Clears INTTB0CC0 interrupt request signal, releases mask, sets to priority level 7.

- **EI**
  - Enables maskable interrupt request.

- **ad_start**
  - A/D conversion operation enable function
Analog input pin setting function

```plaintext
ad_port_set

AD0CHEN = 0x0001
AD0CH1 = 0x05
AD0CH2 = 0x23

ret
```

A/D control register setting function

```plaintext
ad_set

AD0OCKS = 0x12
AD0SCM = 0x0182

WAIT1 μs

ADTSEL = 0x90

ADCTLO = 0x03

AD0CTC = 0x0C

ADLTS1 = 0x00

ADLTS2 = 0x00

OP0CTL0 = 0x00
OP1CTL0 = 0x00

CMP0CTL0 = 0x00
CMP1CTL0 = 0x00

ret
```

A/D conversion operation enable function

```plaintext
ad_start

AD0CE = 1

ret
```

A/D conversion operation stop function

```plaintext
ad_stop

AD0CE = 0

ret
```

Sets selection trigger 1 to ANI00, ANI05.
Sets selection trigger 2 to ANI02, ANI03.
Sets input clock to fx0/4.
Sets operation mode to hardware trigger mode.
Waits for 1 μs.
Specifies selection trigger.
Specifies extension buffer mode.
Sets the number of conversion clocks to 32 (2 μs).
Specifies input signal to selection load trigger 1.
Specifies input signal to selection load trigger 2.
Disables operational amplifier operation.
Disables comparator operation.

Sets selection trigger 2 to ANI02, ANI03.
Sets input clock to fXX/4.
Waits for 1 μs.
Figure 2-2. Extension Buffer Mode (3/3)

INTAD0 interrupt

ad0_int

reti

INTTB0CC0 interrupt

ad0_int_tabcc0

buf[3] = AD0ECR3

buf[4] = AD0ECR4

ad_stop

reti

INTTB0CV interrupt

ad0_int_tab0ov

buf[0] = AD0ECR0

buf[1] = AD0ECR1

buf[2] = AD0ECR2

ad_stop

A/D conversion stop function

Stores conversion result to buffer.

Stores conversion result to buffer.

Stores conversion result to buffer.

Stores conversion result to buffer.
For further information, please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
http://www.necel.com/

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
http://www.am.necel.com/

[Europe]
NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
http://www.eu.necel.com/

Hanover Office
Podbielkistrasse 166 B
30177 Hannover
Tel: 0 511 33 40 2-0

Munich Office
Werner-Eckert-Straße 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

Succursale Française
9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cédex
France
Tel: 01-3067-5800

Sucursal en España
Juan Espandiari, 15
28007 Madrid, Spain
Tel: 091-504-2787

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands
Steijgerweg 6
5616 HS Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]
NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
Tel: 010-8235-1155
http://www.cn.necel.com/

Shanghai Branch
Room 2509-2510, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai, P.R.China P.C:200120
Tel:021-5888-5400
http://www.cn.necel.com/

Shenzhen Branch
Unit 01, 39/F, Excellence Times Square Building,
No. 4068 Yi Tian Road, Futian District, Shenzhen,
P.R.China P.C:518048
Tel:0755-8282-9800
http://www.cn.necel.com/

NEC Electronics Hong Kong Ltd.
Unit 1601-1613, 16/F., Tower 2, Grand Century Place,
193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: 2886-9318
http://www.hk.necel.com/

NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-8175-9600
http://www.tw.necel.com/

NEC Electronics Singapore Pte. Ltd.
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/

NEC Electronics Korea Ltd.
11F., Samik Lavied’or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul. 135-080, Korea
Tel: 02-558-3737
http://www.kr.necel.com/

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