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Application Note

V850E/IF3, V850E/IG3
32-Bit Single-Chip Microcontrollers

Flash Memory Programming (Programmer)

μPD70F3451
μPD70F3452
μPD70F3453
μPD70F3454
NOTES FOR CMOS DEVICES

1. **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between \( V_{IL} \) (MAX) and \( V_{IH} \) (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between \( V_{IL} \) (MAX) and \( V_{IH} \) (MIN).

2. **HANDLING OF UNUSED INPUT PINS**
   Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to \( V_{DD} \) or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

3. **PRECAUTION AGAINST ESD**
   A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

4. **STATUS BEFORE INITIALIZATION**
   Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

5. **POWER ON/OFF SEQUENCE**
   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

6. **INPUT OF SIGNAL DURING POWER OFF STATE**
   Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.
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INTRODUCTION

Target Readers  This application note is intended for users who understand the functions of the V850E/IF3, V850E/IG3 and who will use this product to design application systems.

Purpose  The purpose of this application note is to help users understand how to develop dedicated flash memory programmers for rewriting the internal flash memory of the V850E/IF3, V850E/IG3.
The sample programs and circuit diagrams shown in this document are for reference only and are not intended for use in actual design-ins. Therefore, these sample programs must be used at the user’s own risk. Correct operation is not guaranteed if these sample programs are used.

Organization  This manual consists of the following main sections.

• Flash memory programming
• Programmer operating environment
• Basic programmer operation
• Command/data frame format
• Description of command processing
• UART communication mode
• 3-wire serial I/O communication mode with handshake supported (CSI + HS)
• 3-wire serial I/O communication mode (CSI)
• Flash memory programming parameter characteristics

How to Read This Manual  It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.
This Application Note explains a case where the V850E/IG3 is used as a representative microcontroller. When you use this document as a manual for V850E/IF3, replace V850E/IG3 with V850E/IF3.

☐ To gain a general understanding of functions:
→ Read this manual in the order of the CONTENTS. The mark “<R>” shows major revised points. The revised points can be easily searched by copying an “<R>” in the PDF file and specifying it in the “Find what:” field.
☐ To learn more about the hardware functions of V850E/IF3 or V850E/IG3:

Conventions

Data significance: Higher digits on the left and lower digits on the right
Active low representation: XXX (overscore over pin or signal name)
Note: Footnote for item marked with Note in the text
Caution: Information requiring particular attention
Remark: Supplementary information
Numeral representation: Binary....................xxxx or xxxxB
Decimal....................xxxx
Hexadecimal .........xxxxH
Related Documents  The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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CHAPTER 1 FLASH MEMORY PROGRAMMING

To rewrite the contents of the internal flash memory of the V850E/IG3, a dedicated flash memory programmer (hereafter referred to as the “programmer”) is usually used.

This Application Note explains how to develop a dedicated programmer.

1.1 Overview

The V850E/IG3 incorporates firmware that controls flash memory programming. The programming to the internal flash memory is performed by transmitting/receiving commands between the programmer and the V850E/IG3 via serial communication.

Figure 1-1. System Outline of Flash Memory Programming in V850E/IG3
1.2 System Configuration

Examples of the system configuration for programming the flash memory are illustrated in Figure 1-2.

These figures illustrate how to program the flash memory with the programmer, under control of a host machine.

Depending on how the programmer is connected, the programmer can be used in a standalone mode without using the host machine, if a user program has been downloaded to the programmer in advance.

For example, NEC Electronics’ flash memory programmer PG-FP4 can execute programming either by using the GUI software with a host machine connected or by itself (standalone).

Figure 1-2. System Configuration Examples

(1) UART communication mode (LSB-first transfer)

(2) 3-wire serial I/O communication mode with handshake supported (CSI + HS) (MSB-first transfer)

(3) 3-wire serial I/O communication mode (CSI) (MSB-first transfer)
1.3 Programming Overview

To rewrite the contents of the flash memory with the programmer, the V850E/IG3 must first be set to the flash memory programming mode. After that, select the mode for communication between the programmer and the V850E/IG3, transmit commands from the programmer via serial communication, and then rewrite the flash memory. The flowchart of programming is illustrated in Figure 1-3.

**Figure 1-3. Programming Flowchart**

1.3.1 Setting flash memory programming mode

Supply a specific voltage to the flash memory programming mode setting pins (FLMD0 and FLMD1) in the V850E/IG3 and release a reset; the flash memory programming mode is then set.

1.3.2 Selecting serial communication mode

To select a serial communication mode, generate pulses by changing the voltage at flash memory programming mode setting pin (FLMD0) between the VDD voltage and GND voltage in the flash memory programming mode, and determine the communication mode according to the pulse count.
1.3.3 Manipulating flash memory via command transmission/reception

The flash memory incorporated in the V850E/IG3 has functions to rewrite the flash memory contents. The flash memory manipulating functions shown in Table 1-1 are available.

<table>
<thead>
<tr>
<th>Function</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>Erase</td>
<td>Erases the flash memory contents.</td>
</tr>
<tr>
<td>Write</td>
<td>Writes data to the flash memory.</td>
</tr>
<tr>
<td>Verify</td>
<td>Compares the flash memory contents with data for verify.</td>
</tr>
<tr>
<td>Acquisition of information</td>
<td>Reads information related to the flash memory.</td>
</tr>
</tbody>
</table>

Table 1-1. Outline of Flash Memory Functions

To control these functions, the programmer transmits commands to the V850E/IG3 via serial communication. The V850E/IG3 returns the response status for the commands. The programming to the flash memory is performed by repeating these series of serial communications.

1.4 Information Specific to V850E/IF3 and V850E/IG3

The V850E/IF3 and V850E/IG3 must manage product-specific information (such as a device name and memory information).

Table 1-2 shows the flash memory size of the V850E/IF3 and V850E/IG3. And Figure 1-4 shows the configuration of the flash memory.

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>V850E/IF3</td>
<td>128 KB</td>
</tr>
<tr>
<td>PD70F3451</td>
<td></td>
</tr>
<tr>
<td>PD70F3452</td>
<td>256 KB</td>
</tr>
<tr>
<td>V850E/IG3</td>
<td>128 KB</td>
</tr>
<tr>
<td>PD70F3453</td>
<td></td>
</tr>
<tr>
<td>PD70F3454</td>
<td>256 KB</td>
</tr>
</tbody>
</table>

Table 1-2. Flash Memory Size of V850E/IF3 and V850E/IG3
Figure 1-4. Flash Memory Configuration

Remark   Each block consists of 2 KB (this figure only illustrates some parts of entire blocks in the flash memory).
CHAPTER 2 PROGRAMMER OPERATING ENVIRONMENT

2.1 Programmer Control Pins

Table 2-1 lists the pins that the programmer must control to implement the programmer function in the user system. See the following pages for details on each pin.

Table 2-1. Pin Description

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>I/O</th>
<th>Pin Function</th>
<th>Pin Name</th>
<th>CSi</th>
<th>CSi + HS</th>
<th>UART</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLMD0</td>
<td>Output</td>
<td>Output of signal level to set programming mode and output of pulse to select communication mode</td>
<td>FLMD0</td>
<td>O</td>
<td>O</td>
<td>O</td>
</tr>
<tr>
<td>FLMD1</td>
<td>Output</td>
<td>Output of signal level to set programming mode</td>
<td>FLMD1</td>
<td>O</td>
<td>O</td>
<td>O</td>
</tr>
<tr>
<td>VDD</td>
<td>Output</td>
<td>VDD voltage generation/monitoring</td>
<td>Note1</td>
<td>△</td>
<td>△</td>
<td>△</td>
</tr>
<tr>
<td>GND</td>
<td>–</td>
<td>Ground</td>
<td>Note2</td>
<td>O</td>
<td>O</td>
<td>O</td>
</tr>
<tr>
<td>CLK</td>
<td>Output</td>
<td>Operating clock output to V850E/IG3</td>
<td>X1, X2</td>
<td>△</td>
<td>△</td>
<td>△</td>
</tr>
<tr>
<td>RESET</td>
<td>Output</td>
<td>Programming mode switching trigger</td>
<td>RESET</td>
<td>O</td>
<td>O</td>
<td>O</td>
</tr>
<tr>
<td>SO</td>
<td>Output</td>
<td>Command transmission to V850E/IG3</td>
<td>SIB0</td>
<td>O</td>
<td>O</td>
<td>×</td>
</tr>
<tr>
<td>SI</td>
<td>Input</td>
<td>Response status and data reception from V850E/IG3</td>
<td>SOB0</td>
<td>O</td>
<td>O</td>
<td>×</td>
</tr>
<tr>
<td>SCK</td>
<td>Output</td>
<td>Serial clock supply to V850E/IG3</td>
<td>SCKB0</td>
<td>O</td>
<td>O</td>
<td>×</td>
</tr>
<tr>
<td>HS (handshake)</td>
<td>Input</td>
<td>Handshake signal reception for serial communication with V850E/IG3</td>
<td>P43</td>
<td>×</td>
<td>O</td>
<td>×</td>
</tr>
<tr>
<td>TxD</td>
<td>Output</td>
<td>Command transmission to V850E/IG3</td>
<td>RXDA0</td>
<td>×</td>
<td>×</td>
<td>O</td>
</tr>
<tr>
<td>RxD</td>
<td>Input</td>
<td>Response status and data reception from V850E/IG3</td>
<td>TXDA0</td>
<td>×</td>
<td>×</td>
<td>O</td>
</tr>
</tbody>
</table>

Notes 1. VDD0, VDD1, EVDD0, EVDD1, EVDD2, AVDD0, AVDD1, AVDD2, AVREFP0, AVREFP1
2. VSS0, VSS1, EVSS0, EVSS1, EVSS2, AVSS0, AVSS1, AVSS2
3. Operation clock of V850E/IG3 is sourced from an oscillation circuit configured by an oscillator and a condenser on the board which mounted V850E/IG3.

Remark  
- O: Be sure to connect the pin.
- ×: The pin does not have to be connected.
- △: The pin does not have to be connected if the signal is generated on the target board.

For the voltage of the pins controlled by the programmer, refer to the user’s manual of the device that is subject to flash memory programming.
2.2 Details of Control Pins

2.2.1 Flash memory programming mode setting pins (FLMD0, FLMD1)

The FLMD0 and FLMD1 pins are used to control the operating mode of the V850E/IG3. The V850E/IG3 operates in flash memory programming mode when a specific voltage is supplied to these pins and a reset is released.

The mode for the serial communication between the programmer and the V850E/IG3 is determined by controlling the voltage at the FLMD0 pin between VDD and GND and outputting pulses, after reset. Refer to Table 2-3 for the relationship between the FLMD0 pulse counts and communication modes.
2.2.2 Serial interface pins (TxD, RxD, SI, SO, SCK, HS)

The serial interface pins are used to transfer the flash memory writing commands between the programmer and the V850E/IG3.

With the V850E/IG3, the communication mode can be selected from UART, CSI + HS, and CSI. The following figures illustrate the connection of pins used in each communication mode.

**Figure 2-1. Serial Interface Pins**

(1) UART communication mode

```
  Programmer   V850E/IG3
  TxD          RXDA0
  RxD          TXDA0
```

(2) 3-wire serial I/O communication mode with handshake supported (CSI + HS)

```
  Programmer   V850E/IG3
  SO           SIB0
  SCK          SCKB0
  SI           SOB0
  HS           P43
```

(3) 3-wire serial I/O communication mode (CSI)

```
  Programmer   V850E/IG3
  SO           SIB0
  SCK          SCKB0
  SI           SOB0
```
2.2.3 Reset control pin (RESET)

The reset control pin is used to control the system reset for the V850E/IG3 from the programmer. The flash memory programming mode can be selected when a specific voltage is supplied to the FLMD0 and FLMD1 pins and a reset is released.

Figure 2-2. Reset Control Pin

![Diagram of Reset Control Pin]

2.2.4 Clock control pin (CLK)

The clock control pin must not be connected with V850E/IG3. Mount an oscillator on user’s system as the operating clock to the V850E/IG3.

Figure 2-3. Clock Control Pin

![Diagram of Clock Control Pin]
2.2.5 VDD/GND control pins

The VDD control pin is used to supply power to the V850E/IG3 from the programmer. Connection of this pin is not necessary when it is not necessary to supply power to the V850E/IG3 from the programmer. However, this pin must be connected regardless of whether the power is supplied from the programmer when the dedicated programmer is used, because the dedicated programmer monitors the power supply status of the V850E/IG3.

The GND control pin must be connected to VSS of the V850E/IG3 regardless of whether the power is supplied from the programmer.

![VDD/GND Control Pin Diagram](image)

Figure 2-4. VDD/GND Control Pin

**Notes 1.** VDD0, VDD1, EVDD0, EVDD1, EVDD2, AVDD0, AVDD1, AVDD2, AVREFP0, AVREFP1

**2.** VSS0, VSS1, EVSS0, EVSS1, EVSS2, AVSS0, AVSS1, AVSS2

2.2.6 Other pins

For the connection of the pins that are not connected to the programmer, refer to the chapter describing the flash memory in the user’s manual of each device.
2.3 Basic Flowchart

The following illustrates the basic flowchart for performing flash memory rewriting with the programmer.

**Figure 2-5. Basic Flowchart for Flash Memory Rewrite Processing**

- **Basic flow**
  - Power application to target (See Figure 2-6)
  - Mode setting (reset release) (See 2.4)
  - Selection of communication mode (pulse input) (See 2.4/2.5)
  - Synchronization processing (Reset command) (See 5.2)
  - Oscillating frequency setting (Oscillating Frequency Set Command) (See 5.4)

  - UART communication? No
    - Baud rate setting (See 5.3)
  - Yes

- Command execution
  - Processing completed? No
    - Baud rate setting processing is not required when a mode other than UART communication mode is set.
  - Yes
  - Target power shutdown processing (See 2.9)

- End
2.4 Setting Flash Memory Programming Mode

To rewrite the contents of the flash memory with the programmer, the V850E/IG3 must first be set to the flash memory programming mode by supplying a specific voltage to the flash memory programming mode setting pins (FLMD0, FLMD1) in the V850E/IG3, then releasing a reset.

The following illustrates a timing chart for setting the flash memory programming mode and selecting the communication mode.

Figure 2-6. Setting Flash Memory Programming Mode and Selecting Communication Mode

The relationship between the settings of the FLMD0 and FLMD1 pins after reset release and the operating mode is shown below.

Table 2-2. Relationship Between Settings of FLMD0 and FLMD1 Pins After Reset Release and Operating Mode

<table>
<thead>
<tr>
<th>FLMD0</th>
<th>FLMD1</th>
<th>Operating Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low (GND)</td>
<td>Any</td>
<td>Normal operating mode</td>
</tr>
<tr>
<td>High (VDD)</td>
<td>Low (GND)</td>
<td>Flash memory programming mode</td>
</tr>
<tr>
<td>High (VDD)</td>
<td>High (VDD)</td>
<td>Setting prohibited</td>
</tr>
</tbody>
</table>
2.4.1 Mode setting flowchart

Processing to set programming mode

- RESET pin = low output
- FLMD0 pin = low output
- FLMD1 pin = low output

- VCC pin = high output (Target power supply on)

Wait for \( t_D \) (MIN.)

- FLMD0 pin = high output

Wait for \( t_R \) (MIN.)

- RESET pin = high output

Start measurement of time until the Reset command processing starts

UARTA0 communication (FLMD0 pulse = 0)?

Yes

No

Wait for \( (t_{RP}(\text{MIN.})+t_{RPE}(\text{MAX.}))/2 \)

Initialization of serial I/O hardware in accordance with communication mode

Initialization of serial I/O hardware in accordance with communication mode

Outputs the number of pulses corresponding to communication mode

Time until Reset command processing starts elapsed?

Yes

End

No

UART communication: \( t_R1 \) (MIN.) elapsed?

CSI communication: \( t_{xc} \) (MIN.) elapsed?

CSI + HS communication: HS pin READY?

Refer to Table 2-3 for the relationship between the pulse counts and communication modes.

After this flow, execute Reset command processing of the respective communication mode.
2.5 Selecting Serial Communication Mode

The communication mode is determined by inputting a pulse to the FLMD0 pin in the V850E/IG3 after reset release. The high- and low-levels of the FLMD0 pulse are VDD and GND, respectively. The following table shows the relationship between the number of FLMD0 pulses (pulse counts) and communication modes that can be selected with the V850E/IG3.

<table>
<thead>
<tr>
<th>Communication Mode</th>
<th>FLMD0 Pulse Counts</th>
<th>Port Used for Communication</th>
</tr>
</thead>
<tbody>
<tr>
<td>UART (UARTA0)</td>
<td>0</td>
<td>TxDA0 (P41), RxDA0 (P40)</td>
</tr>
<tr>
<td>3-wire serial I/O</td>
<td>8</td>
<td>SOB0 (P41), SIB0 (P40), SCKB0 (P42)</td>
</tr>
<tr>
<td>(CSIB0)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3-wire serial I/O</td>
<td>11</td>
<td>SOB0 (P41), SIB0 (P40), SCKB0 (P42), P43</td>
</tr>
<tr>
<td>with handshake</td>
<td></td>
<td></td>
</tr>
<tr>
<td>supported (CSIB0 + HS)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Setting prohibited</td>
<td>Others</td>
<td>–</td>
</tr>
</tbody>
</table>

2.6 UART Communication Mode

The RxD and TxD pins are used for UART communication. The communication conditions are as shown below.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud rate</td>
<td>Selectable from 9,600, 19,200, 31,250, 38,400, 76,800, and 153,600 bps (default: 9,600 bps)</td>
</tr>
<tr>
<td>Parity bit</td>
<td>None</td>
</tr>
<tr>
<td>Data length</td>
<td>8 bits (LSB first)</td>
</tr>
<tr>
<td>Stop bit</td>
<td>1 bit</td>
</tr>
</tbody>
</table>

The programmer always operates as the master device during CSI communication, so the programmer must check whether the processing by the V850E/IG3, such as writing or erasing, is normally completed. On the other hand, the status of the master and slave is occasionally exchanged during UART communication, so communication at the optimum timing is possible without assigning one pin like CSI + HS communication.

Caution Set the same baud rate to the master and slave devices when performing UART communication.
2.7 3-Wire Serial I/O Communication Mode with Handshake Supported (CSI + HS)

In the CSI + HS communication mode, the timing for communication of commands or data is optimized. In addition to the SI, SO and SCK pins, the HS (handshake) pin is used for implementing effective communication.

The level of the HS pin signal falls (low level) when the V850E/IG3 is ready for transmitting or receiving data. The programmer must check the falling edge of the HS pin signal (low level) before starting transmission/reception of commands or data to the V850E/IG3.

The communication data format is MSB-first, in 8-bit units. Keep the clock frequency 5 MHz or lower.

Figure 2-7. Timing Chart of CSI + HS Communication

2.8 3-Wire Serial I/O Communication Mode (CSI)

The SCK, SO and SI pins are used for CSI communication. The programmer always operates as the master device, so communication may not be performed normally if data is transmitted via the SCK pin while the V850E/IG3 is not ready for transmission/reception.

The communication data format is MSB-first, in 8-bit units. Keep the clock frequency 5 MHz or lower.

2.9 Shutting Down Target Power Supply

After each command execution is completed, shut down the power supply to the target after setting the RESET pin to low level, as shown below.

Set other pins to Hi-Z when shutting down the power supply to the target.

Caution Shutting down the power supply and inputting a reset during command processing are prohibited.

Figure 2-8. Timing for Terminating Flash Memory Programming Mode
2.10 Manipulation of Flash Memory

The flash memory incorporated in the V850E/IG3 has functions to manipulate the flash memory, as listed in Table 2-5. The programmer transmits commands to control these functions to the V850E/IG3, and checks the response status sent from the V850E/IG3, to manipulate the flash memory.

<table>
<thead>
<tr>
<th>Classification</th>
<th>Function Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Erase</td>
<td>Chip erase</td>
<td>Erases the entire flash memory area. Clears the security flag.</td>
</tr>
<tr>
<td></td>
<td>Block erase</td>
<td>Erases a specified block in the flash memory.</td>
</tr>
<tr>
<td>Write</td>
<td>Write</td>
<td>Writes data to a specified area in the flash memory.</td>
</tr>
<tr>
<td>Verify</td>
<td>Verify</td>
<td>Compares data acquired from a specified address in the flash memory with data transmitted from the programmer, on the V850E/IG3 side.</td>
</tr>
<tr>
<td>Blank check</td>
<td>Block blank check</td>
<td>Checks the erase status of a specified area in the flash memory.</td>
</tr>
<tr>
<td>Read</td>
<td>Read</td>
<td>Reads data of a specified area in the flash memory.</td>
</tr>
<tr>
<td>Information acquisition</td>
<td>Silicon signature acquisition</td>
<td>Acquires writing protocol information.</td>
</tr>
<tr>
<td></td>
<td>Version acquisition</td>
<td>Acquires version information of the V850E/IG3 and firmware.</td>
</tr>
<tr>
<td></td>
<td>Status acquisition</td>
<td>Acquires the current operating status.</td>
</tr>
<tr>
<td></td>
<td>Checksum acquisition</td>
<td>Acquires checksum data of a specified area.</td>
</tr>
<tr>
<td>Security</td>
<td>Security setting</td>
<td>Sets security information.</td>
</tr>
<tr>
<td>Other</td>
<td>Reset</td>
<td>Detects synchronization in communication.</td>
</tr>
</tbody>
</table>

2.11 Command List

The commands used by the programmer and their functions are listed below.

<table>
<thead>
<tr>
<th>Command Number</th>
<th>Command Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>70H</td>
<td>Status</td>
<td>Acquires the current operating status (status data).</td>
</tr>
<tr>
<td>00H</td>
<td>Reset</td>
<td>Detects synchronization in communication.</td>
</tr>
<tr>
<td>90H</td>
<td>Oscillating Frequency Set</td>
<td>Specifies the oscillation frequency of the V850E/IG3.</td>
</tr>
<tr>
<td>9AH</td>
<td>Baud Rate Set</td>
<td>Sets baud rate when UART communication mode is selected.</td>
</tr>
<tr>
<td>20H</td>
<td>Chip Erase</td>
<td>Erases the entire flash memory area.</td>
</tr>
<tr>
<td>22H</td>
<td>Block Erase</td>
<td>Erases a specified area in the flash memory.</td>
</tr>
<tr>
<td>40H</td>
<td>Programming</td>
<td>Writes data to a specified area in the flash memory.</td>
</tr>
<tr>
<td>13H</td>
<td>Verify</td>
<td>Compares the contents in a specified area in the flash memory with data transmitted from the programmer.</td>
</tr>
<tr>
<td>32H</td>
<td>Block Blank Check</td>
<td>Checks the erase status of a specified block in the flash memory.</td>
</tr>
<tr>
<td>C0H</td>
<td>Silicon Signature</td>
<td>Acquires V850E/IG3 information (part number, flash memory configuration, etc.).</td>
</tr>
<tr>
<td>C5H</td>
<td>Version Get</td>
<td>Acquires version information of the V850E/IG3 and firmware.</td>
</tr>
<tr>
<td>B0H</td>
<td>Checksum</td>
<td>Acquires checksum data of a specified area.</td>
</tr>
<tr>
<td>A0H</td>
<td>Security Set</td>
<td>Sets security information.</td>
</tr>
<tr>
<td>50H</td>
<td>Read</td>
<td>Reads data of a specified area in the flash memory.</td>
</tr>
</tbody>
</table>
2.12 Status List

The following table lists the status codes the programmer receives from the V850E/IG3.

<table>
<thead>
<tr>
<th>Status Code</th>
<th>Status Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>04H</td>
<td>Command number error (Error returned if a command not supported is received)</td>
</tr>
<tr>
<td>05H</td>
<td>Parameter error (Error returned if command information (parameter) is invalid)</td>
</tr>
<tr>
<td>06H</td>
<td>Normal acknowledgment (ACK)</td>
</tr>
<tr>
<td>07H</td>
<td>Checksum error (Error returned if data in a frame transmitted from the programmer is abnormal)</td>
</tr>
<tr>
<td>0FH</td>
<td>Verify error (Error returned if a verify error has occurred upon verifying data transmitted from the programmer)</td>
</tr>
<tr>
<td>10H</td>
<td>Protect error (Error returned if an attempt is made to execute processing that is prohibited by the Security Set command)</td>
</tr>
<tr>
<td>15H</td>
<td>Negative acknowledgment (NACK)</td>
</tr>
<tr>
<td>18H</td>
<td>FLMD error (Error returned when a write error has occurred)</td>
</tr>
<tr>
<td>1AH</td>
<td>MRG10 error (Erase error)</td>
</tr>
<tr>
<td>1BH</td>
<td>MRG11 error (Internal verify error or blank check error during data write)</td>
</tr>
<tr>
<td>1CH</td>
<td>Write error</td>
</tr>
</tbody>
</table>
| FFH         | Processing in progress (BUSY) (Busy response)

**Note** During CSI communication, 1-byte “FFH” may be transmitted, as well as “FFH” as the data frame format.

Reception of a checksum error or NACK is treated as an immediate abnormal end in this manual. When a dedicated programmer is developed, however, the processing may be retried without problem from the wait immediately before transmission of the command that results a checksum error or NACK or after BUSY status check via the HS pin. In this event, limiting the retry count is recommended for preventing infinite repetition of the retry operation.

Although not listed in the above table, if a time-out error (BUSY time-out, HS pin time-out, or time-out in data frame reception during UART communication) occurs, it is recommended to shutdown the power supply to the V850E/IG3 (refer to 2.9 Shutting Down Target Power Supply) and then connect the power supply again.
CHAPTER 3 BASIC PROGRAMMER OPERATION

Figure 3-1 illustrates the general command execution flow when flash memory rewriting is performed with the programmer.

**Figure 3-1. General Command Execution Flow at Flash Memory Rewriting**

- General command flow
- Flash memory programming mode is set
- Reset command
- Oscillating Frequency Set command
- Baud Rate Set command (in UART communication mode only)
- Block Blank Check command
- Chip Erase command
- Programming command
- Security Set command
- Flash memory programming mode is exited
- End

**Note**  It is recommended to perform security settings to disable read as a default in programmer specification.

**Remark**  The Verify command, Checksum command, and Read command can also be supported.
CHAPTER 4 COMMAND/DATA FRAME FORMAT

The programmer uses the command frame to transmit commands to the V850E/IG3. The V850E/IG3 uses the data frame to transmit write data or verify data to the programmer. A header, footer, data length information, and checksum are appended to each frame to enhance the reliability of the transferred data.

The following shows the format of a command frame and data frame.

### Figure 4-1. Command Frame Format

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOH</td>
<td>01H</td>
<td>Command frame header</td>
</tr>
<tr>
<td>LEN</td>
<td>–</td>
<td>Data length information (00H indicates 256).</td>
</tr>
<tr>
<td>COM</td>
<td>–</td>
<td>Command number</td>
</tr>
<tr>
<td>SUM</td>
<td>–</td>
<td>Checksum data for a frame</td>
</tr>
<tr>
<td>ETX</td>
<td>03H</td>
<td>Command frame footer, or footer of last data frame</td>
</tr>
</tbody>
</table>

### Figure 4-2. Data Frame Format

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>STX</td>
<td>02H</td>
<td>Data frame header</td>
</tr>
<tr>
<td>LEN</td>
<td>–</td>
<td>Data field length</td>
</tr>
<tr>
<td>SUM</td>
<td>–</td>
<td>Checksum data for a frame</td>
</tr>
<tr>
<td>ETB</td>
<td>17H</td>
<td>Footer of data frame other than the last frame</td>
</tr>
<tr>
<td>ETX</td>
<td>03H</td>
<td>Command frame footer, or footer of last data frame</td>
</tr>
</tbody>
</table>

Table 4-1. Description of Symbols in Each Frame

The following shows examples of calculating the checksum (SUM) for a frame.
[Command frame]
No command information is included in the following example of a Status command frame, so LEN and COM are targets of checksum calculation.

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>70H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Checksum calculation targets

For this command frame, checksum data is obtained as follows.

\[00H \text{ (initial value)} - 01H \text{ (LEN)} - 70H \text{ (COM)} = 8FH\] (Borrow ignored. Lower 8 bits only.)

The command frame finally transmitted is as follows.

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>70H</td>
<td>8FH</td>
<td>03H</td>
</tr>
</tbody>
</table>

[Data frame]
To transmit a data frame as shown below, LEN and D1 to D4 are targets of checksum calculation.

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>04H</td>
<td>FFH</td>
<td>80H</td>
<td>40H</td>
<td>22H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Checksum calculation targets

For this data frame, checksum data is obtained as follows.

\[00H \text{ (initial value)} - 04H \text{ (LEN)} - FFH \text{ (D1)} - 80H \text{ (D2)} - 40H \text{ (D3)} - 22H \text{ (D4)} = 1BH\] (Borrow ignored. Lower 8 bits only.)

The data frame finally transmitted is as follows.

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>04H</td>
<td>FFH</td>
<td>80H</td>
<td>40H</td>
<td>22H</td>
<td>1BH</td>
<td>03H</td>
</tr>
</tbody>
</table>

When a data frame is received, the checksum data is calculated in the same manner, and the obtained value is used to detect a checksum error by judging whether the value is the same as that stored in the SUM field of the receive data. When a data frame as shown below is received, for example, a checksum error is detected.

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>04H</td>
<td>FFH</td>
<td>80H</td>
<td>40H</td>
<td>22H</td>
<td>1AH</td>
<td>03H</td>
</tr>
</tbody>
</table>

\[^{\uparrow}\text{Should be 1BH, if normal}\]
4.1 Command Frame Transmission Processing

Read the following chapters for details on flowcharts of command processing to transmit command frames, for each communication mode.

- For the UART communication mode, read 6.1 Flowchart of Command Frame Transmission Processing.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 7.1 Flowchart of Command Frame Transmission Processing.
- For the 3-wire serial I/O communication mode (CSI), read 8.1 Flowchart of Command Frame Transmission Processing.

4.2 Data Frame Transmission Processing

The write data frame (user program), verify data frame (user program), and security data frame (security flag) are transmitted as a data frame.

Read the following chapters for details on flowcharts of command processing to transmit data frames, for each communication mode.

- For the UART communication mode, read 6.2 Flowchart of Data Frame Transmission Processing.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 7.2 Flowchart of Data Frame Transmission Processing.
- For the 3-wire serial I/O communication mode (CSI), read 8.2 Flowchart of Data Frame Transmission Processing.

4.3 Data Frame Reception Processing

The status frame, silicon signature data frame, version data frame, checksum data frame, and read data frame are received as a data frame.

Read the following chapters for details on flowcharts of command processing to receive data frames, for each communication mode.

- For the UART communication mode, read 6.3 Flowchart of Data Frame Reception Processing.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 7.3 Flowchart of Data Frame Reception Processing.
- For the 3-wire serial I/O communication mode (CSI), read 8.3 Flowchart of Data Frame Reception Processing.
CHAPTER 5 DESCRIPTION OF COMMAND PROCESSING

5.1 Status Command

5.1.1 Description
This command is used to check the operation status of the V850E/IG3 after issuance of each command such as write or erase.

After the Status command is issued, if the Status command frame cannot be received normally in the V850E/IG3 due to problems based on communication or the like, the status setting will not performed in the V850E/IG3. As a result, a busy response (FFH), not the status frame, may be received. In such a case, retry the Status command.

5.1.2 Command frame and status frame
Figure 5-1 shows the format of a command frame for the Status command, and Figure 5-2 shows the status frame for the command.

Figure 5-1. Status Command Frame (from Programmer to V850E/IG3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>70H (Status)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Figure 5-2. Status Frame for Status Command (from V850E/IG3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>n</td>
<td>ST1</td>
<td>...</td>
<td>STn</td>
</tr>
</tbody>
</table>

Remarks
1. ST1 to STn: Status #1 to Status #n
2. The length of a status frame varies according to each command (such as write or erase) to be transmitted to the V850E/IG3.

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850E/IG3, flowcharts of command processing, and sample programs for each communication mode.

- The Status command is not used in the UART communication mode.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 7.4 Status Command.
- For the 3-wire serial I/O communication mode (CSI), read 8.4 Status Command.

Caution
After each command such as write or erase is transmitted in UART communication, the V850E/IG3 automatically returns the status frame within a specified time. The Status command is therefore not used.
If the Status command is transmitted in UART communication, the Command Number Error is returned.
5.2 Reset Command

5.2.1 Description

This command is used to check the establishment of communication between the programmer and the V850E/IG3 after the communication mode is set.

When UART is selected as the mode for communication with the V850E/IG3, the same baud rate must be set in the programmer and V850E/IG3. However, the V850E/IG3 cannot detect its own operating frequency so the baud rate cannot be set. It makes detection of the operating frequency in the V850E/IG3 possible by sending "00H" twice at 9,600 bps from the programmer, measuring the low-level width of "00H", and then calculating the average of two sent signals. The baud rate can consequently be set, which enables synchronous detection in communication.

5.2.2 Command frame and status frame

Figure 5-3 shows the format of a command frame for the Reset command, and Figure 5-4 shows the status frame for the command.

**Figure 5-3. Reset Command Frame (from Programmer to V850E/IG3)**

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>00H (Reset)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Figure 5-4. Status Frame for Reset Command (from V850E/IG3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>1</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  ST1: Synchronization detection result

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850E/IG3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 6.4 Reset Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 7.5 Reset Command.
- For the 3-wire serial I/O communication mode (CSI), read 8.5 Reset Command.
5.3 Baud Rate Set Command

5.3.1 Description
This command is used to change the baud rate for UART (default value: 9,600 bps).
After the Baud Rate Set command is executed, the Reset command must be executed to confirm synchronization at the new baud rate.
The Baud Rate Set command is valid only in the UART communication mode. Data for setting the baud rate is represented as a 1-byte numeric value.
The V850E/IG3 ignores the Baud Rate Set command if it is transmitted in modes other than the UART communication mode.

5.3.2 Command frame and status frame
Figure 5-5 shows the format of a command frame for the Baud Rate Set command, and Figure 5-6 shows the status frame for the command.

Figure 5-5. Baud Rate Set Command Frame (from Programmer to V850E/IG3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>02H</td>
<td>9AH</td>
<td>(Baud Rate Set)</td>
<td>D01</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  D01: Baud rate selection value

<table>
<thead>
<tr>
<th>D01 Value</th>
<th>03H</th>
<th>04H</th>
<th>05H</th>
<th>06H</th>
<th>07H</th>
<th>08H</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud rate (bps)</td>
<td>9600</td>
<td>19200</td>
<td>31250</td>
<td>38400</td>
<td>76800</td>
<td>153600</td>
</tr>
</tbody>
</table>

Figure 5-6. Status Frame for Baud Rate Set Command (from V850E/IG3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  ST1: Synchronization detection result

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850E/IG3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 6.5 Baud Rate Set Command.
- The Baud Rate Set command is not used in the 3-wire serial I/O communication mode with handshake supported (CSI + HS).
- The Baud Rate Set command is not used in 3-wire serial I/O communication mode (CSI).
5.4 Oscillating Frequency Set Command

5.4.1 Description
This command is used to set oscillation frequency data in the V850E/IG3. Set the frequency of the clock that is actually input to the X1 pin of the V850E/IG3. However, the V850E/IG3 will multiply the CPU operation clock by 8 through the internal PLL immediately after reset.

5.4.2 Command frame and status frame
Figure 5-7 shows the format of a command frame for the Oscillating Frequency Set command, and Figure 5-8 shows the status frame for the command.

Figure 5-7. Oscillating Frequency Set Command Frame (from Programmer to V850E/IG3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>05H</td>
<td>90H</td>
<td>(Oscillating Frequency Set)</td>
<td>D01</td>
<td>D02</td>
</tr>
</tbody>
</table>

Remark D01 to D04: Oscillation frequency = (D01 × 0.1 + D02 × 0.01 + D03 × 0.001) × 10^4 (Unit: kHz)
Settings can be made from 10 kHz to 100 MHz, but set the value according to the specifications of each device when actually transmitting the command. D01 to D03 hold unpacked BCDs, and D04 holds a signed integer.

Setting example: To set 8 MHz
D01 = 08H
D02 = 00H
D03 = 00H
D04 = 04H
Oscillation frequency = 0.1 × 8 × 10^4 = 8,000 kHz = 8 MHz

Figure 5-8. Status Frame for Oscillating Frequency Set Command (from V850E/IG3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark ST1: Oscillation frequency setting result
Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850E/IG3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 6.6 Oscillating Frequency Set Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 7.6 Oscillating Frequency Set Command.
- For the 3-wire serial I/O communication mode (CSI), read 8.6 Oscillating Frequency Set Command.
5.5 Chip Erase Command

5.5.1 Description

This command is used to erase the entire contents of the flash memory. In addition, all of the information that is set by security setting processing can be initialized by chip erase processing, as long as Chip Erase command execution is impossible by the security setting (see 5.13 Security Set Command).

5.5.2 Command frame and status frame

Figure 5-9 shows the format of a command frame for the Chip Erase command, and Figure 5-10 shows the status frame for the command.

![Figure 5-9. Chip Erase Command Frame (from Programmer to V850E/IG3)](image1)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>20H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

(Chip Erase)

![Figure 5-10. Status Frame for Chip Erase Command (from V850E/IG3 to Programmer)](image2)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark ST1: Chip erase result

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850E/IG3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 6.7 Chip Erase Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 7.7 Chip Erase Command.
- For the 3-wire serial I/O communication mode (CSI), read 8.7 Chip Erase Command.
5.6 Block Erase Command

5.6.1 Description
This command is used to erase the contents of blocks with the specified number in the flash memory, as long as Chip Erase command execution is impossible by the security setting (see 5.13 Security Set Command).

5.6.2 Command frame and status frame
Figure 5-11 shows the format of a command frame for the Block Erase command, and Figure 5-12 shows the status frame for the command.

Figure 5-11. Block Erase Command Frame (from Programmer to V850E/IG3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>22H (Block Erase)</td>
<td>SAH</td>
<td>SAM</td>
<td>SAL</td>
</tr>
</tbody>
</table>

Remark  SAH, SAM, SAL: Block erase start address (start address of the block)
EAH, EAM, EAL: Block erase end address (end address of the block)

Figure 5-12. Status Frame for Block Erase Command (from V850E/IG3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  ST1: Block erase result

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850E/IG3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 6.8 Block Erase Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 7.8 Block Erase Command.
- For the 3-wire serial I/O communication mode (CSI), read 8.8 Block Erase Command.
5.7 Programming Command

5.7.1 Description

This command is used to transmit data by the number of written bytes after the write start address and the write end address are transmitted. This command then writes the user program to the flash memory and verifies it internally.

The write start/end address can be set only in the block start/end address units.

If both of the status frames (ST1 and ST2) after the last data transmission indicate ACK, the V850E/IG3 firmware automatically executes internal verify. Therefore, the Status command for this internal verify must be transmitted.

After executing the Programming command, it is recommended to execute the Security Set command that disables read as a default in programmer specification.

5.7.2 Command frame and status frame

Figure 5-13 shows the format of a command frame for the Programming command, and Figure 5-14 shows the status frame for the command.

**Figure 5-13. Programming Command Frame (from Programmer to V850E/IG3)**

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>40H</td>
<td>Programming</td>
<td>SAH</td>
<td>SAM</td>
</tr>
</tbody>
</table>

**Remark** SAH, SAM, SAL: Write start addresses
EAH, EAM, EAL: Write end addresses

**Figure 5-14. Status Frame for Programming Command (from V850E/IG3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (a)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark** ST1 (a): Command reception result

5.7.3 Data frame and status frame

Figure 5-15 shows the format of a frame that includes data to be written, and Figure 5-16 shows the status frame for the data.

**Figure 5-15. Data Frame to Be Written (from Programmer to V850E/IG3)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX/ETB</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>00H to FFH (00H = 256)</td>
<td>Write Data</td>
<td>Checksum</td>
<td>03H/17H</td>
</tr>
</tbody>
</table>

**Remark** Write Data: User program to be written

**Figure 5-16. Status Frame for Data Frame (from V850E/IG3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>02H</td>
<td>ST1 (b)</td>
<td>ST2 (b)</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

**Remark** ST1 (b): Data reception check result
ST2 (b): Write result
5.7.4 Completion of transferring all data and status frame

Figure 5-17 shows the status frame after transfer of all data is completed.

**Figure 5-17. Status Frame After Completion of Transferring All Data (from V850E/IG3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (c)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**  ST1 (c): Internal verify result

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850E/IG3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read **6.9 Programming Command**.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read **7.9 Programming Command**.
- For the 3-wire serial I/O communication mode (CSI), read **8.9 Programming Command**.
5.8 Verify Command

5.8.1 Description
This command is used to compare the data transmitted from the programmer with the data read from the V850E/IG3 (read level) in the specified address range, and check whether they match.

The verify start/end address can be set only in the block start/end address units.

5.8.2 Command frame and status frame
Figure 5-18 shows the format of a command frame for the Verify command, and Figure 5-19 shows the status frame for the command.

Figure 5-18. Verify Command Frame (from Programmer to V850E/IG3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>13H</td>
<td>SAH, SAM, SAL</td>
<td>EAH</td>
<td>EAM</td>
</tr>
</tbody>
</table>

Remark
SAH, SAM, SAL: Verify start addresses
EAH, EAM, EAL: Verify end addresses

Figure 5-19. Status Frame for Verify Command (from V850E/IG3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (a)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark
ST1 (a): Command reception result

5.8.3 Data frame and status frame
Figure 5-20 shows the format of a frame that includes data to be verified, and Figure 5-21 shows the status frame for the data.

Figure 5-20. Data Frame of Data to Be Verified (from Programmer to V850E/IG3)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX/ETB</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>00H to FFH (00H = 256)</td>
<td>Verify data</td>
<td>Checksum</td>
<td>03H/17H</td>
</tr>
</tbody>
</table>

Remark
Verify Data: User program to be verified
Figure 5-21. Status Frame for Data Frame (from V850E/IG3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>02H</td>
<td>ST1 (b)</td>
<td>ST2 (b)</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

**Remark**  
ST1 (b): Data reception check result  
ST2 (b): Verify result\(^{\text{Note}}\)

**Note**  
Even if a verify error occurs in the specified address range, ACK is always returned as the verify result. The status of all verify errors are reflected in the verify result for the last data. Therefore, the occurrence of verify errors can be checked only when all the verify processing for the specified address range is completed.

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850E/IG3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 6.10 Verify Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 7.10 Verify Command.
- For the 3-wire serial I/O communication mode (CSI), read 8.10 Verify Command.
5.9 Block Blank Check Command

5.9.1 Description
This command is used to check if a block in the flash memory, with a specified block number, is blank (erased state).

5.9.2 Command frame and status frame
Figure 5-22 shows the format of a command frame for the Block Blank Check command, and Figure 5-23 shows the status frame for the command.

![Figure 5-22. Block Blank Check Command Frame (from Programmer to V850E/IG3)](image1)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>32H</td>
<td>(Block Blank Check)</td>
<td>SAH</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SAM</td>
<td></td>
<td>SAL</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>EAH</td>
<td></td>
<td>EAM</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>EAL</td>
<td></td>
<td>EAL</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Checksum</td>
<td>03H</td>
<td></td>
</tr>
</tbody>
</table>

Remark  SAH, SAM, SAL: Block blank check start address (start address of the block)
EAH, EAM, EAL: Block blank check end address (end address of the block)

![Figure 5-23. Status Frame for Block Blank Check Command (from V850E/IG3 to Programmer)](image2)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  ST1: Block blank check result

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850E/IG3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 6.11 Block Blank Check Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 7.11 Block Blank Check Command.
- For the 3-wire serial I/O communication mode (CSI), read 8.11 Block Blank Check Command.
5.10 Silicon Signature Command

5.10.1 Description

This command is used to read the write protocol information (silicon signature) of the device.

If the programmer supports a programming protocol that is not supported in the V850E/IG3, for example, execute this command to select an appropriate protocol in accordance with the values of the second and third bytes.

5.10.2 Command frame and status frame

Figure 5-24 shows the format of a command frame for the Silicon Signature command, and Figure 5-25 shows the status frame for the command.

Figure 5-24. Silicon Signature Command Frame (from Programmer to V850E/IG3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>C0H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

(Silicon Signature)

Figure 5-25. Status Frame for Silicon Signature Command (from V850E/IG3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark ST1: Command reception result

5.10.3 Silicon signature data frame

Figure 5-26 shows the format of a frame that includes silicon signature data.

Figure 5-26. Silicon Signature Data Frame (from V850E/IG3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>VEN</th>
<th>EXT</th>
<th>MSC</th>
<th>DEC</th>
<th>INValid data</th>
<th>SCF</th>
<th>BOT</th>
<th>Checksum</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>n</td>
<td>VEN</td>
<td>EXT</td>
<td>MSC</td>
<td>DEC</td>
<td>Invalid data</td>
<td>SCF</td>
<td>BOT</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remarks 1. VEN: Vendor code (NEC: 10H)
MET: Macro extension code
MSC: Macro function code
DEC: Device extension code
INVALID DATA: Invalid data of 3 byte length.
DEV: Device name (10 bytes)
SCF: Security flag information
BOT: The last block number of the boot block cluster

2. For above data frames except the last block number of the boot block cluster (BOT), the lower 7 bits are used entity, and the highest bit is used as an odd parity. The following shows an example.
Table 5-1. Example of Silicon Signature Data

<table>
<thead>
<tr>
<th>Field</th>
<th>Contents</th>
<th>Length (Byte)</th>
<th>Example of Silicon Signature Data[Note]</th>
<th>Actual Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEN</td>
<td>Vendor code (NEC)</td>
<td>1</td>
<td>10H (00010000B)</td>
<td>10H</td>
</tr>
<tr>
<td>MET</td>
<td>Extension code (fixed)</td>
<td>1</td>
<td>7FH (11111111B)</td>
<td>7FH</td>
</tr>
<tr>
<td>MSC</td>
<td>Macro function code (fixed)</td>
<td>1</td>
<td>02H (00000100B)</td>
<td>02H</td>
</tr>
<tr>
<td>DEC</td>
<td>Device extension code (fixed)</td>
<td>1</td>
<td>FEH (11111110B)</td>
<td>7EH</td>
</tr>
<tr>
<td>INVALID DATA</td>
<td>Invalid data</td>
<td>13</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>DEV</td>
<td>Device name</td>
<td>10</td>
<td>C4H (11000100B) ‘D’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>37H (00111011B) ‘7’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0BH (11010000B) ‘0’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>46H (01000110B) ‘F’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>B3H (11010011B) ‘3’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>34H (0110100B) ‘4’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>B5H (11010101B) ‘5’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>58H (01011000B) ‘X’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20H (00100000B) ‘ ’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20H (00100000B) ‘ ’</td>
<td></td>
</tr>
<tr>
<td>SCF</td>
<td>Security setting</td>
<td>1</td>
<td>7FH (11111111B)</td>
<td>7FH</td>
</tr>
<tr>
<td>BOT</td>
<td>The last block number of the boot block cluster</td>
<td>1</td>
<td>00H (no parity)</td>
<td>00H</td>
</tr>
</tbody>
</table>

Note: 0 and 1 are odd parities (the value to adjust the number of “1” in a byte).

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850E/IG3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 6.12 Silicon Signature Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 7.12 Silicon Signature Command.
- For the 3-wire serial I/O communication mode (CSI), read 8.12 Silicon Signature Command.
5.11 Version Get Command

5.11.1 Description
This command is used to acquire information on the V850E/IG3 device version and firmware version.
Use this command when the programming parameters must be changed in accordance with the V850E/IG3 firmware version.

Caution  The firmware version may be updated during firmware update that does not affect the change of flash programming parameters (at this time, update of the firmware version is not reported).

Example  Firmware version and reprogramming parameters

5.11.2 Command frame and status frame
Figure 5-28 shows the format of a command frame for the Version Get command, and Figure 5-29 shows the status frame for the command.

Figure 5-28. Version Get Command Frame (from Programmer to V850E/IG3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>C5H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Figure 5-29. Status Frame for Version Get Command (from V850E/IG3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  ST1: Command reception result
5.11.3 Version data frame

Figure 5-30 shows the data frame of version data.

**Figure 5-30. Version Data Frame (from V850E/IG3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>06H</td>
<td>DV1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DV2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DV3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>FV1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>FV2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>FV3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Checksum</td>
<td></td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**
- DV1: Integer of device version
- DV2: First decimal place of device version
- DV3: Second decimal place of device version
- FV1: Integer of firmware version
- FV2: First decimal place of firmware version
- FV3: Second decimal place of firmware version

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850E/IG3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read **6.13 Version Get Command**.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read **7.13 Version Get Command**.
- For the 3-wire serial I/O communication mode (CSI), read **8.13 Version Get Command**.
5.12 Checksum Command

5.12.1 Description

This command is used to acquire the checksum data in the specified area.

For the checksum calculation start/end address, specify a fixed address in block units (2 KB) starting from the top of the flash memory.

Checksum data is obtained by sequentially subtracting data in the specified address range from the initial value (00H) in 1-byte units.

5.12.2 Command frame and status frame

Figure 5-31 shows the format of a command frame for the Checksum command, and Figure 5-32 shows the status frame for the command.

**Figure 5-31. Checksum Command Frame (from Programmer to V850E/IG3)**

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>B0H</td>
<td>SAH</td>
<td>SAM</td>
<td>SAL</td>
</tr>
</tbody>
</table>

**Remark**  
SAH, SAM, SAL: Checksum calculation start addresses  
EAH, EAM, EAL: Checksum calculation end addresses

**Figure 5-32. Status Frame for Checksum Command (from V850E/IG3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**  
ST1: Command reception result

5.12.3 Checksum data frame

Figure 5-33 shows the format of a frame that includes checksum data.

**Figure 5-33. Checksum Data Frame (from V850E/IG3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>02H</td>
<td>CK1</td>
<td>CK2</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

**Remark**  
CK1: Higher 8 bits of checksum data  
CK2: Lower 8 bits of checksum data

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850E/IG3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 6.14 Checksum Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 7.14 Checksum Command.
- For the 3-wire serial I/O communication mode (CSI), read 8.14 Checksum Command.
5.13 Security Set Command

5.13.1 Description

This command is used to perform security settings (enable or disable of write, block erase, and chip erase). By performing these settings with this command, rewriting of the flash memory by an unauthorized party can be restricted. After executing the Programming command, it is recommended to execute the Security Set command that disables read as a default in programmer specification.

Caution Once the security setting is performed, additional setting to the security flags or changing of the setting from disable to enable will no longer be possible. If such settings are attempted, a Protect error (10H) will occur. To re-set the security flag, all the security flags must be initialized by executing the Chip Erase command (the Block Erase command cannot be used to initialize the security flags). If chip erase has been disabled (Chip Erase command execution impossible), however, chip erase itself will be impossible and so the settings cannot be erased from the programmer. Re-confirmation of security setting execution is therefore recommended before disabling chip erase (Chip Erase command execution impossible), due to this programmer specification.

5.13.2 Command frame and status frame

Figure 5-34 shows the format of a command frame for the Security Set command, and Figure 5-35 shows the status frame for the command.

The Security Set command frame includes the block number field and page number field but these fields do not have any particular usage, so set these fields to 00H.

**Figure 5-34. Security Set Command Frame (from Programmer to V850E/IG3)**

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>03H</td>
<td>A0H (Security Set)</td>
<td>00H (fixed)</td>
<td>00H (fixed)</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

**Remark** BLK, PAG: Fixed to 00H

**Figure 5-35. Status Frame for Security Set Command (from V850E/IG3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (a)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark** ST1 (a): Command reception result
5.13.3 Data frame and status frame

Figure 5-36 shows the format of a security data frame, and Figure 5-37 shows the status frame for the data.

Figure 5-36 Security Data Frame (from Programmer to V850E/IG3)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>02H</td>
<td>FLG</td>
<td>BOT</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

**Remark**
- FLG: Security flag
- BOT: The last block number of the boot block cluster
- (When bit 4 in FLG = 1, it is fixed to 00H. When the bit is 0, its value is arbitrary.)

Figure 5-37. Status Frame for Security Data Writing (from V850E/IG3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (b)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**
- ST1 (b): Security data write result

5.13.4 Internal verify check and status frame

Figure 5-38 shows the status frame for internal verify check.

Figure 5-38. Status Frame for Internal Verify Check (from V850E/IG3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (c)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**
- ST1 (c): Internal verify result

The following table shows the contents in the security flag field.

<table>
<thead>
<tr>
<th>Item</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>Fixed to “1”</td>
</tr>
<tr>
<td>Bit 6</td>
<td></td>
</tr>
<tr>
<td>Bit 5</td>
<td></td>
</tr>
<tr>
<td>Bit 4</td>
<td>Boot block cluster rewrite disable flag (1: Enables rewrite, 0: Disables rewrite)</td>
</tr>
<tr>
<td>Bit 3</td>
<td>Read disable flag (1: Enables read, 0: Disables read)</td>
</tr>
<tr>
<td>Bit 2</td>
<td>Programming disable flag (1: Enables programming, 0: Disables programming)</td>
</tr>
<tr>
<td>Bit 1</td>
<td>Block erase disable flag (1: Enables block erase, 0: Disables block erase)</td>
</tr>
<tr>
<td>Bit 0</td>
<td>Chip erase disable flag (1: Enables chip erase, 0: Disables chip erase)</td>
</tr>
</tbody>
</table>
The following table shows the relationship between the security flag field settings and the enable/disable status of each operation.

### Table 5-3. Security Flag Field and Enable/Disable Status of Each Operation

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>Flash Memory Programming Mode</th>
<th>Self-Programming Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Command Operation After Security Setting</td>
<td>• All commands can be executed regardless of the security setting values</td>
</tr>
<tr>
<td></td>
<td>(\checkmark): Execution possible, (\times): Execution impossible</td>
<td>• Retention of security setting values and change from enabled to disabled are possible</td>
</tr>
<tr>
<td></td>
<td>(\triangle): Writing and block erase in boot area are impossible</td>
<td></td>
</tr>
<tr>
<td>Security Setting Item</td>
<td>Programming</td>
<td>Chip Erase</td>
</tr>
<tr>
<td>Disable programming</td>
<td>(\times)</td>
<td>(\checkmark)</td>
</tr>
<tr>
<td>Disable chip erase</td>
<td>(\checkmark)</td>
<td>(\times)</td>
</tr>
<tr>
<td>Disable block erase</td>
<td>(\checkmark)</td>
<td>(\checkmark)</td>
</tr>
<tr>
<td>Disable read</td>
<td>(\checkmark)</td>
<td>(\checkmark)</td>
</tr>
<tr>
<td>Disable boot block rewrite</td>
<td>(\triangle)</td>
<td>(\times)</td>
</tr>
</tbody>
</table>

Same condition as that in flash memory programming mode (on-board/off-board programming)

Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850E/IG3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 6.15 Security Set Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 7.15 Security Set Command.
- For the 3-wire serial I/O communication mode (CSI), read 8.15 Security Set Command.
5.14 Read Command

5.14.1 Description
This command is used to read data from the flash memory of the V850E/IG3.
The write start/end address can be set only in the block start/end address units.

5.14.2 Command frame and status frame
Figure 5-39 shows the format of a command frame for the Read command, and Figure 5-40 shows the status frame for the command.

![Figure 5-39. Read Command Frame (from Programmer to V850E/IG3)](image)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>50H (Read)</td>
<td>SAH</td>
<td>SAM</td>
<td>SAL</td>
</tr>
</tbody>
</table>

**Remark**
SAH, SAM, SAL: Read start address (start address of the block)
EAH, EAM, EAL: Read end address (end address of the block)

![Figure 5-40. Status Frame for Read Command (from V850E/IG3 to Programmer)](image)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (a)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**
ST1 (a): Command reception result

5.14.3 Data frame and status frame
Figure 5-41 shows the format of a frame that includes data to be read, and Figure 5-42 shows the status frame for the data.

![Figure 5-41. Data Frame of Data to Be Read (from Programmer to V850E/IG3)](image)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX/ETB</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>00H to FFH (00H = 256)</td>
<td>Read Data</td>
<td>Checksum</td>
<td>03H/17H</td>
</tr>
</tbody>
</table>

**Remark**
Read Data: Data read from V850E/IG3

![Figure 5-42. Status Frame for Read Data (from V850E/IG3 to Programmer)](image)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>00H to FFH (00H = 256)</td>
<td>ST1 (b)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**
ST1 (b): ACK (06H) or NACK (15H) sent from the programmer for read data
Read the following chapters for details on flowcharts of processing sequences between the programmer and the V850E/IG3, flowcharts of command processing, and sample programs for each communication mode.

- For the UART communication mode, read 6.16 Read Command.
- For the 3-wire serial I/O communication mode with handshake supported (CSI + HS), read 7.16 Read Command.
- For the 3-wire serial I/O communication mode (CSI), read 8.16 Read Command.
CHAPTER 6 UART COMMUNICATION MODE

Each of the symbol (tXX and twXXX) shown in the flowchart in this chapter is the symbol of characteristic item in CHAPTER 9 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS.

For each specified value, refer to CHAPTER 9 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS.
6.1 Command Frame Transmission Processing Flowchart

- Command frame transmission processing
  - Command frame header (SOH = 01H) transmission
    - Wait between data transmissions
    - Data length (LEN) transmission
      - Wait between data transmissions
      - Command number (COM) transmission
        - (LEN - 1) bytes transmitted?
          - Yes
          - Command frame footer (ETX = 03H) transmission
            - End of command frame transmission
          - No
            - Transmits 1-byte command information
              - Wait between data transmissions
              - Checksum data (SUM) transmission
                - Wait between data transmissions
                - Command frame footer (ETX = 03H) transmission
                  - End of command frame transmission
            - Wait between data transmissions

6.2 Data Frame Transmission Processing Flowchart

1. Data frame transmission processing
2. Data frame header (STX = 02H) transmission
3. Wait between data transmissions
4. Data length (LEN) transmission
5. LEN bytes transmitted?
   - Yes: Continue
   - No: Wait between data transmissions
6. Wait between data transmissions
7. Transmits 1-byte data
8. Wait between data transmissions
9. Checksum data (SUM) transmission
10. Wait between data transmissions
11. Last data frame?
    - No: Wait between data transmissions
    - Yes: Continue
12. Transmission of last data frame footer (ETX = 03H)
13. Transmission of footer other than those of last data frame (ETB = 17H)
14. End of data frame transmission
6.3 Data Frame Reception Processing Flowchart
6.4 Reset Command

6.4.1 Processing sequence chart

Reset command processing sequence

Note Do not exceed the retry count for the reset command transmission (up to 16 times).
6.4.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command processing starts (wait time \( t_{com} \)).
<2> The low level is output (data 00H is transmitted at 9,600 bps).
<3> Wait state (wait time \( t_{isl} \)).
<4> The low level is output (data 00H is transmitted at 9,600 bps).
<5> Wait state (wait time \( t_{is2} \)).
<6> The Reset command is transmitted by command frame transmission processing.
<7> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{wto} \)).
<8> The status code is checked.

When ST1 = ACK: Normal completion [A]
When ST1 ≠ ACK: The retry count \( t_{rs} \) is checked.
   The sequence is re-executed from <5> if the retry count is not over.
   If the retry count is over, the processing ends abnormally [B].

6.4.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
| Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
   • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]             | – | The status frame was not received within the specified time. |
6.4.4 Flowchart

Reset command processing

Wait from previous frame reception until next command transmission

Transmits “00” at 9,600 bps

Wait

Transmits “00” at 9,600 bps

Wait

Command frame transmission processing (Reset)

Status frame received?

Yes

Timed out?

Yes

Time-out error [C]

No

Status = ACK?

Yes

Retry count over?

Yes

Abnormal termination [B]

No

Normal completion [A]

No

No

No

Yes

Time-out error [C]
6.4.5 Sample program

The following shows a sample program for Reset command processing.

```c
/* **************************************************
/* * Reset command *
/* **************************************************/
/* [r] u16 ... error code */
/*********************************************************/

u16 fl_ua_reset(void)
{
    u16 rc;
    u32 retry;

    set_uart0_br(BR_9600); // change to 9600bps

    fl_wait(tCOM); // wait
    putc_ua(0x00);  // send 0x00 @ 9600bps

    fl_wait(t12);   // wait
    putc_ua(0x00);  // send 0x00 @ 9600bps

    for (retry = 0; retry < tRS; retry++)
    {
        fl_wait(t2C); // wait

        put_cmd_ua(FL_COM_RESET, 1, fl_cmd_prm); // send RESET command

        rc = get_sfrm_ua(fl_ua_sfrm, tWT0_TO);
        if (rc == FLC_DFTO_ERR) // t.o. ?
            break; // yes // case [C]
        if (rc == FLC_ACK) {
            break; // yes // case [A]
        } else {
            NOP();
        }
        //continue; // case [B] (if exit from loop)
    }

    // switch(rc) {
    //    case FLC_NO_ERR: return rc; break; // case [A]
    //    case FLC_DFTO_ERR: return rc; break; // case [C]
    //    default: return rc; break; // case [B]
    // }

    return rc;
}
```
6.5  Baud Rate Set Command

6.5.1  Processing sequence chart

Baud Rate Set command processing sequence

Note  Do not exceed the retry count for the reset command transmission (up to 16 times).
6.5.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{com} \)).
<2> The Baud Rate Set command is transmitted by command frame transmission processing.
<3> Waits from command transmission until Reset command transmission (wait time \( t_{WT10} \)).
<4> The Reset command is transmitted by command frame transmission processing.
<5> A time-out check is performed from command transmission until status frame reception. If a time-out occurs, a time-out error \([C]\) is returned (time-out time \( t_{WT0} \)).
<6> Since the status code should be ACK, the processing ends normally \([A]\).

6.5.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion ([A])</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination ([B])</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error ([C])</td>
<td>–</td>
<td>Data frame reception was timed out. With the V850E/IG3, this command also results in errors in the following cases.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
6.5.4 Flowchart

Baud Rate Set command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Baud Rate Set)

Wait from command frame transmission until Reset command transmission

Command frame transmission processing (Reset)

Status frame received? No

Normal completion [A]

Yes

Timed out? No

Time-out error [C]

Yes
6.5.5 Sample program
The following shows a sample program for Baud Rate Set command processing.

```c
/* *************************************************************************/
/* */
/* Set baudrate command */
/* */
/* *************************************************************************/
/* [i] u8 brid ... baudrate ID */
/* [r] u16 ... error code */
/* *************************************************************************/

u16 fl_ua_setbaud(u8 brid)
{
    u16 rc;
    u8 br;
    u32 retry;

    switch(brid){
        default: break;
        case BR_9600: br = 0x03; break;
        case BR_19200: br = 0x04; break;
        case BR_31250: br = 0x05; break;
        case BR_38400: br = 0x06; break;
        case BR_76800: br = 0x07; break;
        case BR_153600: br = 0x08; break;
    }
    fl_cmd_prm[0] = br;  // "D01"

    fl_wait(tCOM);  // wait before sending command
    put_cmd_ua(FL_COM_SET_BAUDRATE, 2, fl_cmd_prm);  // send "Baudrate Set" command
    set_flbaud(brid);  // change baud-rate
    set_uart0_br(brid);  // change baud-rate (h.w.)

    retry = tRS;
    while(1){
        fl_wait(tWT10);
        put_cmd_ua(FL_COM_RESET, 1, fl_cmd_prm);  // send RESET command
        rc = get_sfrm_ua(fl_ua_sfrm, tWT0_TO);  // get status frame
        if (rc){
            if (retry--)
                continue;
            else
                return rc;
        }
        break;  // got ACK !
    }

    // switch(rc) {
    //     case FLC_NO_ERR: return rc; break; // case [A]
    //     case FLC_DFTO_ERR: return rc; break; // case [C]
    //     default: return rc; break; // case [B]
    // }

    return rc;
}
```
6.6 Oscillating Frequency Set Command

6.6.1 Processing sequence chart

Chip Erase command processing sequence

Programmer V850E/IG3

<1> Wait from previous frame reception until next command transmission

<2> Chip Erase command frame transmission

<3> Time-out check for status frame reception

<4> Status frame reception

Status frame received within specified time

Time-out error [C]

Time-out occurs

Reception status [ACK/other than ACK]

Other than ACK

ACK

Abnormal termination [B]

Normal completion [A]
6.6.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{COM}} \)).

<2> The Oscillating Frequency Set command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception. If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT9}} \)).

<4> The status code is checked.

When ST1 = ACK: Normal completion [A]
When ST1 ≠ ACK: Abnormal termination [B]

6.6.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
</tbody>
</table>
6.6.4 Flowchart

- Oscillating Frequency Set command processing
- Wait from previous frame reception until next command transmission
  \( t_{com} \)
- Command frame transmission processing (Oscillating Frequency Set)
- Status frame received?
  - Yes
    - Status = ACK?
      - Yes
        - Normal completion [A]
      - No
        - Abnormal termination [B]
  - No
    - Timed out?
      - Yes
        - Time-out error [C]
      - No
        - Status frame received?
### 6.6.5 Sample program

The following shows a sample program for Oscillating Frequency Set command processing.

```c
/****************************************************************************
/* */
/* Set Flash device clock value command */
/* */
/****************************************************************************
/* [i] u8 clk[4] ... frequency data(D1-D4) */
/* [r] u16 ... error code */
/****************************************************************************

u16 fl_ua_setclk(u8 clk[])
{
    u16 rc;

    fl_cmd_prm[0] = clk[0]; // "D01"
    fl_cmd_prm[1] = clk[1]; // "D02"
    fl_cmd_prm[2] = clk[2]; // "D03"
    fl_cmd_prm[3] = clk[3]; // "D04"

    fl_wait(tCOM); // wait before sending command
    put_cmd_ua(FL_COM_SET_OSC_FREQ, 5, fl_cmd_prm);

    rc = get_sfrm_ua(fl_ua_sfrm, tWT9_TO); // get status frame
    // switch(rc) {
    //  case FLC_NO_ERR: return rc; break; // case [A]
    //  case FLC_DFTO_ERR: return rc; break; // case [C]
    //  default: return rc; break; // case [B]
    // }

    return rc;
}
```
6.7 Chip Erase Command

6.7.1 Processing sequence chart

Chip Erase command processing sequence

- **<1>** Wait from previous frame reception until next command transmission
- **<2>** Chip Erase command frame transmission
- **<3>** Time-out check for status frame reception
- **<4>** Status frame reception

Time-out occurs

Status frame received within specified time

- **Time-out error [C]**
- **Status frame received within specified time**
  - **Reception status [ACK/other than ACK]**
    - **Other than ACK**
    - **ACK**
      - **Abnormal termination [B]**
      - **Normal completion [A]**
6.7.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{com}$).

<2> The Chip Erase command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT1}$).

<4> The status code is checked.

   When ST1 = ACK: Normal completion [A]
   When ST1 ≠ ACK: Abnormal termination [B]

6.7.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H The command was executed normally and chip erase was performed normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H The checksum of the transmitted command frame does not match.</td>
</tr>
</tbody>
</table>
| Protection error                      | Protect error | 10H • Chip erase is prohibited in the security setting.  
                                       |                           | • Boot block cluster rewrite is prohibited in the security setting.       |
| Abnormal termination [B]              | Negative acknowledgment (NACK) | 15H Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Abnormal termination [B]              | FLMD error    | 18H An erase error has occurred.                                           |
| Abnormal termination [B]              | Write error   | 1CH                                                                        |
| Abnormal termination [B]              | MRG10 error   | 1AH                                                                        |
| Abnormal termination [B]              | MRG11 error   | 18H                                                                        |
| Abnormal termination [B]              | Time-out error [C] | – The status frame was not received within the specified time.             |
6.7.4 Flowchart

- Chip Erase command processing
- Waits from previous frame reception until next command transmission
- Command frame transmission processing (Chip Erase)
- Status frame received? (Yes/No)
  - No: Timed out? (Yes/No)
    - Yes: Time-out error [C]
    - No: Status = ACK? (Yes/No)
      - Yes: Normal completion [A]
      - No: Abnormal termination [B]
6.7.5 Sample program

The following shows a sample program for Chip Erase command processing.

```c
/******************************************************************
/* Erase all(chip) command */
/******************************************************************
/* [r] u16 ... error code */
/******************************************************************
u16 fl_ua_erase_all(void)
{
    u16 rc;

    fl_wait(tCOM); // wait before sending command
    put_cmd_ua(FL_COM_ERASE_CHIP, 1, fl_cmd_prm); // send ERASE CHIP command
    rc = get_sfrm_ua(fl_ua_sfrm, tWT1_MAX); // get status frame
    // switch(rc) {
    //     case FLC_NO_ERR: return rc; break; // case [A]
    //     case FLC_DFTO_ERR: return rc; break; // case [C]
    //     default: return rc; break; // case [B]
    // }
    return rc;
}
```
6.8 Block Erase Command

6.8.1 Processing sequence chart

Block Erase command processing sequence
6.8.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{com}} \)).

<2> The Block Erase command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception. If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT2}} \)).

<4> The status code is checked.

When \( ST1 = \text{ACK} \): Normal completion [A]
When \( ST1 \neq \text{ACK} \): Abnormal termination [B]

6.8.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
| Protect error                  | 10H | • Block erase is prohibited in the security setting.  
|                                |             | • Boot area is included in the specified range while boot block cluster rewrite is prohibited in the security setting.  
|                                |             | • Chip erase is prohibited in the security setting.  
|                                |             | • Programming is prohibited in the security setting.  |
| Negative acknowledgment (NACK) | 15H | Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| MRG10 error                    | 1AH | An erase error has occurred. |
| Time-out error [C]             | – | The status frame was not received within the specified time. |
6.8.4 Flowchart

Block Erase command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Block Erase)

Status frame received?

Status = ACK?

Abnormal termination [B]

Normal completion [A]

Yes

No

Timed out?

Yes

Time-out error [C]

No

Yes
6.8.5 Sample program
The following shows a sample program for Block Erase command processing for one block.

```c
/*****************************************************************
/* Erase block command */
/*****************************************************************/
/* [i] u16 sblk ... start block to erase (0...255) */
/* [i] u16 eblk ... end block to erase   (0...255) */
/* [r] u16 ... error code */
/**************************************************************************/

u16 fl_ua_erase_blk(u16 sblk, u16 eblk)
{
    u16 rc;
    u32 wt2_max;
    u32 top, bottom;

    top = get_top_addr(sblk);  // get start address of start block
    bottom = get_bottom_addr(eblk);  // get end address of end block

    set_range_prm(fl_cmd_prm, top, bottom);  // set SAH/SAM/SAL, EAH/EAM/EAL
    wt2_max = make_wt2_max(sblk, eblk);  // get tWT2(Max)
    fl_wait(tCOM);  // wait before sending command

    put_cmd_ua(FL_COM_ERASE_BLOCK, 7, fl_cmd_prm);  // send ERASE CHIP command
    rc = get_sfrm_ua(fl_ua_sfrm, wt2_max);  // get status frame

    switch(rc) {
        case FLC_NO_ERR: return rc; break; // case [A]
        case FLC_DFTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

    return rc;
}
```
6.9 Programming Command

6.9.1 Processing sequence chart

Programming command processing sequence

- **<1>** Wait from previous frame reception until next command transmission
- **<2>** Programming command frame transmission
- **<3>** Time-out check for status frame reception
- **<4>** Status frame reception
- **<5>** Wait from previous frame reception until next data frame transmission
- **<6>** Data frame (user data) transmission
- **<7>** Time-out check for status frame reception
- **<8>** Status frame reception
- **<9>** Time-out check for status frame reception
- **<10>** Status frame reception

- **Time-out occurs**
  - **<C>** Abnormal termination
  - **<C>** Time-out error

- **Other than ACK**
  - **<B>** Abnormal termination
  - **<C>** Time-out error
  - **<C>** Time-out error

- **ACK**
  - **<A>** Normal completion

- **Reception status**
  - **[ACK/other than ACK]**
  - **[ACK/other than ACK]**
  - **[ACK/other than ACK]**

- **All data frames transmitted?**
  - **[Yes/No]**

- **Status frame received within specified time**
  - **<D>** Abnormal termination

- **Time-out occurs**
  - **<E>** Time-out error
6.9.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{COM}$).

<2> The Programming command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT3}$).

<4> The status code is checked.

   When ST1 = ACK: Proceeds to <5>.
   When ST1 ≠ ACK: Abnormal termination [B]

<5> Waits from the previous frame reception until the next data frame transmission (wait time $t_{FD3}$).

<6> User data is transmitted by data frame transmission processing.

<7> A time-out check is performed from user data transmission until data frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT4}$).

<8> The status code (ST1/ST2) is checked (also refer to the processing sequence chart and flowchart).

   When ST1 ≠ ACK: Abnormal termination [B]
   When ST1 = ACK: The following processing is performed according to the ST2 value.
      • When ST2 = ACK: Proceeds to <9> when transmission of all data frames is completed.
         If there still remain data frames to be transmitted, the processing re-executes the sequence from <5>.
      • When ST2 ≠ ACK: Abnormal termination [D]

<9> A time-out check is performed until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT5}$).

<10> The status code is checked.

   When ST1 = ACK: Normal completion [A]
   When ST1 ≠ ACK: Abnormal termination [E]
### 6.9.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
</tbody>
</table>
| Abnormal termination [B]        | Parameter error | 05H | • The specified start/end address is not the start/end address of the block.  
• The data length is under 2 words. |
|                                 | Checksum error | 07H | The checksum of the transmitted command frame does not match. |
| Protect error                   | 10H | • Write is prohibited in the security setting.  
• Boot block cluster rewrite is prohibited in the security setting. |
| Negative acknowledgment (NACK)  | 15H | Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]              | – | The status frame was not received within the specified time. |
| Abnormal termination [D]        | Checksum error | 07H | The checksum of the transmitted command frame does not match. |
|                                 | Write error | 1CH (ST2) | A write error has occurred. |
| Abnormal termination [E]        | MRG11 error | 1BH | An internal verify error has occurred. |
6.9.4 Flowchart

- **Programming command processing**
  - Wait for previous frame reception until next command transmission
  - Command frame transmission processing (Programming)
  - Status frame received?
    - Yes: ST1 = ACK?
    - No: Timed out?
      - Yes: Time-out error [C]
      - No: Abnormal termination [B]
  - Status = ACK?
    - Yes: Abnormal termination [B]
    - No: Abnormal termination [E]

- **Data frame transmission processing (User program)**
  - Wait for previous frame reception until next command transmission
  - Status frame received?
    - Yes: ST2 = ACK?
    - No: All data frames transmitted?
      - Yes: Normal completion [A]
      - No: Abnormal termination [E]
  - Status = ACK?
    - Yes: Abnormal termination [B]
    - No: Abnormal termination [D]

- **Status frame received?**
  - Yes: Timed out?
    - Yes: Time-out error [C]
    - No: Abnormal termination [B]
  - No: Abnormal termination [B]
6.9.5 Sample program
The following shows a sample program for Programming command processing.

```c
#define fl_st2_ua (fl_ua_sfrm[OFS_STA_PLD+1])

u16 fl_ua_write(u32 top, u32 bottom)
{
    u16 rc;
    u32 send_head, send_size;
    bool is_end;
    u32 wt5_max;

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL
    wt5_max = make_wt5_max(get_block_num(top, bottom));

    fl_wait(tCOM);  // wait before sending command
    put_cmd_ua(FL_COM_WRITE, 7, fl_cmd_prm); // send "Programming" command
    rc = get_sfrm_ua(fl_ua_sfrm, tWT3_TO); // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }

    send_head = top;
    while(1){
        // make send data frame
        if ((bottom - send_head) > 256){ // rest size > 256 ?
            is_end = false; // yes, not is end frame
            send_size = 256; // transmit size = 256 byte
        }
        else{
            is_end = true;
        }
```
send_size = bottom - send_head + 1;  // transmit size = (bottom - send_head)+1 byte
}
memcpy(fl_txdata_frm, rom_buf+send_head, send_size); // set data frame payload
send_head += send_size;
fl_wait(tFD3);  // wait before sending data frame
put_dfrm_ua(send_size, fl_txdata_frm, is_end); // send user data
rc = get_sfrm_ua(fl_ua_sfrm, tWT4_MAX);  // get status frame
switch(rc) {
    case FLC_NO_ERR:   break; // continue
    case FLC_DFTO_ERR: return rc; break; // case [C]
    default:  return rc; break; // case [B]
}
if (fl_st2_ua != FLST_ACK){ // ST2 = ACK ?
    rc = decode_status(fl_st2_ua); // No
    return rc;    // case [D]
}  
if (is_end)
    break;
}

/*************************************************
/* Check internally verify
 *************************************************/
rc = get_sfrm_ua(fl_ua_sfrm, tWT5_MAX); // get status frame again
switch(rc) {
    case FLC_NO_ERR: return rc;   break; // case [A]
    case FLC_DFTO_ERR: return rc;   break; // case [C]
    default: return rc;   break; // case [E]
}
return rc;
}
6.10 Verify Command

6.10.1 Processing sequence chart

Verify command processing sequence

- **<1>** Wait from previous frame reception until next command transmission
- **<2>** Verify command frame transmission
- **<3>** Time-out check for status frame reception
- **<4>** Status frame reception
- **<5>** Wait from previous frame reception until next data frame transmission
- **<6>** Data frame (user data for verify) transmission
- **<7>** Time-out check for status frame reception
- **<8>** Status frame reception (ST1/ST2)

**Reception status [ACK/other than ACK]**

- **Abnormal termination [B]**
- **Time-out error [C]**
- **Others than ACK**
- **Abnormal termination [B]**
- **Abnormal termination [D]**

- **<5>** Time-out occurs
- **<7>** Status frame received within specified time
- **<8>** Status frame received (ST1/ST2)

**Time-out occurs**

- **<2>** Verify command frame transmission
- **<3>** Time-out check for status frame reception
- **<4>** Status frame reception
- **<6>** Data frame (user data for verify) transmission
- **<7>** Time-out check for status frame reception
- **<8>** Status frame reception (ST1/ST2)

- **<5>** Time-out occurs
- **<7>** Status frame received within specified time
- **<8>** Status frame received (ST1/ST2)

**Reception status (ST1) [ACK/other than ACK]**

- **<6>** Data frame (user data for verify) transmission
- **<7>** Time-out check for status frame reception
- **<8>** Status frame reception (ST1/ST2)

- **<5>** Time-out occurs
- **<7>** Status frame received within specified time
- **<8>** Status frame received (ST1/ST2)

**Reception status (ST2) [ACK/other than ACK]**

- **<6>** Data frame (user data for verify) transmission
- **<7>** Time-out check for status frame reception
- **<8>** Status frame reception (ST1/ST2)

- **<5>** Time-out occurs
- **<7>** Status frame received within specified time
- **<8>** Status frame received (ST1/ST2)

**All data frames transmitted? [Yes/No]**

- **Yes**: Normal completion [A]
- **No**: Go to <5>

**Time-out occurs**

- **<2>** Verify command frame transmission
- **<3>** Time-out check for status frame reception
- **<4>** Status frame reception
- **<6>** Data frame (user data for verify) transmission
- **<7>** Time-out check for status frame reception
- **<8>** Status frame reception (ST1/ST2)

- **<5>** Time-out occurs
- **<7>** Status frame received within specified time
- **<8>** Status frame received (ST1/ST2)

**Time-out occurs**

- **<2>** Verify command frame transmission
- **<3>** Time-out check for status frame reception
- **<4>** Status frame reception
- **<6>** Data frame (user data for verify) transmission
- **<7>** Time-out check for status frame reception
- **<8>** Status frame reception (ST1/ST2)

- **<5>** Time-out occurs
- **<7>** Status frame received within specified time
- **<8>** Status frame received (ST1/ST2)
6.10.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{COM}} \)).

<2> The Verify command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT6}} \)).

<4> The status code is checked.
   
   When ST1 = ACK:  Proceeds to <5>.
   When ST1 \( \neq \) ACK:  Abnormal termination [B]

<5> Waits from the previous frame reception until the next data frame transmission (wait time \( t_{\text{FD3}} \)).

<6> User data for verifying is transmitted by data frame transmission processing.

<7> A time-out check is performed from user data transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT7}} \)).

<8> The status code (ST1/ST2) is checked (also refer to the processing sequence chart and flowchart).

   When ST1 \( \neq \) ACK:  Abnormal termination [B]
   When ST1 = ACK:  The following processing is performed according to the ST2 value.
   
   - When ST2 = ACK:  If transmission of all data frames is completed, the processing ends normally [A].
     If there still remain data frames to be transmitted, the processing re-executes the sequence from <5>.
   - When ST2 \( \neq \) ACK:  Abnormal termination [D]

6.10.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A] Normal acknowledgment (ACK)</td>
<td>06H</td>
<td>The command was executed normally and the verify was completed normally.</td>
</tr>
<tr>
<td>Abnormal termination [B] Parameter error</td>
<td>05H</td>
<td>The specified start/end address is not the start/end address of the block.</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
<tr>
<td>Abnormal termination [D] Checksum error</td>
<td>07H</td>
<td>The checksum of the transmitted command frame or data frame does not match.</td>
</tr>
<tr>
<td></td>
<td>Verify error</td>
<td>0FH (ST2)</td>
</tr>
</tbody>
</table>

Application Note U18897EJ1V0AN
6.10.4 Flowchart

- Verify command processing
- Wait from previous frame reception until next command transmission
- Command frame transmission processing (Verify)
  - Status frame received?
    - Yes
      - Timed out?
        - No
      - ST1 = ACK? (Verify)
        - No
        - Abnormal termination [B]
        - Yes
          - Abnormal termination [B]
    - No
  - Status frame received?
    - Yes
      - Timed out?
        - No
      - ST1 = ACK?
        - No
        - Abnormal termination [B]
        - Yes
          - Abnormal termination [B]
      - ST2 = ACK?
        - No
        - Abnormal termination [D]
        - Yes
          - Abnormal termination [D]
    - No
  - All data frames transmitted?
    - No
      - Timed out?
        - No
      - Status frame received?
        - Yes
          - Timed out?
            - No
          - ST1 = ACK?
            - No
              - Abnormal termination [B]
              - Yes
                - Abnormal termination [B]
            - Yes
              - Abnormal termination [D]
              - ST2 = ACK?
                - No
                  - Abnormal termination [D]
                  - Yes
                    - Normal completion [A]
                - Yes
                  - Normal completion [A]
          - Time-out error [C]
    - Yes
      - Time-out error [C]
6.10.5 Sample program

The following shows a sample program for Verify command processing.

```c
u16 fl_ua_verify(u32 top, u32 bottom, u8 *buf)
{
    u16 rc;
    u32 send_head, send_size;
    bool is_end;

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    fl_wait(tCOM);       // wait before sending command
    put_cmd_ua(FL_COM_VERIFY, 7, fl_cmd_prm); // send VERIFY command

    rc = get_sfrm_ua(fl_uasfrm, tWT6_TO);    // get status frame
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        default: return rc; break; // case [B]
    }

    while(1) {
        // make send data frame
        if ((bottom - send_head) > 256){ // rest size > 256 ?
            is_end = false;               // yes, not is_end frame
            send_size = 256;              // transmit size = 256 byte
        }
        else{
            is_end = true;
            send_size = bottom - send_head + 1;
            // transmit size = (bottom - send_head)+1 byte
```
memcpy(fl_txdata_frm, buf+send_head, send_size); // set data frame payload
send_head += send_size;

fl_wait(tFD3_UA);
put_dfrm_ua(send_size, fl_txdata_frm, is_end); // send user data

rc = get_sfrm_ua(fl_ua_sfrm, tWT7_MAX);   // get status frame
switch(rc) {
    case FLC_NO_ERR:   break; // continue
    case FLC_DFTO_ERR: return rc; break; // case [C]
    default:  return rc; break; // case [B]
}

if (fl_st2_ua != FLST_ACK){  // ST2 = ACK ?
    rc = decode_status(fl_st2_ua); // No
    return rc;    // case [D]
}

if (is_end)   // send all user data ?
    break;   // yes
    //continue;

return FLC_NO_ERR;   // case [A]
}
6.11 Block Blank Check Command

6.11.1 Processing sequence chart

Block Blank Check command processing sequence

Programmer

<1> Wait from previous frame reception until next command transmission

<2> Block Blank Check command frame transmission

<3> Time-out check for status frame reception

Status frame received within specified time

<4> Status frame reception

V850E/IG3

Time-out error [C]

Reception status [ACK/other than ACK]

Other than ACK

Abnormal termination [B]

ACK

Normal completion [A]
6.11.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{COM}} \)).

<2> The Block Blank Check command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.

If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT8}} \)).

<4> The status code is checked.

When \( ST1 = \text{ACK} \): Normal completion [A]

When \( ST1 \neq \text{ACK} \): Abnormal termination [B]

6.11.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
</tbody>
</table>
| Abnormal termination [B]        | Parameter error | 05H | • The specified start/end address is out of the flash memory range.  

• The specified start/end address is not the start/end address of the block. |
| Checksum error                  | 07H | The checksum of the transmitted command frame does not match. |
| Negative acknowledgment (NACK)  | 15H | Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| MRG11 error                     | 1BH | The specified block in the flash memory is not blank. |
| Time-out error [C]              | – | The status frame was not received within the specified time. |
6.11.4 Flowchart

```
Block Blank Check command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Block Blank Check)

Status frame received?

Yes

Status = ACK?

Yes

Normal completion [A]

No

Timed out?

Yes

Time-out error [C]

No

Abnormal termination [B]

No

No Yes


t_\text{com}


t_\text{WTS}

```
6.11.5 Sample program

The following shows a sample program for Block Blank Check command processing for one block.

```c
/*******************************/
/* */
/* Block blank check command */
/* */
/*******************************/
/* [i] u16 sblk ... start block number */
/* [i] u16 eblk ... end block number */
/* [r] u16 ... error code */
/*******************************/

u16 fl UA_blk_blank_chk(u16 sblk, u16 eblk)
{
    u16 rc;
    u32 wt8_max;
    u32 top, bottom;

    top = get_top_addr(sblk); // get start address of start block
    bottom = get_bottom_addr(eblk); // get end address of end block
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    wt8_max = make_wt8_max(sblk, eblk); // get tWT8(Max)

    fl_wait(tCOM); // wait before sending command

    put_cmd_ua(FL_COM_BLOCK_BLANK_CHK, 7, fl_cmd_prm);
    rc = get_sfrm_ua(fl UA_sfrm, wt8_max); // get status frame
    switch(rc) {
        case FLC_NO_ERR: return rc; break; // case [A]
        case FLC_DFTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }
    return rc;
}
```
6.12 Silicon Signature Command

6.12.1 Processing sequence chart

Silicon Signature command processing sequence

- **Time-out error [C]**
- **Abnormal termination [B]**
- **Normal data frame? [Yes/No]**
- **Normal completion [A]**
- **Data frame error [D]**

**Processing sequence chart**:

1. Wait from previous frame reception until next command transmission
2. Silicon Signature command frame transmission
3. Time-out check for status frame reception
4. Status frame reception
5. Time-out check for data frame reception
6. Data frame (silicon signature) reception processing
6.12.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{com} \)).

<2> The Silicon Signature command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT} \)).

<4> The status code is checked.
   - When \( ST1 = \text{ACK} \): Proceeds to <5>.
   - When \( ST1 \neq \text{ACK} \): Abnormal termination [B]

<5> A time-out check is performed until data frame (silicon signature data) reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{FD} \)).

<6> The received data frame (silicon signature data) is checked.
   - If data frame is normal: Normal completion [A]
   - If data frame is abnormal: Data frame error [D]

6.12.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>The command was executed normally and the silicon signature was acquired normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>07H</td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td></td>
<td>15H</td>
<td>Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame or data frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as silicon signature data does not match.</td>
</tr>
</tbody>
</table>
6.12.4 Flowchart

- Silicon Signature command processing
- Wait from previous frame reception until next command transmission $t_{com}$
- Command frame transmission processing (Silicon Signature)
- Status frame received?
  - Yes
    - Status = ACK?
      - Yes
        - Abnormal termination [B]
      - No
        - Data frame (silicon signature) received?
          - Yes
            - Normal data frame?
              - Yes
                - Normal completion [A]
              - No
                - Data frame error [D]
          - No
            - Timed out?
              - Yes
                - Time-out error [C]
              - No
                - Normal completion [A]
- No
  - Timed out?
    - Yes
      - Time-out error [C]
    - No
      - Normal completion [A]
6.12.5 Sample program

The following shows a sample program for Silicon Signature command processing.

```c
u16 fl_ua_getsig(u8 *sig)
{
    u16 rc;

    fl_wait(tCOM); // wait before sending command

    put_cmd_ua(FL_COM_GET_SIGNATURE, 1, fl_cmd_prm); // send GET SIGNATURE command

    rc = get_sfrm_ua(fl_ua_sfrm, tWT11_TO);  // get status frame
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

    rc = get_dfrm_ua(fl_rxdata_frm, tFD2_TO); // get status frame
    if (rc){ // if error
        return rc; // case [D]
    }

    memcpy(sig, fl_rxdata_frm+OFS_STA_PLD, fl_rxdata_frm[OFS_LEN]); // copy Signature data
    return rc; // case [A]
}
```
6.13 Version Get Command

6.13.1 Processing sequence chart

Version Get command processing sequence

Programmer

V850E/IG3

<1> Wait from previous frame reception until next command transmission 

<2> Version Get command frame transmission

<3> Time-out check for status frame reception

<4> Status frame reception

Reception status [ACK/other than ACK]

ACK

<5> Time-out check for data frame reception

<6> Data frame (version data) reception

Data frame received within specified time

Time-out occurs

Other than ACK

Abnormal termination [B]

Time-out error [C]

Normal data frame? [Yes/No]

No

Data frame error [D]

Yes

Normal completion [A]

Time-out occurs

Time-out error [C]
6.13.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{com}$).
<2> The Version Get command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT12}$).
<4> The status code is checked.

   When $ST1 = ACK$: Proceeds to <5>.
   When $ST1 \neq ACK$: Abnormal termination [B]

<5> A time-out check is performed until data frame (version data) reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{FD2}$).
<6> The received data frame (version data) is checked.

   If data frame is normal: Normal completion [A]
   If data frame is abnormal: Data frame error [D]

6.13.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame or data frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as version data does not match.</td>
</tr>
</tbody>
</table>
6.13.4 Flowchart

- **Version Get command processing**
- **Wait from previous frame reception until next command transmission**
- **Command frame transmission processing (Version Get)**
- **Status frame received?**
  - Yes: **Status = ACK?**
    - Yes: **Normal completion [A]**
    - No: **Abnormal termination [B]**
  - No:** Data frame (version data) received?**
    - Yes:** Normal data frame?**
      - Yes: **Normal completion [A]**
      - No:** Data frame error [D]**
    - No:** Timed out?**
      - Yes: **Time-out error [C]**
      - No: **Abnormal termination [B]**
6.13.5 Sample program

The following shows a sample program for Version Get command processing.

```c
u16  fl_ua_getver(u8 *buf)
{
  u16   rc;

  fl_wait(tCOM); // wait before sending command

  put_cmd_ua(FL_COM_GET_VERSION, 1, fl_cmd_prm); // send GET VERSION command

  rc = get_sfrm_ua(fl_ua_sfrm, tWT12_TO); // get status frame
  switch(rc) {
      case FLC_NO_ERR:   break; // continue
  //   case FLC_DFTO_ERR: return rc; break; // case [C]
      default:  return rc; break; // case [B]
  }

  rc = get_dfrm_ua(fl_rxdata_frm, tFD2_TO); // get data frame
  if (rc){
      return rc; // case [D]
  }

  memcpy(buf, fl_rxdata_frm+OFS_STA_PLD, DFV_LEN); // copy version data
  return rc; // case [A]
}
```
6.14 Checksum Command

6.14.1 Processing sequence chart

Checksum command processing sequence
6.14.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{\text{com}}$).

<2> The Checksum command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
    If a time-out occurs, a time-out error [C] is returned (time-out time $t_{\text{wt16}}$).

<4> The status code is checked.

    When ST1 = ACK: Proceeds to <5>.
    When ST1 $\neq$ ACK: Abnormal termination [B]

<5> A time-out check is performed until data frame (checksum data) reception.
    If a time-out occurs, a time-out error [C] is returned (time-out time $t_{\text{fd1}}$).

<6> The received data frame (checksum data) is checked.

    If data frame is normal: Normal completion [A]
    If data frame is abnormal: Data frame error [D]

6.14.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame or data frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as version data does not match.</td>
</tr>
</tbody>
</table>
6.14.4 Flowchart

- Checksum command processing
- Wait from previous frame reception until next command transmission
- Command frame transmission processing (Checksum)
- Status frame received?
  - Yes
    - Status = ACK?
      - Yes
        - Normal completion [A]
      - No
        - Data frame (checksum data) received?
          - Yes
            - Normal data frame?
              - Yes
                - Normal completion [A]
              - No
                - Data frame error [D]
          - No
            - Abnormal termination [B]
- Timed out?
  - Yes
    - Time-out error [C]
  - No

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6.14.5 Sample program

The following shows a sample program for Checksum command processing.

```c
u16 fl_ua_getsum(u16 *sum, u32 top, u32 bottom)
{
    u16 rc;
    u32 fd1_max;

    // set params
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL
    fd1_max = get_fd1_max(get_block_num(top, bottom)); // get tFD1(MAX)

    // send command
    fl_wait(tCOM); // wait before sending command
    put_cmd_ua(FL_COM_GET_CHECK_SUM, 7, fl_cmd_prm); // send GET CHECKSUM command

    rc = get_sfrm_ua(fl_uasfrm, tWT16_TO); // get status frame
    switch(rc) {
        case FLC_NO_ERR:-break; // continue
        case FLC_DFTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

    // get data frame (Checksum data)
    rc = get_dfrm_ua(fl_rxdata_frm, fd1_max); // get status frame
    if (rc){
        return rc; // case [D]
    }

    *sum = (fl_rxdata_frm[OFS_STA_PLD] << 8) + fl_rxdata_frm[OFS_STA_PLD+1]; // set SUM data
    return rc; // case [A]
}
```
6.15 Security Set Command

6.15.1 Processing sequence chart

Security Set command processing sequence
6.15.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{COM}$).

<2> The Security Set command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT13}$).

<4> The status code is checked.
   When ST1 = ACK: Proceeds to <5>.
   When ST1 ≠ ACK: Abnormal termination [B]

<5> Waits from the previous frame reception until the next data frame transmission (wait time $t_{FD3}$).

<6> The data frame (security setting data) is transmitted by data frame transmission processing.

<7> A time-out check is performed until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT14}$).

<8> The status code is checked.
   When ST1 = ACK: Proceeds to <9>.
   When ST1 ≠ ACK: Abnormal termination [D]

<9> A time-out check is performed until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT15}$).

<10> The status code is checked.
    When ST1 = ACK: Normal completion [A]
    When ST1 ≠ ACK: Abnormal termination [E]

6.15.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
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</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Abnormal termination [D]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
| | Protect error | 10H | • An attempt was made to enable a flag that was already prohibited in the setting.  
| | | | • An attempt was made to change the last block number of the boot cluster in the state that boot block cluster rewrite is prohibited. |
| | MGR10 error | 1AH | A write error has occurred. |
| | Write error | 1CH | |
| Abnormal termination [E] | MRG11 error | 1BH | An internal verify error has occurred. |
6.15.4 Flowchart

- Security Set command processing

  Wait from previous frame reception until next command transmission

  Command frame transmission processing (Security Set)

  Status frame received? No

  Status = ACK? Yes

  timer

  Yes

  Status frame received? No

  Status = ACK? Yes

  timer

  Abnormal termination [B]

  Data frame transmission processing (Security data)

  Status frame received? No

  Status = ACK? Yes

  timer

  Abnormal termination [D]

  Status frame received? No

  Status = ACK? Yes

  timer

  Abnormal termination [E]

  Abnormal termination [A]

  Normal completion [A]

  Time-out error [C]

  Time-out error [C]

  Time-out error [C]

  Time-out error [C]
6.15.5 Sample program

The following shows a sample program for Security Set command processing.

```c
u16 fl_ua_setscf(u8 scf, u8 bot)
{
    u16 rc;
    /*******************************************************************************/
    /* set params */
    /*******************************************************************************/
    fl_cmd_prm[0] = 0x00;   // "BLK" (must be 0x00)
    fl_cmd_prm[1] = 0x00;   // "PAG" (must be 0x00)
    fl_txdata_frm[0] = scf|= 0b11100000; // "FLG" (bit 7,6,5,4 must be '1')
    fl_txdata_frm[1] = bot;   // "BOT"
    /*******************************************************************************/
    /* send command */
    /*******************************************************************************/
    fl_wait(tCOM);  // wait before sending command
    put_cmd_ua(FL_COM_SET_SECURITY, 3, fl_cmd_prm);
    rc = get_sfrm_ua(fl_ua_sfrm, tWT13_TO);  // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }
    /*******************************************************************************/
    /* send data frame (security setting data) */
    /*******************************************************************************/
    fl_wait(tFD3);
    put_dfrm_ua(2, fl_txdata_frm, true);    // send security setting data
    rc = get_sfrm_ua(fl_ua_sfrm, tWT14_MAX);  // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }
```
rc = get_sfrm_uaa(f1_uaa_sfrm, tWT15_MAX);   // get status frame
  switch(rc) {
    //
    //   case FLC_NO_ERR: return rc; break; // case [A]
    //   case FLC_DFTO_ERR: return rc; break; // case [C]
    //   default: return rc; break; // case [B]
    //
    return rc;
  }
6.16 Read Command

6.16.1 Processing sequence chart
6.16.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{cwa}} \)).

<2> The Read command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT17}} \)).

<4> The status code is checked.

   When ST1 = ACK:   Proceeds to <5>.
   When ST1 \( \neq \) ACK:   Abnormal termination [B]

<5> A time-out check is performed until reception of the data frame reception result (user data).
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT18}} \)).

<6> The received data frame is checked.

   If data frame is normal:   Proceeds to <9>.
   If data frame is abnormal: Proceeds to <7>.

<7> Waits from the previous frame reception until the next status (NACK) frame transmission (wait time \( t_{\text{WT19}} \)).

<8> The NACK frame is transmitted by data frame transmission processing.
   \( \rightarrow \) A data frame error [D] is returned.

<9> Waits from the previous frame reception until the next status (ACK) frame transmission (wait time \( t_{\text{WT19}} \)).

<10> The ACK frame is transmitted by data frame transmission processing.

   When reception of all data frames is completed, normal completion [A] is returned.
   If there still remain data frames to be received, the processing re-executes the sequence from <5>.

6.16.3 Status at processing completion

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<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame or data frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as read data does not match.</td>
</tr>
</tbody>
</table>
6.16.4 Flowchart

```
6.16.4 Flowchart

Read command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Read)

Status frame received?

No

Yes

ST1 = ACK?

No

Yes

Time-out error [C]

Abnormal termination [B]

Data frame (user program) reception processing

Data frame received?

No

Yes

Data frame reception error?

No

Yes

Wait from previous frame reception until next data frame transmission

Status (NACK) frame transmission

Data frame error [D]

Wait from previous frame reception until next data frame transmission

Status (NACK) frame transmission

All data frames received?

No

Yes

Normal completion [A]
```
6.16.5 Sample program

The following shows a sample program for Read command processing.

```c
u16 fl_ua_read(u32 top, u32 bottom)
{
    u16 rc;
    u32 read_head;
    u16 len;
    u8 hooter;

    /*****************************************************************
    /* set params */
    /*****************************************************************/
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    /*****************************************************************
    /* send command & check status */
    /*****************************************************************/
    fl_wait(tCOM); // wait before sending command
    put_cmd_ua(FL_COM_READ, 7, fl_cmd_prm);

    rc = get_sfrm_ua(fl_uasfrm, tWT17_TO); // get status frame
    switch(rc) {
        case FLC_NO_ERR: break;
        case FLC_RX_DFSUM_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

    /*****************************************************************
    /* receive user data */
    /*****************************************************************/
    read_head = top;

    while(1){
        rc = get_dfrm_ua(fl_rxdata_frm, tWT18_TO); // get ROM data from FLASH
        switch(rc) {
            case FLC_NO_ERR: break; // continue
            case FLC_DFTO_ERR: return rc; break; // case [C]
            case FLC_RX_DFSUM_ERR: break; // case [B]
            default: fl_wait(tWT19); // case [B]

            fl_wait(tWT19);
            fl_wait(5000);
            put_sfrm_ua(FLST_NACK); // send status(NACK) frame
            return rc;
        }
    }
}
```
} 
fl_wait(tWT19);
// fl_wait(5000);
put_sfrm_uu(FLST_ACK);

/* save ROM data */
if ((len = fl_rxdata_frm[OFS_LEN]) == 0) // get length
    len = 256;

memcpw(read_buf+read_head, fl_rxdata_frm+2, len); // save to external RAM
read_head += len;

/* end check */
hoster = fl_rxdata_frm[len + 3];
if (hoster == FL_ETB) // end frame ?
    continue; // no
break; // yes

return FLC_NO_ERR;
}
CHAPTER 7  3-WIRE SERIAL I/O COMMUNICATION MODE WITH HANDSHAKE SUPPORTED (CSI + HS)

Each of the symbol (txx and twtxx) shown in the flowchart in this chapter is the symbol of characteristic item in CHAPTER 9 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS.

For each specified value, refer to CHAPTER 9 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS.
7.1 Command Frame Transmission Processing Flowchart
7.2 Data Frame Transmission Processing Flowchart

Data frame transmission processing

Data frame header (STX = 02H) transmission

HS pin = BUSY?

Yes

Timed out?

No

Data length (LEN) transmission

LEN byte transmitted?

Yes

No

Transmit 1-byte data

HS pin = BUSY?

Yes

Timed out?

No

checksum data (SUM) transmission

HS pin = BUSY?

Yes

Timed out?

No

Last data frame?

No

Yes

Transmission of last data frame footer (ETX = 03H)

Transmission of footer other than those of last data frame (ETS = 17H)

End of data frame transmission

No
7.3 Data Frame Reception Processing Flowchart

Data frame reception processing

Data frame header (STX = 02H) reception

HS pin = BUSY?
Yes
No

Timed out?
Yes
No

Reception time-out error

Data length (LEN) reception

HS pin = BUSY?
Yes
No

Receives 1-byte data

HS pin = BUSY?
Yes
No

Timed out?
Yes
No

Ending of data frame reception

LEN bytes received?
Yes
No

Checksum data (SUM) reception

HS pin = BUSY?
Yes
No

Timed out?
Yes
No

Reception time-out error

Checksum error?
Yes
No

Checksum error

End of data frame reception
7.4 Status Command

7.4.1 Processing sequence chart

Status command processing sequence

Programmer V850E/IG3

<1> Status command frame transmission

<2> BUSY time-out check using HS pin

<3> Status frame reception

Time-out error [C]

BUSY release

Reception status [ACK/other than ACK]

Other than ACK

ACK

Abnormal termination [B]

Normal completion [A]
7.4.2 Description of processing sequence

<1> The Status command is transmitted by command frame transmission processing.
<2> A V850E/IG3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{SF}$).
<3> The status code is checked.

When ST1 = ACK: Normal completion [A]
When ST1 ≠ ACK: Abnormal termination [B]

7.4.3 Status at processing completion

<table>
<thead>
<tr>
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<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Command error</td>
<td>04H</td>
</tr>
<tr>
<td></td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Verify error</td>
<td>0FH</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
<tr>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
<td>Negative acknowledgment</td>
</tr>
<tr>
<td>FLMD error</td>
<td>18H</td>
<td>A write error has occurred.</td>
</tr>
<tr>
<td>MRG10 error</td>
<td>1AH</td>
<td>An erase error has occurred.</td>
</tr>
<tr>
<td>MRG11 error</td>
<td>1BH</td>
<td>An internal verify error has occurred during data write, or a blank check error has occurred.</td>
</tr>
<tr>
<td>Write error</td>
<td>1CH</td>
<td>A write error has occurred.</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
</tbody>
</table>
7.4.4 Flowchart

Status command processing

Command frame transmission processing (Status)

HS pin = BUSY?

Yes

HS timed out?

Yes

Time-out error [C]

No

Status frame reception processing

Status = ACK?

No

Abnormal termination [B]

Yes

Normal completion [A]

No

Yes

Normal completion [A]

Abnormal termination [B]
7.4.5 Sample program

The following shows a sample program for Status command processing.

```c
/* *******************************************************************/
/* *                                                               */
/* *  Get status command (CSI-HS)                                  */
/* *                                                               */
/* *******************************************************************/
/* [r] u16       ... decoded status or error code */
/* *                                                               */
/* * (see fl.h/fl-proto.h &                                        */
/* *       definition of decode_status() in fl.c)                  */
/* *******************************************************************/
static u16 fl_hs_getstatus(void)
{
    u16 rc;
    u32 retry = 0;

    rc = put_cmd_hs(FL_COM_GET_STA, 1, fl_cmd_prm);  // send "Status" command
    if (rc)
        return rc;  // case [C]

    if (hs_busy_to(tSF_TO))  // HS-Busy t.o. ?
        return FLC_HSTO_ERR;  // t.o. detected : case [C]

    if (rc = get_sfrm_hs(fl_rxdata_frm))
        return rc;  // case [C] or [B(checksum error)]

    rc = decode_status(fl_st1);  // decode return code
    return rc;  // case [A] or [B]
}
```
7.5 Reset Command

7.5.1 Processing sequence chart

Reset command processing sequence

Note  Do not exceed the retry count for the reset command transmission (up to 16 times).
7.5.2 Description of processing sequence

<1> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{com}} \)).

<2> The Reset command is transmitted by command frame transmission processing.

<3> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{wto}} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

   When the processing ends normally: Normal completion [A]
   When the processing ends abnormally: The sequence is re-executed from <1> if the retry count is not over.
   If the retry count is over, the processing ends abnormally [B].
   When a time-out error occurs: A time-out error [C] is returned.

7.5.3 Status at processing completion

<table>
<thead>
<tr>
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<th>Status Code</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>Normal completion [A]</td>
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<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|                                 | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
                                 |                                      |   | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]              | –           | Status check processing timed out.  
                                 |                                      |   | Processing timed out due to the busy status at the HS pin. |
7.5.4 Flowchart

Reset command processing

HS pin = BUSY?

Yes

Command frame transmission processing (Reset)

HS timed out?

Yes
t_{C_{OM}}

Time-out error [C]

Yes

HS timed out?

No

No

Status check processing

Result of status check processing = Abnormal termination?

Yes

No

Retry count over?

Yes

Abnormal termination [B]

No

Result of status check processing = Time-out error?

Yes

No (normal completion)

Normal completion [A]

Time-out error [C]
7.5.5 Sample program

The following shows a sample program for Reset command processing.

```c
u16  fl_hs_reset(void)
{
    u16  rc;
    u32 retry;

    for (retry = 0; retry < tRS; retry++){

        if (hs_busy_to(tCOM_TO))
            return FLC_HSTO_ERR;  // t.o. detected :case [C]

        rc = put_cmd_hs(FL_COM_RESET, 1, fl_cmd_prm); // send "Reset" command
        if (rc)
            return rc;  // case [C]

        if (hs_busy_to(tWT0_TO))
            return FLC_HSTO_ERR;  // t.o. detected :case [C]

        rc = fl_hs_getstatus();  // get status frame
        if (rc == FLC_ACK)  // ST1 = ACK ?
            break;  // case [A]
        //continue;  // case [B] (if exit from loop)

    }

    switch(rc) {
    //  case FLC_NO_ERR: return rc;  break;  // case [A]
    //  case FLC_HSTO_ERR: return rc;  break;  // case [C]
    //  default:  return rc;  break;  // case [B]
    // }
    return rc;
}
```
CHAPTER 7 3-WIRE SERIAL I/O COMMUNICATION MODE WITH HANDSHAKE SUPPORTED (CSI + HS)

7.6 Oscillating Frequency Set Command

7.6.1 Processing sequence chart

Oscillating Frequency Set command processing sequence

Programmer

<tCOM>
BUSY time-out check using HS pin

<2> Oscillating Frequency Set command frame transmission

<3> BUSY time-out check using HS pin

Result [Normal completion/ Abnormal termination/ Time-out error]

Time-out error

Normal completion

Abnormal termination

Normal completion [A]

Abnormal termination [B]

Result of status check processing

<4> Status check processing

<5> Result of status check processing

V850E/IG3

Time-out error [C]

Time-out error [C]

Time-out occurs

BUSY release

Time-out occurs

<1> Status check processing

<5> Result of status check processing
7.6.2 Description of processing sequence

<1> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{com}} \)).

<2> The Oscillating Frequency Set command is transmitted by command frame transmission processing.

<3> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{HS}} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

   When the processing ends normally: Normal completion [A]
   When the processing ends abnormally: Abnormal termination [B]
   When a time-out error occurs: A time-out error [C] is returned.

7.6.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H The command was executed normally and the operating frequency was correctly set to the V850E/IG3.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H The oscillation frequency value is out of range.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Negative acknowledgment (NACK)</td>
<td>15H Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
</tbody>
</table>
7.6.4 Flowchart

- Oscillating Frequency Set command processing
- HS pin = BUSY?
  - Yes
    - Timed out?
      - Yes
        - Time-out error [C]
      - No
    - No
  - No
    - Command frame transmission processing (Oscillating Frequency Set)
    - HS pin = BUSY?
      - Yes
        - Timed out?
          - Yes
            - Time-out error [C]
          - No
    - No
    - Status check processing
      - Yes
        - Timed out?
          - Yes
            - Time-out error [C]
          - No
      - No
        - Time-out error?
          - Yes
            - Time-out error [C]
          - No
    - Normal completion?
      - Yes
        - Normal completion [A]
      - No
        - Abnormal termination [B]
7.6.5 Sample program

The following shows a sample program for Oscillating Frequency Set command processing.

```c
/**************************************************************************
/*                                                               */
/* Set Flash device clock value command (CSI-HS)               */
/*                                                               */
/**************************************************************************
/* [i] u8 clk[4] ... frequency data(D1-D4)                     */
/* [r] u16        ... error code                                */
/**************************************************************************
/**************************************************************************
u16  fl_hs_setclk(u8 clk[])  
{  
  u16  rc;

  fl_cmd_prm[0] = clk[0];  // "D01"
  fl_cmd_prm[1] = clk[1];  // "D02"
  fl_cmd_prm[2] = clk[2];  // "D03"
  fl_cmd_prm[3] = clk[3];  // "D04"

  if (hs_busy_to(tCOM_TO))
    return FLC_HSTO_ERR;  // t.o. detected :case [C]

  if (rc = put_cmd_hs(FL_COM_SET_OSC_FREQ, 5, fl_cmd_prm))
    return rc;  // case [C]

  if (hs_busy_to(tWT9_TO))
    return FLC_HSTO_ERR;  // t.o. detected :case [C]

  rc = fl_hs_getstatus();  // get status frame
  // switch(rc) {
    //  case FLC_NO_ERR: return rc;  break;  // case [A]
    //  case FLC_HSTO_ERR: return rc;  break;  // case [C]
    //  default:         return rc;  break;  // case [B]
    //  }
  return rc;
}
```
7.7 Chip Erase Command

7.7.1 Processing sequence chart

Chip Erase command processing sequence
7.7.2 Description of processing sequence

<1> A V850E/IG3 BUSY status is checked using the HS pin. If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{com} \)).

<2> The Chip Erase command is transmitted by command frame transmission processing.

<3> A V850E/IG3 BUSY status is checked using the HS pin. If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT1} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

When the processing ends normally: Normal completion [A]

When the processing ends abnormally: Abnormal termination [B]

When a time-out error occurs: A time-out error [C] is returned.

7.7.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK) 06H</td>
<td>The command was executed normally and chip erase was performed normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error 07H</td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
</tbody>
</table>
|                                | Protect error 10H | • Chip erase is prohibited in the security setting.  
                                |                       | • Boot block rewrite is prohibited in the security setting. |
|                                | Negative acknowledgment (NACK) 15H | Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
|                                | FLMD error 18H | An erase error has occurred. |
|                                | Write error 1CH | |
|                                | MRG10 error 1AH | |
|                                | MRG11 error 1BH | |
| Time-out error [C]             | –            | Processing timed out due to the busy status at the HS pin. |
7.7.4 Flowchart

Chip Erase command processing

HS pin = BUSY?

Yes

Timed out?

Yes

Time-out error [C]

No

Command frame transmission processing (Chip Erase)

HS pin = BUSY?

Yes

Timed out?

Yes

Time-out error [C]

No

Status check processing

HS pin = BUSY?

Yes

Timed out?

Yes

Time-out error [C]

No

Time-out error?

Yes

Time-out error [C]

No

Normal completion?

Yes

Normal completion [A]

No

Abnormal termination [B]
7.7.5 Sample program

The following shows a sample program for Chip Erase command processing.

```c
ul6 fl_hs_erase_all(void)
{
    ul6 rc;

    if (hs_busy_to(tCOM_TO))
        return FLC_HSTO_ERR;  // t.o. detected

    if (rc = put_cmd_hs(FL_COM_ERASE_CHIP, 1, fl_cmd_prm))
        // send "Chip Erase" command
        return rc;  // case [C]

    if (hs_busy_to(tWT1_TO))
        return FLC_HSTO_ERR;  // case [C]

    rc = fl_hs_getstatus();  // get status frame
    // switch(rc) {
    //     case FLC_NO_ERR: return rc; break; // case [A]
    //     case FLC_HSTO_ERR: return rc; break; // case [C]
    //     default: return rc; break; // case [B]
    // }
    return rc;
}
```
7.8 Block Erase Command

7.8.1 Processing sequence chart

Block Erase command processing sequence

Programmer

V850E/IG3

<1> BUSY time-out check using HS pin

BUSY release

<2> Block Erase command frame transmission

BUSY release

<3> BUSY time-out check using HS pin

<4> Status check processing

<5> Result of status check processing

Result
[Normal completion/ Abnormal termination/ Time-out error]

Normal completion

Erasure of specified blocks completed? [Yes/No]

Yes

Normal completion [A]

No

Time-out error [C]

Abnormal termination

Abnormal termination [B]

Time-out error

Time-out occurs

BUSY release

Time-out occurs

BUSY release

Time-out occurs

Time-out error [C]

Time-out error [C]
7.8.2 Description of processing sequence

<1> A V850E/IG3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{com}} \)).

<2> The Block Erase command is transmitted by command frame transmission processing.

<3> A V850E/IG3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT2}} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

When the processing ends normally: Normal completion [A]
When the processing ends abnormally: Abnormal termination [B]
When a time-out error occurs: A time-out error [C] is returned.

7.8.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|                                | Protect error | 10H | • Block erase is prohibited in the security setting.  
                                |                |          | • The boot area is included in the specified range while boot block rewrite is prohibited in the security setting.  
                                |                |          | • Chip erase is prohibited in the security setting.  
                                |                |          | • Programming is prohibited in the security setting. |
|                                | Negative acknowledgment (NACK) | 15H | Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
|                                | MRG10 error | 1AH | An erase error has occurred. |
| Time-out error [C]             | – | Processing timed out due to the busy status at the HS pin. |
7.8.4 Flowchart

Block Erase command processing

HS pin = BUSY?
Yes

Command frame transmission processing (Block Erase)

HS pin = BUSY?
Yes

Status check processing

Time-out error?
Yes

Erasure of specified blocks completed?
No

Abnormal termination [B]

Normal completion?
Yes

Normal completion [A]

Time-out error [C]

Timed out?
Yes

No

Time-out error [C]

Timed out?
No

Time-out error [C]

Timed out?
Yes

No

Time-out error [C]
7.8.5 Sample program

The following shows a sample program for Block Erase command processing for one block.

```c
/*****************************************************************
/* */
/* Erase block command (CSI-HS) */
/* */
/***************************************************************************/
/* [i] u16 sblk ... start block number */
/* [i] u16 eblk ... end block number */
/* [r] u16 ... error code */
/***************************************************************************/

u16 fl hs erase_blk(u16 sblk, u16 eblk)
{
    u16 rc;
    u32 wt2_max;

    u32 top, bottom;
    top = get_top_addr(sblk); // get start address of start block
    bottom = get_bottom_addr(eblk); // get end address of end block

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL
    wt2_max = make_wt2_max(sblk, eblk); // get tWT2(Max)

    if (hs_busy_to(tCOM_TO))
        return FLC_HSTO_ERR; // t.o. detected :case [C]

    if (rc = put_cmd_hs(FL_COM_ERASE_BLOCK, 7, fl_cmd_prm))
        return rc; // case [C]

    if (hs_busy_to(wt2_max))
        return FLC_HSTO_ERR; // t.o. detected :case [C]

    rc = fl hs getstatus(); // get status frame
    switch(rc) {
        case FLC_NO_ERR: return rc; break; // case [A]
        case FLC_HSTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }
    return rc;
}
```
7.9 Programming Command

7.9.1 Processing sequence chart

Programming command processing sequence

Programmer V850E/IG3
7.9.2 Description of processing sequence

<1> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{COM}} \)).

<2> The Programming command is transmitted by command frame transmission processing.

<3> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT3}} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.
   When the processing ends normally: Proceeds to <6>.
   When the processing ends abnormally: Abnormal termination [B]
   When a time-out error occurs: A time-out error [C] is returned.

<6> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{FD3}} \)).

<7> User data is transmitted by data frame transmission processing.

<8> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT4}} \)).

<9> The status frame is acquired by status check processing.

<10> The following processing is performed according to the result of status check processing (status code (ST1/ST2)) (also refer to the processing sequence chart and flowchart).
   When ST1 = abnormal termination: Abnormal termination [B]
   When ST1 = time-out error: A time-out error [C] is returned.
   When ST1 = normal completion: The following processing is performed according to the ST2 value.
      • When ST2 ≠ ACK: Abnormal termination [D]
      • When ST2 = ACK: Proceeds to <11> when transmission of all of the user data is completed.
         If there still remain user data to be transmitted, the processing re-executes the sequence from <6>.

<11> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT5}} \)).

<12> The status frame is acquired by status check processing.

<13> The following processing is performed according to the result of status check processing.
   When the processing ends normally: Normal completion [A]
      (Indicating that the internal verify check has performed normally after completion of write)
   When the processing ends abnormally: Abnormal termination [E]
      (Indicating that the internal verify check has not performed normally after completion of write)
   When a time-out error occurs: A time-out error [C] is returned.
### 7.9.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Normal completion [A]</strong></td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
</tbody>
</table>
| Abnormal termination [B]       | Parameter error | 05H |  - The specified start/end address is not the start/end address of the block.  
  - The data length is under 2 words. |
|                                | Checksum error | 07H | The checksum of the transmitted command frame does not match. |
|                                | Protect error | 10H |  - Write is prohibited in the security setting.  
  - Boot block cluster rewrite is prohibited in the security setting. |
|                                | Negative acknowledgment (NACK) | 15H | Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]             | – | | Processing timed out due to the busy status at the HS pin. |
| Abnormal termination [D]       | Checksum error | 07H | The checksum of the transmitted command frame does not match. |
|                                | Write error | 1CH (ST2) | A write error has occurred. |
| Abnormal termination [E]       | MRG11 error | 1BH | An internal verify error has occurred. |
7.9.4 Flowchart
7.9.5 Sample program

The following shows a sample program for Programming command processing.

```c
/****************************************************************/
/* */
/* Write command (CSI-HS) */
/* */
/****************************************************************/
/* [i] u32 top ... start address */
/* [i] u32 bottom ... end address */
/* [r] u16 ... error code */
/****************************************************************/
u16 fl_hs_write(u32 top, u32 bottom)
{
    u16 rc;
    u32 send_head, send_size;
    bool is_end;
    u32 wt5_max;

    /*****************************************************************
    /* set params */
    /*****************************************************************
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL
    wt5_max = make_wt5_max(get_block_num(top, bottom));

    /*****************************************************************
    /* send command & check status */
    /*****************************************************************
    if (hs_busy_to(tCOM_TO))
        return FLC_HSTO_ERR; // t.o. detected
    if (rc = put_cmd_hs(FL_COM_WRITE, 7, fl_cmd_prm)) // send "Programming"
        return rc; // t.o. detected
    if (hs_busy_to(tWT3_TO))
        return FLC_HSTO_ERR; // t.o. detected

    rc = fl_hs_getstatus(); // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        case FLC_HSTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }

    /*****************************************************************
    /* send user data */
    /*****************************************************************
    send_head = top;

    while(1){
        // make send data frame
        if ((bottom - send_head) > 256){ // rest size > 256 ?
            is_end = false; // yes, not end frame
            send_size = 256; // transmit size = 256 byte
```
{  
    else{  
        is_end = true;  
        send_size = bottom - send_head + 1;  
        // transmit size = (bottom - send_head)+1 byte
    }
  
    memcpy(fl_txdata_frm, rom_buf+send_head, send_size);  
    // set data frame payload
    send_head += send_size;
  
  
  
  
    if (hs_busy_to(tFD3_TO)) // t.o. check before sending data frame  
        return FLC_HSTO_ERR; // t.o. detected
  
    if (rc = put_dfrm_hs(send_size, fl_txdata_frm, is_end))  
        // send user data
        return rc;  
        // error detected
  
    if (hs_busy_to(tWT4_MAX))  
        return FLC_HSTO_ERR;  // t.o. detected
  
    rc = fl_hs_getstatus();  // get status frame
    switch(rc) {  
        case FLC_NO_ERR: break; // continue
        // case FLC_HSTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

  
  
    if (fl_st2 != FLST_ACK){ // ST2 = ACK ?
        rc = decode_status(fl_st2);  // No
        return rc;  
        // case [D]
    }

  
  
    if (is_end) // send all user data ?
        break; // yes

  
  
  
  
  
    //***********************************************************************/
    /* Check internally verify */
    //***********************************************************************/
  
    if (hs_busy_to(wt5_max))
        return FLC_HSTO_ERR;  // t.o. detected
  
    rc = fl_hs_getstatus();  // get status frame
    switch(rc) {  
        case FLC_NO_ERR: return rc; break; // case [A]
        // case FLC_HSTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

    return rc;
}
7.10 Verify Command

7.10.1 Processing sequence chart

Verify command processing sequence
7.10.2 Description of processing sequence

<1> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{COM}} \)).

<2> The Verify command is transmitted by command frame transmission processing.

<3> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT6}} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

   When the processing ends normally: Proceeds to <6>.
   When the processing ends abnormally: Abnormal termination [B]
   When a time-out error occurs: A time-out error [C] is returned.

<6> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{FD3}} \)).

<7> User data for verifying is transmitted by data frame transmission processing.

<8> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT7}} \)).

<9> The status frame is acquired by status check processing.

<10> The following processing is performed according to the result of status check processing (status code (ST1/ST2)) (also refer to the processing sequence chart and flowchart).

   When ST1 = abnormal termination: Abnormal termination [B]
   When ST1 = time-out error: A time-out error [C] is returned.
   When ST1 = normal completion: The following processing is performed according to the ST2 value.
      • When ST2 = ACK: If transmission of all data frames is completed, the processing ends normally [A].
        If there still remain data frames to be transmitted, the processing re-executes the sequence from <6>.
      • When ST2 \( \neq \) ACK: Abnormal termination [D]

7.10.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
<tr>
<td>Abnormal termination [D]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Verify error</td>
<td>0FH (ST2)</td>
</tr>
</tbody>
</table>
7.10.4 Flowchart

![Flowchart Image]
7.10.5 Sample program

The following shows a sample program for Verify command processing.

```c
u16 fl_hs_verify(u32 top, u32 bottom, u8 *buf)
{
    u16   rc;
    u32   send_head, send_size;
    bool  is_end;

    // set params
    set_range_prm(fl_cmd_prm, top, bottom);  // set SAH/SAM/SAL, EAH/EAM/EAL

    // send command & check status
    if (hs_busy_to(tCOM_TO))
        return FLC_HSTO_ERR;  // t.o. detected

    if (rc = put_cmd_hs(FL_COM_VERIFY, 7, fl_cmd_prm))  // send "Verify" command
        return rc;  // error detected

    if (hs_busy_to(tWT6_TO))
        return FLC_HSTO_ERR;  // t.o. detected

    rc = fl_hs_getstatus();  // get status frame
    switch(rc) {
        case FLC_NO_ERR:    break;  // continue
        case FLC_HSTO_ERR:   return rc;  // error detected
        default:   return rc;  // case [B]
    }

    // send user data
    while(1){
        // make send data frame
        if (((bottom - send_head) > 256){  // rest size > 256 ?
            is_end = false;  // yes, not is_end frame
            send_size = 256;  // transmit size = 256 byte
        }
```
else{
    is_end = true;
    send_size = bottom - send_head + 1;
    // transmit size = (bottom - send_head)+1 byte
}
memcpy(fl_txdata_frm, buf+send_head, send_size); // set data frame payload
send_head += send_size;

if (hs_busy_to(tFD3_TO))
    return FLC_HSTO_ERR; // t.o. detected

if (rc = put_dfrm_hs(send_size, fl_txdata_frm, is_end))
    // send user data
    return rc; // error detected

if (hs_busy_to(tWT7_MAX))
    return FLC_HSTO_ERR; // t.o. detected

rc = fl_hs_getstatus(); // get status frame
switch(rc) {
    case FLC_NO_ERR: break; // continue
    default: return rc; break; // case [B]
}

if (fl_st2 != FLST_ACK){ // ST2 = ACK ?
    rc = decode_status(fl_st2); // No
    return rc; // case [D]
}

if (is_end) // send all user data ?
    break; // yes

return FLC_NO_ERR; // case [A]
7.11 Block Blank Check Command

7.11.1 Processing sequence chart

Block Blank Check command processing sequence

![Diagram of Block Blank Check command processing sequence]
7.11.2 Description of processing sequence

<1> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{com}$).
<2> The Block Blank Check command is transmitted by command frame transmission processing.
<3> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{wax}$).
<4> The status frame is acquired by status check processing.
<5> The following processing is performed according to the result of status check processing.

   When the processing ends normally: Normal completion [A]
   When the processing ends abnormally: Abnormal termination [B]
   When a time-out error occurs: A time-out error [C] is returned.

7.11.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>Normal acknowledgment (ACK)</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>05H</td>
<td>Parameter error</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The specified start/end address is out of the flash memory range.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The specified start/end address is not the start/end address of the block.</td>
</tr>
<tr>
<td>Checksum error</td>
<td>07H</td>
<td>Checksum error</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
<td>Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>MRG11 error</td>
<td>18H</td>
<td>The specified block in the flash memory is not blank.</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
</tbody>
</table>
7.11.4 Flowchart

Block Blank Check command processing

HS pin = BUSY?
  Yes
  Timed out?
    Yes
    tCOM
    Time-out error [C]
  No

No

Command frame transmission processing (Block Blank Check)

HS pin = BUSY?
  Yes
  Timed out?
    Yes
    tWTB
    Time-out error [C]
  No

No

Status check processing

Time-out error?
  Yes
  Time-out error [C]
  No

Normal completion?
  Yes
  Abnormal termination [B]
  No

Normal completion [A]
7.11.5 Sample program

The following shows a sample program for Block Blank Check command processing for one block.

```c
/*******************************************************************************/
/* */
/* Block blank check command (CSI-HS) */
/* */
/*******************************************************************************/
/* [i] u16 sblk ... start block number */
/* [i] u16 eblk ... end block number */
/* [r] u16 ... error code */
/*******************************************************************************/

u16 fl_hs_blk_blank_chk(u16 sblk, u16 eblk)
{
    u16 rc;
    u32 wt8_max;

    top = get_top_addr(sblk);  // get start address of start block
    bottom = get_bottom_addr(eblk); // get end address of end block
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    wt8_max = make_wt8_max(sblk, eblk); // get tWT8(Max)

    if (hs_busy_to(tCOM_TO))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]

    if (rc = put_cmd_hs(FL_COM_BLOCK_BLANK_CHK, 7, fl_cmd_prm))
        return rc;   // case [C]

    if (hs_busy_to(wt8_max))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]

    rc = fl_hs_getstatus(); // get status frame
    switch(rc) {
        case FLC_NO_ERR: return rc; break; // case [A]
        case FLC_HSTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

    return rc;
}
```
7.12 Silicon Signature Command

7.12.1 Processing sequence chart

Silicon Signature command processing sequence

Programmer

V850E/IG3

<1> BUSY time-out check using HS pin

<2> Silicon Signature command frame transmission

<3> BUSY time-out check using HS pin

<4> Status check processing

<5> Result of status check processing

Result
[Normal completion/ Abnormal termination/ Time-out error]

<6> BUSY time-out check using HS pin

<7> Data frame (silicon signature) reception processing

Time-out occurs

BUSY release

Time-out
occurs

Time-out
occurs

Abnormal termination

Normal completion

Normal data frame? [Yes/No]

Yes

Normal completion [A]

No

Data frame error [D]

Time-out error [C]

Abnormal termination [B]

Time-out error [C]
7.12.2 Description of processing sequence

<1> A V850E/IG3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time t_{com}).

<2> The Silicon Signature command is transmitted by command frame transmission processing.

<3> A V850E/IG3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time t_{w211}).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

- When the processing ends normally: Proceeds to <6>.
- When the processing ends abnormally: Abnormal termination [B]
- When a time-out error occurs: A time-out error [C] is returned.

<6> A V850E/IG3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time t_{f2}).

<7> The received data frame (silicon signature data) is checked.

- If data frame is normal: Normal completion [A]
- If data frame is abnormal: Data frame error [D]

7.12.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>The command was executed normally and the silicon signature was acquired normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>07H</td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td></td>
<td>15H</td>
<td>Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as silicon signature data does not match.</td>
</tr>
</tbody>
</table>
7.12.4 Flowchart

- Silicon Signature command processing
  - HS pin = BUSY?
    - Yes
    - Normal completion [A]
    - No
    - Time-out error [C]
  - No
    - Command frame transmission processing (Silicon Signature)
      - HS pin = BUSY?
        - Yes
        - Timed out?
          - Yes
          - Time-out error [C]
          - No
          - Status check processing
            - Time-out error?
              - Yes
              - Time-out error [C]
              - No
              - Normal completion?
                - Yes
                - Abnormal termination [B]
                - No
                - Normal completion [A]
      - No
        - Data frame reception processing
          - HS pin = BUSY?
            - Yes
            - Timed out?
              - Yes
              - Data frame error [D]
              - No
              - Normal data frame?
                - Yes
                - Normal completion [A]
                - No
                - Data frame error [D]
7.12.5 Sample program

The following shows a sample program for Silicon Signature command processing.

```c
#include <stdio.h>
#include <stdlib.h>

#define OFS_STA_PLD 0
#define OFS_LEN 24

/* Get silicon signature command (CSI-HS) */
u16 fl_hs_getsig(u8 *sig) {
    u16 rc;
    if (hs_busy_to(tCOM_TO))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]
    if (rc = put_cmd_hs(FL_COM_GET_SIGNATURE, 1, fl_cmd_prm))
        // send "Silicon Signature" command
        return rc;   // error detected :case [C]
    if (hs_busy_to(tWT11_MAX))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]
    rc = fl_hs_getstatus();  // get status frame
    switch(rc) {  // get status frame
        case FLC_NO_ERR:   break; // continue
        // case FLC_HSTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }
    if (hs_busy_to(tFD2_MAX))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]
    rc = get_dfrm_hs(fl_rxdata_frm); // get signature data
    switch(rc) {  // get signature data
        case FLC_NO_ERR:   break; // continue
        // case FLC_HSTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [D]
    }
    memcpy(sig, fl_rxdata_frm+OFS_STA_PLD, fl_rxdata_frm[OFS_LEN]);  // copy Signature data
    return rc;    // case [A]
}
```
7.13 Version Get Command

7.13.1 Processing sequence chart

Version Get command processing sequence

Programmer

- <1> BUSY time-out check using HS pin
- BUSY release
- <2> Version Get command frame transmission
- <3> BUSY time-out check using HS pin
- BUSY release
- <4> Status check processing
- <5> Result of status check processing
- Result
  - [Normal completion/ Abnormal termination/ Time-out error]

V850E/IG3

- <6> BUSY time-out check using HS pin
- BUSY release
- <7> Data frame (version data) reception processing
- Normal data frame?
  - [Yes/No]
  - No
  - Data frame error [D]
  - Yes
  - Normal completion [A]
7.13.2 Description of processing sequence

<1> A V850E/IG3 BUSY status is checked using the HS pin.
If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{com}$).

<2> The Version Get command is transmitted by command frame transmission processing.

<3> A V850E/IG3 BUSY status is checked using the HS pin.
If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{v311}$).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

When the processing ends normally: Proceeds to <6>.
When the processing ends abnormally: Abnormal termination [B]
When a time-out error occurs: A time-out error [C] is returned.

<6> A V850E/IG3 BUSY status is checked using the HS pin.
If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{f3d}$).

<7> The received data frame (version data) is checked.

If data frame is normal: Normal completion [A]
If data frame is abnormal: Data frame error [D]

7.13.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as version data does not match.</td>
</tr>
</tbody>
</table>
7.13.4 Flowchart

- **Version Get command processing**

  - HS pin = BUSY?
    - Yes: Timed out?
      - Yes: Time-out error [C]
      - No: Normal completion?
        - Yes: Abnormal termination [B]
        - No: Normal completion?
          - Yes: Abnormal termination [B]
          - No: Data frame reception processing

  - No: Command frame transmission processing (Version Get)

  - HS pin = BUSY?
    - Yes: Timed out?
      - Yes: Time-out error [C]
      - No: Normal completion?
        - Yes: Abnormal termination [B]
        - No: Data frame reception processing

  - No: Status check processing

  - Time-out error?
    - Yes: Time-out error [C]
    - No: Normal completion?
      - Yes: Normal completion [A]
      - No: Data frame error [D]
7.13.5 Sample program

The following shows a sample program for Version Get command processing.

```
/***********************)
/*                    */
/* Get device/firmware version command (CSI-HS) */
/*                    */
*****************************/
/* [i] u8 *buf ... pointer to version date save area */
/* [r] u16         ... error code */
*****************************/

u16  fl_hs_getver(u8 *buf)
{
    u16   rc;

    if (hs_busy_to(tCOM_TO))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]

    if (rc = put_cmd_hs(FL_COM_GET_VERSION, 1, fl_cmd_prm))
        return rc;   // error detected :case [C]

    if (hs_busy_to(tWT12_TO))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]

    rc = fl_hs_getstatus();  // get status frame
    switch(rc) {
      case FLC_NO_ERR: break; // continue
      // case FLC_HSTO_ERR: return rc; break; // case [C]
      default:         return rc; break; // case [B]
    }

    if (hs_busy_to(tFD2_TO))
        return FLC_HSTO_ERR;  // t.o. detected :case [C]

    rc = get_dfrm_hs(fl_rxdata_frm);  // get version data
    switch(rc) {
      case FLC_NO_ERR: break; // continue
      // case FLC_HSTO_ERR: return rc; break; // case [C]
      default:         return rc; break; // case [D]
    }

    memcpy(buf, fl_rxdata_frm+OFS_STA_PLD, DFV_LEN);  // copy version data
    return rc;    // case [A]
}
```
7.14 Checksum Command

7.14.1 Processing sequence chart

Checksum command processing sequence
7.14.2 Description of processing sequence

<1> A V850E/IG3 BUSY status is checked using the HS pin. If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{com}$).

<2> The Checksum command is transmitted by command frame transmission processing.

<3> A V850E/IG3 BUSY status is checked using the HS pin. If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{w16}$).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

<table>
<thead>
<tr>
<th>When the processing ends normally:</th>
<th>Proceeds to &lt;6&gt;.</th>
</tr>
</thead>
<tbody>
<tr>
<td>When the processing ends abnormally:</td>
<td>Abnormal termination [B]</td>
</tr>
<tr>
<td>When a time-out error occurs:</td>
<td>A time-out error [C] is returned.</td>
</tr>
</tbody>
</table>

<6> A V850E/IG3 BUSY status is checked using the HS pin. If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{f16}$).

<7> The received data frame (checksum data) is checked.

<table>
<thead>
<tr>
<th>If data frame is normal:</th>
<th>Normal completion [A]</th>
</tr>
</thead>
<tbody>
<tr>
<td>If data frame is abnormal:</td>
<td>Data frame error [D]</td>
</tr>
</tbody>
</table>

7.14.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>The command was executed normally and checksum data was acquired normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>05H</td>
<td>The specified start/end address is not a fixed address in block units (2 KB) starting from the top of the flash memory.</td>
</tr>
<tr>
<td>Checksum error</td>
<td>07H</td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
<td>Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as version data does not match.</td>
</tr>
</tbody>
</table>
7.14.4 Flowchart

- Checksum command processing
- HS pin = BUSY?
  - Yes: Timed out? Yes → Time-out error [C]
  - No: Command frame transmission processing (Checksum)
  - HS pin = BUSY?
    - Yes: Timed out? Yes → Time-out error [C]
    - No: Status check processing
      - Time-out error? Yes → Time-out error [C]
      - No: Normal completion?
        - Yes: Abnormal termination [B]
        - No: Data frame reception processing
          - Timed out? Yes → Time-out error [C]
          - No: Normal data frame?
            - Yes: Normal completion [A]
            - No: Data frame error [D]
7.14.5 Sample program

The following shows a sample program for Checksum command processing.

```c
/**
/* Get checksum command (CSI-HS)
/*
/**
******************************************************************************/

u16 fl_hs_getsum(u16 *sum, u32 top, u32 bottom) {
    u16 rc;
    u32 fd1_max;

    /******************************************************************************/
    /* set params */
    /******************************************************************************/
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL
    fd1_max = get_fd1_max(get_block_num(top, bottom)); // get tFD1(Max)

    /******************************************************************************/
    /* send command */
    /******************************************************************************/
    if (hs_busy_to(tCOM_TO))
        return FLC_HSTO_ERR; // t.o. detected :case [C]
    if (rc = put_cmd_hs(FL_COM_GET_CHECK_SUM, 7, fl_cmd_prm))
        // send "Checksum" command
        return rc; // error detected :case [C]
    if (hs_busy_to(tWT16_TO))
        return FLC_HSTO_ERR; // t.o. detected :case [C]
    rc = fl_hs_getstatus(); // get status frame
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        case FLC_HSTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

    /******************************************************************************/
    /* get data frame (Checksum data) */
    /******************************************************************************/
    if (hs_busy_to(fd1_max))
        return FLC_HSTO_ERR; // t.o. detected :case [C]
    rc = get_dfrm_hs(fl_rxdata_frm); // get sum data
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        case FLC_HSTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [D]
    }

    *sum = (fl_rxdata_frm[OFS_STA_PLD] << 8) + fl_rxdata_frm[OFS_STA_PLD+1];
    return rc; // case [A]
}
```
7.15 Security Set Command

7.15.1 Processing sequence chart

Security Set command processing sequence

Programmer

V850E/IG3

<1> BUSY time-out check using HS pin

<2> Security Set command frame transmission

<3> BUSY time-out check using HS pin

<4> Status check processing

<5> Result of status check processing

<6> BUSY time-out check using HS pin

<7> Data frame transmission (security data)

<8> BUSY time-out check using HS pin

<9> Status check processing

<10> Result of status check processing

<11> BUSY time-out check using HS pin

<12> Status check processing

<13> Result of status check processing

Time-out error [C]

Abnormal termination [B]

Time-out error [C]

Abnormal termination [C]

Time-out error [C]

Abnormal termination [E]

Normal completion

Abnormal termination [A]
7.15.2 Description of processing sequence

<1> A V850E/IG3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{com} \)).

<2> The Security Set command is transmitted by command frame transmission processing.

<3> A V850E/IG3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT13} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.
    When the processing ends normally: Proceeds to <6>.
    When the processing ends abnormally: Abnormal termination [B]
    When a time-out error occurs: A time-out error [C] is returned.

<6> A V850E/IG3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{rea} \)).

<7> The data frame (security setting data) is transmitted by data frame transmission processing.

<8> A V850E/IG3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT14} \)).

<9> The status frame is acquired by status check processing.

<10> The following processing is performed according to the result of status check processing.
    When the processing ends normally: Proceeds to <11>.
    When the processing ends abnormally: Abnormal termination [D]
    When a time-out error occurs: A time-out error [C] is returned.

<11> A V850E/IG3 BUSY status is checked using the HS pin.
    If a BUSY time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT15} \)).

<12> The status frame is acquired by status check processing.

<13> The following processing is performed according to the result of status check processing.
    When the processing ends normally: Normal completion [A]
    When the processing ends abnormally: Abnormal termination [E]
    When a time-out error occurs: A time-out error [C] is returned.
### 7.15.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td>Abnormal termination [C]</td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
<tr>
<td>Abnormal termination [D]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td>Abnormal termination [D]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
| Abnormal termination [D]       | Protect error | 10H | • An attempt was made to enable a flag that was already prohibited in the setting.  
    • An attempt was made to change the last block number of the boot block cluster in the state that boot block cluster rewrite is prohibited. |
| Abnormal termination [D]       | MGR10 error | 1AH | A write error has occurred. |
| Write error                    | 1CH          |             |
| Abnormal termination [E]       | MRG11 error | 1BH | An internal verify error has occurred. |
7.15.4 Flowchart

```
Normal completion?

Security Set command processing

HS pin = BUSY?
  Yes
  Time-out error [C]
  No
  Command frame transmission processing (Security Set)

Status check processing

Timeout error?
  Yes
  Abnormal termination [B]
  No
  Normal completion? (security data)

Time-out error?
  Yes
  Abnormal termination [C]
  No
  Status check processing

Timeout error?
  Yes
  Abnormal termination [C]
  No
  Normal completion?

Abnormal termination [D]

Yes

Normal completion? [A]

Yes

Time-out error?
  Yes
  Abnormal termination [C]
  No
  Time-out error [C]

Yes

Abnormal termination [E]

Yes

Normal completion? [A]
```

### 7.15.5 Sample program

The following shows a sample program for Security Set command processing.

```c
/**
 * Set security flag command (CSI-HS)
 */
/**
 * 
 */
u16 fl_hs_setscf(u8 scf, u8 bot)
{
    u16 rc;

    /***************************************************************************/
    /* set params */
    /***************************************************************************/
    fl_cmd_prm[0] = 0x00;   // "BLK" (must be 0x00)
    fl_cmd_prm[1] = 0x00;   // "PAG" (must be 0x00)
    fl_txdata_frm[0] = scf|= 0b11100000;// "FLG" (bit 7,6,5,4 must be '1')
    fl_txdata_frm[1] = bot;   // "BOT"

    /***************************************************************************/
    /* send command */
    /***************************************************************************/
    if (hs_busy_to(tCOM_TO))
      return FLC_HSTO_ERR;  // t.o. detected :case [C]
    if (rc = put_cmd_hs(FL_COM_SET_SECURITY, 3, fl_cmd_prm))
      // send "Security Set" command
      return rc;   // error detected :case [C]
    if (hs_busy_to(tWT13_TO))
      return FLC_HSTO_ERR;  // t.o. detected :case [C]

    rc = fl_hs_getstatus();   // get status frame
    switch(rc) {
      case FLC_NO_ERR:   break; // continue
      case FLC_HSTO_ERR: return rc; // case [C]
      default:  return rc; break; // case [B]
    }

    /***************************************************************************/
    /* send data frame (security setting data) */
    /***************************************************************************/
    if (hs_busy_to(tFD3_TO))
      return FLC_HSTO_ERR;  // t.o. detected :case [C]
    if (rc = put_dfrm_hs(2, fl_txdata_frm, true)) // send security setting data
      return rc;   // error detected :case [C]
    if (hs_busy_to(tWT14_MAX))
```

```c
```
return FLC_HSTO_ERR;       // t.o. detected : case [C]

rc = fl1_hs_getstatus();   // get status frame
switch(rc) {
    case FLC_NO_ERR:   break; // continue
    case FLC_HSTO_ERR: return rc; break; // case [C]
    default:  return rc; break; // case [B]
}

/************************************************/
/* Check internally verify                           */
/************************************************/
if (hs_busy_to(tWT15_MAX))
    return FLC_HSTO_ERR;       // t.o. detected

rc = fl1_hs_getstatus();   // get status frame again
switch(rc) {
    case FLC_NO_ERR: return rc; break; // case [A]
    case FLC_HSTO_ERR: return rc; break; // case [C]
    default:  return rc; break; // case [B]
}

return rc;
7.16  Read Command

7.16.1  Processing sequence chart

Read command processing sequence: 

1. BUSY time-out check using HS pin
2. Read command frame transmission
3. BUSY time-out check using HS pin
4. Status check processing
5. Result of status check processing
6. BUSY time-out check using HS pin
7. Data frame reception (user data)
8. BUSY time-out check using HS pin
9. Status (NACK) frame transmission
10. BUSY time-out check using HS pin
11. Status (ACK) frame transmission

Time-out: 

- Time-out check
- BUSY release
- Time-out error
- Normal completion
- Abnormal termination

Reception error occurred? 

- Yes: Time-out error
- No: Data frame error

All data frames received? 

- Yes: Normal completion
- No: To <6>

Result 

- Normal completion
- Abnormal completion
- Abnormal termination
7.16.2 Description of processing sequence

<1> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{COM}$).

<2> The Read command is transmitted by command frame transmission processing.

<3> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{W17}$).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

   When the processing ends normally: Proceeds to <6>.
   When the processing ends abnormally: Abnormal termination [B]
   When a time-out error occurs: A time-out error [C] is returned.

<6> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{W18}$).

<7> The data frame (user data) in the flash memory is received by data frame reception processing.

   When the processing ends normally: Proceeds to <10>.
   When an error such as checksum error occurs: Proceeds to <8>.
   When a time-out error occurs: A time-out error [C] is returned.

<8> A V850E/IG3 BUSY status is checked using the HS pin.
   If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{W19}$).

<9> The NACK frame is transmitted by data frame transmission processing.
    A data frame error [D] is returned.

<10> A V850E/IG3 BUSY status is checked using the HS pin.
     If a BUSY time-out occurs, a time-out error [C] is returned (time-out time $t_{W19}$).

<11> The ACK frame is transmitted by data frame transmission processing.
     When reception of all data frames is completed, the normal completion status [A] is returned.
     If there still remain data frames to be received, the sequence is re-executed from <6>.
### 7.16.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as read data does not match.</td>
</tr>
</tbody>
</table>
7.16.4 Flowchart

- Read command processing
  - HS pin = BUSY?
    - Yes: Command frame transmission processing (Read)
    - No: Time-out error
  - Normal completion?
    - Yes: Abnormal termination [B]
    - No: Time-out error [C]

- Status check processing
  - HS pin = BUSY?
    - Yes: Time-out error [C]
    - No: Normal completion?
      - Yes: Abnormal termination [B]
      - No: Time-out error [C]

- Data frame (user program) reception processing
  - HS pin = BUSY?
    - Yes: Time-out error [C]
    - No: Timed out during data frame reception?
      - Yes: Time-out error [C]
      - No: Normal completion?
        - Yes: Abnormal termination [B]
        - No: All data frames Received?
          - Yes: Normal completion [A]
          - No: Status (ACK) frame transmission
            - HS pin = BUSY?
              - Yes: Time-out error [C]
              - No: Timed out?
                - Yes: Time-out error [C]
                - No: Status (NACK) frame transmission
                  - HS pin = BUSY?
                    - Yes: Time-out error [C]
                    - No: Normal completion?
7.16.5 Sample program
The following shows a sample program for Read command processing.

```c
u16 fl_hs_read(u32 top, u32 bottom)
{
    u16 rc;
    u32 read_head;
    u16 len;
    u8 hooter;

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    if (hs_busy_to(tCOM_TO))
        return FLC_HSTO_ERR; // t.o. detected :case [C]

    if (rc = put_cmd_hs(FL_COM_READ, 7, fl_cmd_prm))
        return rc;

    if (hs_busy_to(tWT17_TO))
        return FLC_HSTO_ERR; // t.o. detected :case [C]

    rc = fl_hs_getstatus(); // get status frame
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        case FLC_HSTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

    while(1){
        if (hs_busy_to(tWT18_TO))
            return FLC_HSTO_ERR; // t.o. detected :case [C]

        rc = get_dfrm_hs(fl_rxdata_frm); // get ROM data from FLASH
        switch(rc) {
            case FLC_NO_ERR: break; // continue
            case FLC_HSTO_ERR: return rc; break; // case [C]
        }
    }
```

// case FLC_RX_DFSUM_ERR:
   default:  // case [D]

      if (hs_busy_to(tWT19_TO))
         return FLC_HSTO_ERR;  // t.o. detected

         put_sfrm_hs(FLST_NACK);  // send status(NACK) frame
         return rc;
      break;

   }

   if (hs_busy_to(tWT19_TO))
      return FLC_HSTO_ERR;  // t.o. detected

   put_sfrm_hs(FLST_ACK);  // send status(ACK) frame

   /*************************************************************************/
   /* save ROM data */
   /*************************************************************************/
   if ((len = fl_rxdata_frm[OFS_LEN]) == 0)  // get length
      len = 256;

   memcpy(read_buf+read_head, fl_rxdata_frm+2, len);  // save to external RAM
   read_head += len;

   /*************************************************************************/
   /* end check */
   /*************************************************************************/
   hooter = fl_rxdata_frm[len + 3];
   if (hooter == FL_ETB)  // end frame ?
      continue;  // no
   break;  // yes

   return FLC_NO_ERR;
}
CHAPTER 8  3-WIRE SERIAL I/O COMMUNICATION MODE (CSI)

Each of the symbol (tXX and twXXX) shown in the flowchart in this chapter is the symbol of characteristic item in CHAPTER 9 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS.

For each specified value, refer to CHAPTER 9 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS.
8.1 Command Frame Transmission Processing Flowchart

```
Command frame transmission processing
  Command frame header (SOH = 01H) transmission
    Wait between data transmissions
    Data length (LEN) transmission
    Wait between data transmissions
    Command number (COM) transmission
      (LEN - 1) bytes transmitted?
        Yes
          ... (Flowchart continues)
        No
          Wait between data transmissions
          Transmits 1-byte parameter
            ... (Flowchart continues)
    Wait between data transmissions
    Checksum data (SUM) transmission
    Wait between data transmissions
    Command frame footer (ETX = 03H) transmission
    End of command frame transmission
```
8.2 Data Frame Transmission Processing Flowchart

```
Data frame transmission processing

Data frame header (STX = 02H) transmission

Wait between data transmissions

Data length (LEN) transmission

LEN bytes transmitted? Yes

Data frame transmission processing

No

Wait between data transmissions

Transmits 1-byte data

Wait between data transmissions

Checksum data (SUM) transmission

Wait between data transmissions

Last data frame? No

Wait between data transmissions

Last data frame footer (ETX = 03H) transmission

Yes

Transmission of footer other than those of last data frame (ETB = 17H)

End of data frame transmission
```
8.3 Data Frame Reception Processing Flowchart

- Data frame reception processing
  - Data frame header (STX = 02H) reception
    - Wait between data receptions
      - Data length (LEN) reception
        - Wait between data receptions
          - Receives 1-byte data
            - LEN bytes received?
              - Yes
                - Wait between data receptions
                  - Checksum data (SUM) reception
                    - Wait between data receptions
                      - Reception of last data frame footer (ETX = 03H) or footer other than those of last data frame (ETB = 17H)
                        - Checksum error?
                          - Yes
                            - Checksum error
                          - No
                            - End of data frame reception
8.4 Status Command

8.4.1 Processing sequence chart

Status command processing sequence

Note: Applied specifications differ depending on the command executed.
8.4.2 Description of processing sequence

<1> The Status command is transmitted by command frame transmission processing.
<2> Waits from command transmission until status frame reception (wait time tSF).
<3> The status code is checked.

When ST1 = ACK: Normal completion [A]
When ST1 = BUSY: A time-out check is performed (tWT x N).

If the processing is not timed out, the sequence is re-executed from <1>.
If a time-out occurs, a time-out error [C] is returned.

When ST1 ≠ ACK, BUSY: Abnormal termination [B]

Note Applied specifications differ depending on the command executed.

8.4.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Command error</td>
<td>04H</td>
</tr>
<tr>
<td></td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Verify error</td>
<td>0FH</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td></td>
<td>FLMD error</td>
<td>18H</td>
</tr>
<tr>
<td></td>
<td>MRG10 error</td>
<td>1AH</td>
</tr>
<tr>
<td></td>
<td>MRG11 error</td>
<td>1BH</td>
</tr>
<tr>
<td></td>
<td>Write error</td>
<td>1CH</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>After command transmission, the specified time has elapsed but a BUSY response is still returned.</td>
</tr>
</tbody>
</table>
8.4.4 Flowchart

Note  Applied specifications differ depending on the command executed.
8.4.5 Sample program

The following shows a sample program for Status command processing.

```c
static u16 fl_csi_getstatus(u32 limit)
{
    u16 rc;
    start_flto(limit);
    while(1){
        put_cmd_csi(FL_COM_GET_STA, 1, fl_cmd_prm); // send "Status" command frame
        fl_wait(tSF); // wait
        rc = get_sfrm_csi(fl_rxdata_frm); // get status frame
        switch(rc){
            case FLC_BUSY:
                if (check_flto()) // time out ?
                    return FLC_DFTO_ERR; // Yes, time-out // case [C]
                continue; // No, retry
            default: // checksum error
                return rc;
            case FLC_NO_ERR: // no error
                break;
        }
        if (fl_st1 == FLST_BUSY){ // ST1 = BUSY
            if (check_flto()) // time out ?
                return FLC_DFTO_ERR; // Yes, time-out // case [C]
            continue; // No, retry
        }
        if (fl_rxdata_frm[OFS_LEN] == 2 && fl_st1 == FLST_ACK && fl_st2 == FLST_BUSY){
            if (check_flto()) // time out ?
                return FLC_DFTO_ERR; // Yes, time-out // case [C]
            continue;
        }
        break; // ACK or other error (but BUSY)
    }
    rc = decode_status(fl_st1); // decode status to return code
    switch(rc) {
    // case FLC_NO_ERR: return rc; break; // case [A]
    // default: return rc; break; // case [B]
    }
    return rc;
}
```

8.5 Reset Command

8.5.1 Processing sequence chart

Reset command processing sequence

**Note**  Do not exceed the retry count for the reset command transmission (up to 16 times).
8.5.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{COM}$).
<2> The Reset command is transmitted by command frame transmission processing.
<3> Waits from command transmission until status check processing (wait time $t_{WK}$).
<4> The status frame is acquired by status check processing.
<5> The following processing is performed according to the result of status check processing.

When the processing ends normally: Normal completion [A]
When the processing ends abnormally: The sequence is re-executed from <1> if the retry count is not over.
If the retry count is over, the processing ends abnormally [B].
When a time-out error occurs: A time-out error [C] is returned.

8.5.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|                                 | Negative acknowledgment (NACK) | 15H | • A command other than the Status command was received during processing.  
|                                 |                          |     | • Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]             | –                      | – | Status check processing timed out. |
8.5.4 Flowchart

- Reset command processing
- Wait from previous frame reception until next command transmission
- Command frame transmission processing (Reset)
- Wait from command frame transmission until status check
- Status check processing
- Result of status check processing = Abnormal termination?
  - Yes
    - Retry count over?
      - Yes
        - Abnormal termination [B]
      - No
        - Result of status check processing = Time-out error?
          - Yes
            - Time-out error [C]
          - No
            - Normal completion [A]

- Result of status check processing = Abnormal termination?
8.5.5 Sample program

The following shows a sample program for Reset command processing.

```c
/**
* Reset command (CSI)
*/
/**
* [r] u16 ... error code
*/

u16 fl_csi_reset(void)
{
    u16 rc;
    u32 retry;

    for (retry = 0; retry < tRS; retry++){
        fl_wait(tCOM);    // wait before sending command frame
        put_cmd_csi(FL_COM_RESET, 1, fl_cmd_prm); // send "Reset" command frame
        fl_wait(tWT0);
        rc = fl_csi_getstatus(tWT0_TO);  // get status
        if (rc == FLC_DFTO_ERR)  // timeout error ?
            break;   // yes // case [C]
        if (rc == FLC_ACK)   // Ack ?
            break;    // yes // case [A]
        //continue;    // case [B] (if exit from loop)
    }
    //switch(rc) {
    //  case FLC_NO_ERR:  return rc; break; // case [A]
    //  case FLC_DFTO_ERR: return rc; break; // case [C]
    //  default:   return rc; break; // case [B]
    //}
    return rc;
}
```
8.6 Oscillating Frequency Set Command

8.6.1 Processing sequence chart

Oscillating Frequency Set command processing sequence

- **<1>** Wait from previous frame reception until next command transmission
- **<2>** Oscillating Frequency Set command frame transmission
- **<3>** Wait from command frame transmission until status check
- **<4>** Status check processing
- **<5>** Result of status check processing

Result:
- Normal completion
- Abnormal termination
- Time-out error

Abnormal termination [B]

Normal completion [A]

Abnormal termination [C]

Time-out error [C]

Time-out error
8.6.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{\text{com}}$).
<2> The Oscillating Frequency Set command is transmitted by command frame transmission processing.
<3> Waits from command transmission until status check processing (wait time $t_{\text{wa}}$).
<4> The status frame is acquired by status check processing.
<5> The following processing is performed according to the result of status check processing.

When the processing ends normally: Normal completion [A]
When the processing ends abnormally: Abnormal termination [B]
When a time-out error occurs: A time-out error [C] is returned.

8.6.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
</tbody>
</table>
8.6.4 Flowchart

1. Oscillating Frequency Set command processing

2. Wait from previous frame reception until next command transmission

3. Command frame transmission processing (Oscillating Frequency Set)

4. Wait from command frame transmission until status check

5. Status check processing

6. Time-out error?
   - Yes: Time-out error [C]
   - No: Normal completion?
     - Yes: Normal completion [A]
     - No: Abnormal termination [B]
8.6.5 Sample program
The following shows a sample program for Oscillating Frequency Set command processing.

```c
/****************************************************************************
/*                                                                          *
/* Set Flash device clock value command (CSI)                              *
/*                                                                          *
****************************************************************************/
/* [i] u8 clk[4] ... frequency data(D1-D4)                               *
/* [r] u16 ... error code                                                 *
****************************************************************************/
u16 fl_csi_setclk(u8 clk[])
{
    u16 rc;

    fl_cmd_prm[0] = clk[0];  // "D01"
    fl_cmd_prm[1] = clk[1];  // "D02"
    fl_cmd_prm[2] = clk[2];  // "D03"
    fl_cmd_prm[3] = clk[3];  // "D04"

    fl_wait(tCOM);        // wait before sending command frame

    put_cmd_csi(FL_COM_SET_OSC_FREQ, 5, fl_cmd_prm); // send "Oscillation
                                                      // Frequency Set" command

    fl_wait(tWT9);

    rc = fl_csi_getstatus(tWT9_TO); // get status frame

    //switch(rc) {
    //    case FLC_NO_ERR:  return rc; break; // case [A]
    //    case FLC_ERRTO:    return rc; break; // case [C]
    //    default:           return rc; break; // case [B]
    //}
    return rc;
}
```
8.7 Chip Erase Command

8.7.1 Processing sequence chart

Chip Erase command processing sequence

<table>
<thead>
<tr>
<th>Step</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Wait from previous frame reception until next command transmission</td>
</tr>
<tr>
<td>2</td>
<td>Chip Erase command frame transmission</td>
</tr>
<tr>
<td>3</td>
<td>Wait from command frame transmission until status check</td>
</tr>
<tr>
<td>4</td>
<td>Status check processing</td>
</tr>
<tr>
<td>5</td>
<td>Result of status check processing</td>
</tr>
</tbody>
</table>

Result:
- Normal completion
- Abnormal termination
- Time-out error

Time-out error:
- Time-out error [C]

Abnormal termination:
- Abnormal termination [B]

Normal completion:
- Normal completion [A]
8.7.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{\text{com}}$).
<2> The Chip Erase command is transmitted by command frame transmission processing.
<3> Waits from command transmission until status check processing (wait time $t_{\text{WT1}}$).
<4> The status frame is acquired by status check processing.
<5> The following processing is performed according to the result of status check processing.

When the processing ends normally: Normal completion [A]
When the processing ends abnormally: Abnormal termination [B]
When a time-out error occurs: A time-out error [C] is returned.

8.7.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
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<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
</tbody>
</table>
|                                 | Protect error | 10H | - Chip erase is prohibited in the security setting.  
- Boot block cluster rewrite is prohibited in the security setting. |
|                                 | Negative acknowledgment (NACK) | 15H | Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Erase error                     | 1AH | An erase error has occurred. |
| Write error                     | 1CH | |
| MRG10 error                     | 1AH | |
| MRG11 error                     | 18H | |
| Time-out error [C]              | – | The status frame was not received within the specified time. |
8.7.4 Flowchart

Chip Erase command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Chip Erase)

Wait from command frame transmission until status check

Status check processing

Time-out error?

No

Yes

Normal completion?

No

Abnormal termination [B]

Yes

Normal completion [A]

Time-out error [C]
8.7.5 Sample program

The following shows a sample program for Chip Erase command processing.

```c
/****************************************************************************
/*
/* Erase all(chip) command (CSI)
/*
/****************************************************************************
/* [r] ul6   ... error code */
/****************************************************************************
ul6   fl_csi_erase_all(void)
{
  ul6   rc;

  fl_wait(tCOM);    // wait before sending command frame
  put_cmd_csi(FL_COM_ERASE_CHIP, 1, fl_cmd_prm); // send "Chip Erase" command
  fl_wait(tWT1);

  rc = fl_csi_getstatus(tWT1_MAX); // get status frame
  //switch(rc) {
  //   case FLC_NO_ERR:  return rc; break; // case [A]
  //   case FLC_DFTO_ERR: return rc; break; // case [C]
  //   default:   return rc; break; // case [B]
  //}
  return rc;
}
```
8.8 Block Erase Command

8.8.1 Processing sequence chart

Block Erase command processing sequence

- **<1>** Wait from previous frame reception until next command transmission
- **<2>** Block Erase command frame transmission
- **<3>** Wait from command frame transmission until status check
- **<4>** Status check processing
- **<5>** Result of status check processing

Result:
- Normal completion
- Abnormal termination
- Time-out error

Flow:
- Time-out error [C] -> Normal completion [A]
- Abnormal termination [B]
8.8.2 Description of processing sequence

1. Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{COM}} \)).
2. The Block Erase command is transmitted by command frame transmission processing.
3. Waits until status frame acquisition (wait time \( t_{\text{WT2}} \)).
4. The status frame is acquired by status check processing.
5. The following processing is performed according to the result of status check processing.

   When the processing ends normally: Normal completion [A]
   When the processing ends abnormally: Abnormal termination [B]
   When a time-out error occurs: A time-out error [C] is returned.

8.8.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td>Protect error</td>
<td>10H</td>
<td>Block erase is prohibited in the security setting.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
<td>Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>MRG10 error</td>
<td>1AH</td>
<td>An erase error has occurred.</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
</tbody>
</table>
8.8.4 Flowchart

Block Erase command processing

Wait from previous frame reception until next command transmission  \( t_{COM} \)

Command frame transmission processing (Block Erase)

Wait from command frame transmission until status check  \( t_{WT2} \)

Status check processing

Time-out error?

Yes

Time-out error [C]

No

Normal completion?

Yes

Normal completion [A]

No

Abnormal termination [B]
8.8.5 Sample program

The following shows a sample program for Block Erase command processing for one block.

```c
/************************************************************************
/* */
/* Erase block command (CSI) */
/* */
/************************************************************************
/* [i] u16 sblk ... start block number */
/* [i] u16 eblk ... end block number */
/* [r] u16 ... error code */
/************************************************************************

u16 fl_csi_erase_blk(u16 sblk, u16 eblk)
{
    u16 rc;
    u32 wt2, wt2_max;
    u32 top, bottom;

    top = get_top_addr(sblk);  // get start address of start block
    bottom = get_bottom_addr(eblk); // get end address of end block

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    wt2 = make_wt2_min(sblk, eblk);  // get tWT2(Min)
    wt2_max = make_wt2_max(sblk, eblk);  // get tWT2(Max)

    fl_wait(tCOM);   // wait before sending command frame

    put_cmd_csi(FL_COM_ERASE_BLOCK, 7, fl_cmd_prm); // send "Block Erase"
    command

    fl_wait(wt2);

    rc = fl_csi_getstatus(wt2_max); // get status frame

    switch(rc) {
        //
        // case FLC_NO_ERR: return rc; break; // case [A]
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        //
        //
        // default: return rc; break; // case [B]
    }

    return rc;
}
```
8.9 Programming Command

8.9.1 Processing sequence chart

Programming command processing sequence

- **<1>** Wait from previous frame reception until next command transmission
- **<2>** Programming command frame transmission
- **<3>** Wait from command frame transmission until status check
- **<4>** Status check processing
- **<5>** Result of status check processing
- **<6>** Wait from previous frame reception until next data frame transmission
- **<7>** Data frame (user data) transmission
- **<8>** Wait during status check
- **<9>** Status check processing
- **<10>** Result of status check processing (ST1/ST2)
- **<11>** Wait during status check (internal verify)
- **<12>** Status check processing
- **<13>** Result of status check processing

**Result**
- Normal completion
- Abnormal termination
- Time-out error

**Reception status (ST1)**
- Normal completion
- Abnormal termination
- Time-out error

**Reception status (ST2)**
- ACK (other than ACK)

All data frames transmitted?
- Yes
  - Go to <6>
- No
  - Abnormal termination [D]

**Abnormal termination [B]**
- Time-out error
- Normal completion

**Abnormal termination [A]**
- Time-out error
- Normal completion

**Abnormal termination [E]**
- Time-out error
- Normal completion
8.9.2 Description of processing sequence

<<1>> Waits from the previous frame reception until the next command transmission (wait time $t_{COM}$).
<<2>> The Programming command is transmitted by command frame transmission processing.
<<3>> Waits from command transmission until status check processing (wait time $t_{WT3}$).
<<4>> The status frame is acquired by status check processing.
<<5>> The following processing is performed according to the result of status check processing.

- When the processing ends normally: Proceeds to <<6>>.
- When the processing ends abnormally: Abnormal termination [B]
- When a time-out error occurs: A time-out error [C] is returned.

<<6>> Waits until the next data frame transmission (wait time $t_{FD3}$).
<<7>> User data to be written to the V850E/IG3 flash memory is transmitted by data frame transmission processing.
<<8>> Waits from data frame (user data) transmission until status check processing (wait time $t_{WT4}$).
<<9>> The status frame is acquired by status check processing.
<<10>> The following processing is performed according to the result of status check processing (status code (ST1/ST2)) (also refer to the processing sequence chart and flowchart).

- When ST1 = abnormal termination: Abnormal termination [B]
- When ST1 = time-out error: A time-out error [C] is returned.
- When ST1 = normal completion: The following processing is performed according to the ST2 value.
  - When ST2 $\neq$ ACK: Abnormal termination [D]
  - When ST2 = ACK: Proceeds to <<11>> when transmission of all of the user data is completed.
    - If there still remain user data to be transmitted, the processing re-executes the sequence from <<6>>.

<<11>> Waits until status check processing (time-out time $t_{WT5}$).
<<12>> The status frame is acquired by status check processing.
<<13>> The following processing is performed according to the result of status check processing.

- When the processing ends normally: Normal completion [A]
  (Indicating that the internal verify check has performed normally after completion of write)
- When the processing ends abnormally: Abnormal termination [E]
  (Indicating that the internal verify check has not performed normally after completion of write)
- When a time-out error occurs: A time-out error [C] is returned.
### 8.9.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
</tbody>
</table>
| Abnormal termination [B]       | Parameter error | 05H | • The specified start/end address is not the start/end address of the block.  
• The data length is under 2 words. |
|                                | Checksum error | 07H | The checksum of the transmitted command frame does not match. |
|                                | Protect error  | 10H | • Write is prohibited in the security setting.  
• Boot block cluster rewrite is prohibited in the security setting. |
|                                | Negative acknowledgment (NACK) | 15H | Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
| Time-out error [C]             | –            | The status frame was not received within the specified time. |
| Abnormal termination [D]       | Checksum error | 07H | The checksum of the transmitted command frame does not match. |
|                                | Write error   | 1CH (ST2) | A write error has occurred. |
| Abnormal termination [E]       | MRG11 error   | 1BH | An internal verify error has occurred. |
8.9.4 Flowchart

- Programming command processing
- Wait from previous frame reception until next command transmission
  - Command frame transmission processing (Programming)
  - Wait from command frame transmission until status check
    - Status check processing
      - Time-out error?
        - No
          - Normal completion?
            - Yes
            - Abnormal termination [B]
            - No
            - Time-out error [C]
          - No
          - Abnormal termination [B]
      - Yes
      - ST2 = ACK?
        - Yes
          - All data frames transmitted?
            - Yes
            - Abnormal termination [C]
            - No
            - Abnormal termination [D]
        - No
          - Abnormal termination [B]
      - No
        - Time-out error [C]
        - Abnormal termination [C]
      - Yes
        - Normal completion?
          - Yes
          - Normal completion [A]
          - No
          - Abnormal termination [B]

8.9.5 Sample program

The following shows a sample program for Programming command processing.

```c
u16 fl_csi_write(u32 top, u32 bottom)
{
    u16 rc;
    u32 send_head, send_size;
    bool is_end;
    u32 wt5, wt5_max;

    // set params
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL
    wt5     = make_wt5_min(get_block_num(top, bottom));
    wt5_max = make_wt5_max(get_block_num(top, bottom));

    // send command & check status
    fl_wait(tCOM);
    put_cmd_csi(FL_COM_WRITE, 7, fl_cmd_prm); // send "Programming" command
    fl_wait(tWT3);

    rc = fl_csi_getstatus(tWT3_TO); // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
    // case FLC_DFTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }

    // send user data
    send_head = top;

    while(1){
        if ((bottom - send_head) > 256){ // rest size > 256 ?
            is_end = false; // yes, not end frame
            send_size = 256; // transmit size = 256 byte
        }
        else{
            is_end = true;
            send_size = bottom - send_head + 1;
            // transmit size = (bottom - send_head)+1 byte
        }
    }
}
```
memcpy(fl_txdata_frm, rom_buf+send_head, send_size);
    // set data frame payload
send_head += send_size;

fl_wait(tFD3);   // wait before sending data frame
put_dfrm_csi(send_size, fl_txdata_frm, is_end);
    // send data frame (user data)
fl_wait(tWT4);    // wait

rc = fl_csi_getstatus(tWT4_MAX); // get status frame
switch(rc) {
    case FLC_NO_ERR:   break; // continue
    case FLC_DFTO_ERR: return rc; break; // case [C]
    default:  return rc; break; // case [B]
}
if (fl_st2 != FLST_ACK){  // ST2 = ACK ?
    rc = decode_status(fl_st2); // No
    return rc;   // case [D]
}
if (is_end)   // send all user data ?
    break;   // yes
    //continue;

/****************************************************/
/* Check internally verify                         */
/****************************************************/

fl_wait(wt5);    // wait

rc = fl_csi_getstatus(wt5_max); // get status frame
    //
switch(rc) {
    //
    case FLC_NO_ERR: return rc; break; // case [A]
    case FLC_DFTO_ERR: return rc; break; // case [C]
    default:  return rc; break; // case [E]
    //
}
return rc;

}
8.10 Verify Command

8.10.1 Processing sequence chart

Verify command processing sequence
8.10.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{COM} \)).
<2> The Verify command is transmitted by command frame transmission processing.
<3> Waits from command transmission until status check processing (wait time \( t_{WT6} \)).
<4> The status frame is acquired by status check processing.
<5> The following processing is performed according to the result of status check processing.

When the processing ends normally: Proceeds to <6>.
When the processing ends abnormally: Abnormal termination [B]
When a time-out error occurs: A time-out error [C] is returned.

<6> Waits from the previous frame reception until the next data frame transmission (wait time \( t_{FD3} \)).
<7> User data for verifying is transmitted by data frame transmission processing.
<8> Waits from data frame transmission until status check processing (wait time \( t_{WT7} \)).
<9> The status frame is acquired by status check processing.
<10> The following processing is performed according to the result of status check processing (status code (ST1/ST2)) (also refer to the processing sequence chart and flowchart).

When ST1 = abnormal termination: Abnormal termination [B]
When ST1 = time-out error: A time-out error [C] is returned.
When ST1 = normal completion: The following processing is performed according to the ST2 value.
  • When ST2 \( \neq \) ACK: Abnormal termination [D]
  • When ST2 = ACK: If transmission of all data frames is completed, the processing ends normally [A].
    If there still remain data frames to be transmitted, the processing re-executes the sequence from <6>.

8.10.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
<tr>
<td>Abnormal termination [D]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Verify error</td>
<td>0FH (ST2)</td>
</tr>
</tbody>
</table>
8.10.4 Flowchart

[Flowchart diagram]

Normal completion [A]

Time-out error [C]

Abnormal termination [B]

Abnormal termination [D]

Normal completion [A]

Time-out error [C]

Abnormal termination [B]

Abnormal termination [D]

Normal completion [A]

Time-out error [C]

Abnormal termination [B]

Abnormal termination [D]

Normal completion [A]

Time-out error [C]

Abnormal termination [B]

Abnormal termination [D]

Normal completion [A]

Time-out error [C]

Abnormal termination [B]

Abnormal termination [D]

Normal completion [A]

Time-out error [C]

Abnormal termination [B]

Abnormal termination [D]

Normal completion [A]

Time-out error [C]

Abnormal termination [B]

Abnormal termination [D]

Normal completion [A]

Time-out error [C]

Abnormal termination [B]

Abnormal termination [D]

Normal completion [A]

Time-out error [C]

Abnormal termination [B]

Abnormal termination [D]

Normal completion [A]
8.10.5 Sample program

The following shows a sample program for Verify command processing.

```c
/**
  * Verify command (CSI)
  */
/**
  * 
  * [i] u32 top ... start address
  *
  * [i] u32 bottom ... end address
  *
  * [i] u8 *buf ... pointer to verify data buffer
  *
  * [r] u16 ... error code
  */

u16 fl_csi_verify(u32 top, u32 bottom, u8 *buf)
{
  u16 rc;
  u32 send_head, send_size;
  bool is_end;

  // set params
  set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

  // send command & check status
  fl_wait(tCOM);
  put_cmd_csi(FL_COM_VERIFY, 7, fl_cmd_prm); // send "Verify" command
  fl_wait(tWT6);

  rc = fl_csi_getstatus(tWT6_MAX); // get status frame
  switch(rc) {
    case FLC_NO_ERR: break; // continue
    // case FLC_DFTO_ERR: return rc; break; // case [C]
    default: return rc; break; // case [B]
  }

  // send user data
  send_head = top;

  while(1){
    if ((bottom - send_head) > 256){ // rest size > 256 ?
      is_end = false; // yes, not end frame
      send_size = 256; // transmit size = 256 byte
    } else{
      is_end = true;
      send_size = bottom - send_head + 1; // transmit size = (bottom - send_head)+1 byte
    }
  }
```

memcpy(fl_txdata_frm, buf+send_head, send_size); // set data frame payload
send_head += send_size;

fl_wait(tFD3_CSI);   // wait before sending data frame
put_dfrm_csi(send_size, fl_txdata_frm, is_end);   // send data frame

fl_wait(tWT7);   // wait

rc = fl_csi_getstatus(tWT7_MAX); // get status frame
switch(rc) {
        case FLC_NO_ERR:    break; // continue
//        case FLC_DFTO_ERR:  return rc; break; // case [C]
        default:   return rc; break; // case [B]
}

if (fl_st2 != FLST_ACK) {  // ST2 = ACK ?
        rc = decode_status(fl_st2); // No
        return rc;  // case [D]
}

if (is_end) // send all user data ?
        break; // yes
// continue;

return FLC_NO_ERR;  // case [A]
8.11 Block Blank Check Command

8.11.1 Processing sequence chart

Block Blank Check command processing sequence

Programmer V850E/IG3

<1> Wait from previous frame reception until next command transmission

<2> Block Blank Check command frame transmission

<3> Wait from command frame transmission until status check

<4> Status check processing

<5> Result of status check processing

Result
[Normal completion/
Abnormal termination/
Time-out error]

Abnormal termination [B]

Normal completion

Blank check for all of specified blocks completed?
[Yes/No]

Yes

No

Go to <1>

Abnormal termination

Time-out error

Time-out error [C]

Time-out error

Normal completion [A]
8.11.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{COM}$).

<2> The Block Blank Check command is transmitted by command frame transmission processing.

<3> Waits from command transmission until status check processing (wait time $t_{WT8}$).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

When a time-out error occurs: A time-out error [C] is returned.
When the processing ends abnormally: Abnormal termination [B]
When the processing ends normally: If the blank check for all of the specified blocks is not yet completed, processing changes the number of blocks and re-executes the sequence from <1>.
If the blank check for all of the specified blocks is completed, the processing ends normally [A].

8.11.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
</tbody>
</table>
| Abnormal termination [B]      | Parameter error | 05H | • The specified start/end address is out of the flash memory range.  
• The specified start/end address is not the start/end address of the block. |
|                               | Checksum error | 07H | The checksum of the transmitted command frame does not match. |
|                               | Negative acknowledgment (NACK) | 15H | Command frame data is abnormal (such as invalid data length (LEN) or no ETX). |
|                               | MRG11 error | 1BH | The specified block in the flash memory is not blank. |
| Time-out error [C]            | – | The status frame was not received within the specified time. |
8.11.4 Flowchart

Block Blank Check command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Block Blank Check)

Wait from command frame transmission until status check

Status check processing

Time-out error?

Yes

Time-out error [C]

No

Normal completion?

Yes

Normal completion [A]

No

Blank check for all of specified blocks completed?

Yes

Abnormal termination [B]

No

Yes

No
8.11.5 Sample program

The following shows a sample program for Block Blank Check command processing for one block.

```c
/**
 * Block blank check command (CSI)
 */
/**
 * [i] u16 sblk ... start block number
 * [i] u16 eblk ... end block number
 * [r] u16 ... error code
 */

u16 fl_csi_blk_blank_chk(u16 sblk, u16 eblk)
{
    u16 rc;
    u32 wt8, wt8_max;
    u32 top, bottom;

    top = get_top_addr(sblk);  // get start address of start block
    bottom = get_bottom_addr(eblk); // get end address of end block

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    wt8 = make_wt8_min(sblk, eblk);  // get tWT8(Min)
    wt8_max = make_wt8_max(sblk, eblk);  // get tWT8(Max)

    fl_wait(tCOM);  // wait before sending command frame

    put_cmd_csi(FL_COM_BLOCK_BLANK_CHK, 7, fl_cmd_prm);  // send "Block Blank Check" command

    fl_wait(wt8);

    rc = fl_csi_getstatus(wt8_max);   // get status frame
    switch(rc) {
        //
        //        case FLC_NO_ERR: return rc; break; // case [A]
        //        case FLC_DFTO_ERR: return rc; break; // case [C]
        //        default: return rc; break; // case [B]
        //    }
    return rc;
}
```
8.12 Silicon Signature Command

8.12.1 Processing sequence chart

Silicon Signature command processing sequence

Programmer

1. Wait from previous frame reception until next command transmission

2. Silicon Signature command frame transmission

3. Wait from command frame transmission until status check

4. Status check processing

5. Result of status check processing

Result

[Normal completion/
Abnormal termination/
Time-out error]

V850E/IG3

6. Wait from previous frame reception until next data frame transmission

7. Data frame (silicon signature) reception processing

Normal completion [A]

No

Data frame error [D]

Yes

Normal data frame? [Yes/No]

Abnormal termination [B]

Time-out error

Time-out error [C]

Abnormal termination [B]
8.12.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{com}} \)).

<2> The Silicon Signature command is transmitted by command frame transmission processing.

<3> Waits from command transmission until status check processing (wait time \( t_{\text{WT1}} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

   When the processing ends normally: Proceeds to <6>.

   When the processing ends abnormally: Abnormal termination [B]

   When a time-out error occurs: A time-out error [C] is returned.

<6> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{FD2}} \)).

<7> The received data frame (silicon signature data) is checked.

   If data frame is normal: Normal completion [A]

   If data frame is abnormal: Data frame error [D]

8.12.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>Normal acknowledgment (ACK) The command was executed normally and the silicon signature was acquired normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>07H</td>
<td>Checksum error The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td></td>
<td>15H</td>
<td>Negative acknowledgment (NACK) Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as silicon signature data does not match.</td>
</tr>
</tbody>
</table>
8.12.4 Flowchart

- Silicon Signature command processing
  - Wait from previous frame reception until next command transmission
    - Command frame transmission processing (Silicon Signature)
      - Wait from command frame transmission until status check
        - Status check processing
          - Time-out error?
            - No
              - Normal completion?
                - Yes
                  - Normal completion [A]
                - No
                  - Abnormal termination [B]
                - Time-out error [C]
            - Yes
              - Normal data frame?
                - No
                  - Data frame error [D]
                - Yes
                  - Normal completion [A]
8.12.5 Sample program

The following shows a sample program for Silicon Signature command processing.

```c
/**
 * Get silicon signature command (CSI)
 */

u16 f1_csi_getsig(u8 *sig)
{
    u16 rc;

    fl_wait(tCOM); // wait before sending command frame

    put_cmd_csi(FL_COM_GET_SIGNATURE, 1, fl_cmd_prm); // send "Silicon
                                                        // Signature" command

    fl_wait(tWT11);

    rc = f1_csi_getstatus(tWT11_TO); // get status frame

    switch(rc) {
    case FLC_NO_ERR: break; // continue
    // case FLC_DFT0_ERR: return rc; break; // case [C]
    default: return rc; break; // case [B]
    }

    fl_wait(tFD2_SIG); // wait before getting data frame

    rc = get_dfrm_csi(fl_rxdata_frm); // get data frame (signature data)

    if (rc){ // if no error,
        return rc; // case [D]
    }

    memcpy(sig, fl_rxdata_frm+OFS_STA_PLD, fl_rxdata_frm[OFS_LEN]); // copy Signature data

    return rc; // case [A]
}
```
8.13 Version Get Command

8.13.1 Processing sequence chart

Version Get command processing sequence
8.13.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{COM}} \)).

<2> The Version Get command is transmitted by command frame transmission processing.

<3> Waits from command transmission until status check processing (wait time \( t_{\text{WT12}} \)).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

- When the processing ends normally: Proceeds to <6>.
- When the processing ends abnormally: Abnormal termination [B]
- When a time-out error occurs: A time-out error [C] is returned.

<6> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{FD2}} \)).

<7> The received data frame (version data) is checked.

- If data frame is normal: Normal completion [A]
- If data frame is abnormal: Data frame error [D]

8.13.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>The command was executed normally and version data was acquired normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>07H</td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td>Checksum error</td>
<td>15H</td>
<td>Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Negative acknowledgment (NACK)</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as version data does not match.</td>
</tr>
</tbody>
</table>
8.13.4 Flowchart

- **Version Get command processing**
  - Wait from previous frame reception until next command transmission
  - Command frame transmission processing (Version Get)
  - Wait from command frame transmission until status check
  - Status check processing
  - Time-out error?
    - Yes: Time-out error [C]
    - No: Normal completion? (Yes) Abnormal termination [B] (No)
  - Abnormal termination [B]
- Wait from previous frame reception until next data frame reception
- Data frame reception processing
  - Normal data frame?
    - Yes: Normal completion [A]
    - No: Data frame error [D]
8.13.5 Sample program

The following shows a sample program for Version Get command processing.

```c
u16 fl_csi_getver(u8 *buf)
{
    u16 rc;

    fl_wait(tCOM); // wait before sending command frame
    put_cmd_csi(FL_COM_GET_VERSION, 1, fl_cmd_prm); // send "Version Get" command
    fl_wait(tWT12);
    rc = fl_csi_getstatus(tWT12_TO); // get status frame
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        default: return rc; break; // case [B]
    }
    fl_wait(tFD2_VG); // wait before getting data frame
    rc = get_dfrm_csi(fl_rxdata_frm); // get version data
    if (rc){ // if no error,
        return rc; // case [D]
    }
    memcpy(buf, fl_rxdata_frm+OFS_STA_PLD, DFV_LEN); // copy version data
    return rc; // case [A]
}
```
8.14 Checksum Command

8.14.1 Processing sequence chart

Checksum command processing sequence

![Diagram of checksum command processing sequence]

**Diagram Notes:***
- **<1>** Wait from previous frame reception until next command transmission
- **<2>** Checksum command frame transmission
- **<3>** Wait from command frame transmission until status check
- **<4>** Status check processing
- **<5>** Result of status check processing
- **<6>** Wait from previous frame reception until next data frame reception
- **<7>** Data frame (checksum data) reception processing

**Flow Chart:**
- Normal completion
- Abnormal termination
- Time-out error

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8.14.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{COM}$).

<2> The Checksum command is transmitted by command frame transmission processing.

<3> Waits from command transmission until status check processing (wait time $t_{WT1}$).

<4> The status frame is acquired by status check processing.

<5> The following processing is performed according to the result of status check processing.

- When the processing ends normally: Proceeds to <6>.
- When the processing ends abnormally: Abnormal termination [B]
- When a time-out error occurs: A time-out error [C] is returned.

<6> Waits from the previous frame reception until the next command transmission (wait time $t_{F01}$).

<7> The received data frame (checksum data) is checked.

- If data frame is normal: Normal completion [A]
- If data frame is abnormal: Data frame error [D]

8.14.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>The command was executed normally and checksum data was acquired normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>05H</td>
<td>The specified start/end address is not a fixed address in block units (2 KB) starting from the top of the flash memory.</td>
</tr>
<tr>
<td>Checksum error</td>
<td>07H</td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
<td>Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as version data does not match.</td>
</tr>
</tbody>
</table>
8.14.4 Flowchart

1. **Checksum command processing**
2. **Wait from previous frame reception until next command reception**
3. **Command frame transmission processing (Checksum)**
4. **Wait from command frame transmission until status check**
5. **Status check processing**
6. **Time-out error?**
   - No
     - **Normal completion?**
       - Yes
         - Abnormal termination [B]
       - No
         - **Wait from previous frame reception until next data frame reception**
7. **Data frame reception processing**
8. **Normal data frame?**
   - No
     - **Normal completion [A]**
   - Yes
     - **Normal completion [A]**
8. **Data frame error [D]**
8.14.5 Sample program

The following shows a sample program for Checksum command processing.

```c
/**
 * Get checksum command (CSI)
 */
/**
 * [i] u16 *sum ... pointer to checksum save area
 * [i] u32 top ... start address
 * [i] u32 bottom ... end address
 * [r] u16 ... error code
 */
u16 fl_csi_getsum(u16 *sum, u32 top, u32 bottom)
{
    u16 rc;
    u32 fd1;

    /******************************************************************************/
    /* set params */
    /******************************************************************************/
    // set params
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL
    fd1 = get_fd1(get_block_num(top, bottom)); // get tFD1(Min)

    /******************************************************************************/
    /* send command */
    /******************************************************************************/
    fl_wait(tCOM); // wait before sending command frame
    put_cmd_csi(FL_COM_GET_CHECK_SUM, 7, fl_cmd_prm); // send "Checksum" command
    fl_wait(tWT16);
    rc = fl_csi_getstatus(tWT16_TO); // get status frame
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

    /******************************************************************************/
    /* get data frame (Checksum data) */
    /******************************************************************************/
    fl_wait(fd1);
    rc = get_dfrm_csi(fl_rxdata_frm); // get data frame(version data)
    if (rc){ // if error,
        return rc; // case [D]
    }

    *sum = (fl_rxdata_frm[OFS_STA_PLD] << 8) + fl_rxdata_frm[OFS_STA_PLD+1]; // set SUM data
    return rc; // case [A]
}
```
8.15 Security Set Command

8.15.1 Processing sequence chart

Security Set command processing sequence
8.15.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{com}$).
<2> The Security Set command is transmitted by command frame transmission processing.
<3> Waits from command transmission until status check processing (wait time $t_{WT13}$).
<4> The status frame is acquired by status check processing.
<5> The following processing is performed according to the result of status check processing.

- When the processing ends normally: Proceeds to <6>.
- When the processing ends abnormally: Abnormal termination [B]
- When a time-out error occurs: A time-out error [C] is returned.

<6> Waits from the previous frame reception until the data frame transmission (wait time $t_{FD3}$).
<7> The data frame (security setting data) is transmitted by data frame transmission processing.
<8> Waits from data frame transmission until status check processing (wait time $t_{WT14}$).
<9> The status frame is acquired by status check processing.
<10> The following processing is performed according to the result of status check processing.

- When the processing ends normally: Proceeds to <11>.
- When the processing ends abnormally: Abnormal termination [D]
- When a time-out error occurs: A time-out error [C] is returned.

<11> Waits until status acquisition (completion of internal verify) (wait time $t_{WT15}$).
<12> The status frame is acquired by status check processing.
<13> The following processing is performed according to the result of status check processing.

- When the processing ends normally: Normal completion [A]
- When the processing ends abnormally: Abnormal termination [E]
- When a time-out error occurs: A time-out error [C] is returned.

8.15.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Processing timed out due to the busy status at the HS pin.</td>
</tr>
</tbody>
</table>
### Status at Processing Completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abnormal termination [D]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td>Checksum error</td>
<td>07H</td>
<td>The checksum of the transmitted command frame or data frame does not match.</td>
</tr>
</tbody>
</table>
| Protect error                  | 10H         | • An attempt was made to enable a flag that was already prohibited in the setting.  
• An attempt was made to change the last block number of the boot block cluster in the state that boot block cluster rewrite is prohibited. |
| MRG10 error                    | 1AH         | A write error has occurred.                                                |
| Write error                    | 1CH         |                                             |
| Abnormal termination [E]       | MRG11 error | 1BH  | An internal verify error has occurred.                                      |
8.15.4 Flowchart
8.15.5 Sample program
The following shows a sample program for Security Set command processing.

```c
/**
 * Set security flag command (CSI)
 */
/**
 * [i] u8 scf ... Security flag data
 * [i] u8 bot ... Boot Block Number
 * [r] u16 ... error code
 */

u16 fl_csi_setscf(u8 scf, u8 bot)
{
    u16 rc;
    fl_cmd_prm[0] = 0x00;   // "BLK" (must be 0x00)
    fl_cmd_prm[1] = 0x00;   // "PAG" (must be 0x00)
    fl_txdata_frm[0] = scf|= 0b11100000; // "FLG" (bit 7,6,5,4 must be '1')
    fl_txdata_frm[1] = bot;   // "BOT"

    fl_wait(tCOM);   // wait before sending command frame
    put_cmd_csi(FL_COM_SET_SECURITY, 3, fl_cmd_prm);// send "Security Set" command
    fl_wait(tFD3);  // wait before getting data frame
    put_dfrm_csi(2, fl_txdata_frm, true); // send data frame(Security data)
    fl_wait(tWT14);
    rc = fl_csi_getstatus(tWT14_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }
}
```
default: return rc; break; // case [B]

/* Check internally verify */
/***************************************************/
fl_wait(tWT15);

rc = fl_csi_getstatus(tWT15_MAX); // get status frame
switch(rc) {
    case FLC_NO_ERR: return rc; break; // case [A]
    case FLC_DFTO_ERR: return rc; break; // case [C]
    default: return rc; break; // case [B]
}
return rc;
8.16 Read Command

8.16.1 Processing sequence chart

Read command processing sequence

Programmer V850E/IG3

1. Wait from previous frame reception until next command transmission

2. Read command frame transmission

3. Wait from command frame transmission until status check

4. Status check processing

5. Result of status check processing

6. Wait until data frame reception

7. Data frame (user data) processing

8. Processing of data frame reception completed normally?

9. Status frame (NACK) transmission

10. Wait from previous frame reception until next status frame transmission

11. Status frame (ACK) transmission

Time-out error

Abnormal termination

Normal completion

Abnormal termination

Data frame error

All data frames received?

Yes

No

To <6>

Normal completion [A]
8.16.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{\text{COM}}$).
<2> The Read command is transmitted by command frame transmission processing.
<3> Waits from command transmission until status check processing (wait time $t_{\text{WT1}}$).
<4> The status frame is acquired by status check processing.
<5> The following processing is performed according to the result of status check processing.

When the processing ends normally:  Proceeds to <6>.
When the processing ends abnormally: Abnormal termination [B]
When a time-out error occurs:  A time-out error [C] is returned.

<6> Waits from the previous frame reception until the data frame reception (wait time $t_{\text{WT1}}$).
<7> The data frame (user data) is received by data frame reception processing.
The following processing is performed according to the result of reception processing.

When the processing ends normally:  Proceeds to <10>.
When the processing ends abnormally:  Proceeds to <8>.

<8> Waits from the previous frame reception until the next status (NACK) frame transmission (wait time $t_{\text{WT1}}$).
<9> The NACK frame is transmitted by data frame transmission processing.
A data frame error [D] is returned.
<10> Waits from the previous frame reception until the next status (ACK) frame transmission (wait time $t_{\text{WT1}}$).
<11> The ACK frame is transmitted by data frame transmission processing.
When reception of all data frames is completed, the normal completion status [A] is returned.
If there still remain data frames to be received, the sequence is re-executed from <5>.

8.16.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame or data frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as read data does not match.</td>
</tr>
</tbody>
</table>
8.16.4 Flowchart
8.16.5 Sample program

The following shows a sample program for Read command processing.

```c
u16 fl_csi_read(u32 top, u32 bottom)
{
  u16 rc;
  u32 read_head;
  u16 len;
  u8 hooter;

  set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

  fl_wait(tCOM);  // wait before sending command
  put_cmd_csi(FL_COM_READ, 7, fl_cmd_prm); // send "Read" command
  fl_wait(tWT17);   // wait
  rc = fl_csi_getstatus(tWT17_TO);  // get status frame
  switch(rc) {
    case FLC_NO_ERR:    break; // continue
    default:   return rc; break; // case [B]
  }

  read_head = top;
  while(1){
    fl_wait(tWT18);
    rc = get_dfrm_csi(fl_rxdata_frm);  // get ROM data from FLASH
    switch(rc) {
      case FLC_NO_ERR:    break; // continue
      case FLC_RX_DFSUM_ERR: // case [D]
        fl_wait(tWT19);
        put_sfrm_csi(FLST_NACK); // send status(NACK) frame
        return rc;
        break;
      default: // case [C]
        return rc;
        break;
    }
  }
  fl_wait(tWT19);
  put_sfrm_csi(FLST_ACK); // send status(ACK) frame
}
```
/*********************************************/ /* save ROM data */ /*********************************************/
if ((len = fl_rxdata_frm[OFS_LEN]) == 0) // get length
    len = 256;
memcpy(read_buf+read_head, fl_rxdata_frm+2, len); // save to external RAM
read_head += len;

/*********************************************/ /* end check */ /*********************************************/
hooter = fl_rxdata_frm[len + 3];
if (hooter == FL_ETB) // end frame ?
    continue; // no
break; // yes

return FLC_NO_ERR;
}
CHAPTER 9 FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS

This chapter describes the parameter characteristics between the programmer and the V850E/IG3 in the flash memory programming mode. Be sure to refer to the user’s manual of the V850E/IG3 for the electrical specifications when designing with a programmer.

<Operating clock>
The V850E/IG3 performs multiplication processing immediately after reset, to change the main clock frequency (fXX) to the a frequency eight times the main clock oscillation frequency (fx).

- 4.0 MHz ≤ fx ≤ 8.0 MHz: fXX = fx × 8 (PLL mode)

9.1 Flash Memory Programming Mode Setting Time
(TA = −40 to +85°C, VDD0 = VDD1 = EVDD0 = EVDD1 = EVDD2 = AVDD0 = AVDD1 = AVDD2 = AVREFP0 = AVREFP1, VSS0 = VSS1 = EVSS0 = EVSS1 = EVSS2 = AVSS0 = AVSS1 = AVSS2 = 0 V, CL = 50 pF)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD↑ to FLMD0↑</td>
<td>tDP</td>
<td></td>
<td>1 ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FLMD0↑ to RESET↑</td>
<td>tPR</td>
<td></td>
<td>2 ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Count start time from RESET↑ to FLMD0↑↑↑↑</td>
<td>tRP</td>
<td></td>
<td>132356/fXX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Count finish time from RESET↑ to FLMD0↑↑↑↑</td>
<td>tRPE</td>
<td></td>
<td>749028/fXX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FLMD0 counter high-level width/low-level width</td>
<td>tPW</td>
<td></td>
<td>10 μs</td>
<td>100 μs</td>
<td></td>
</tr>
<tr>
<td>Wait for Reset command</td>
<td>tRC</td>
<td>CSI, CSI + HS</td>
<td>1059034/fXX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for low level (data 1)</td>
<td>tR1</td>
<td>UART</td>
<td>1059034/fXX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for low level (data 2)</td>
<td>tR2</td>
<td>UART</td>
<td>30,000/fXX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for Reset command</td>
<td>tRC</td>
<td>UART</td>
<td>30,000/fXX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low level width (data 1)</td>
<td>tL1</td>
<td>UART</td>
<td>Note 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low level width (data 2)</td>
<td>tL2</td>
<td>UART</td>
<td>Note 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FLMD0 counter rise time</td>
<td>tR</td>
<td></td>
<td>1 μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FLMD0 counter fall time</td>
<td>tF</td>
<td></td>
<td>1 μs</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes
1. (tRP + tRPE)/2 is recommended as the standard value for the FLMD0 pin signal input timing.
2. The low-level width is the same as the 00H data width at 9,600 bps.
### 9.2 Programming characteristics

\((T_A = -40 \text{ to } +85^\circ C, \ V_{D0} = V_{D1} = E_{VDD0} = E_{VDD1} = A_{VDD0} = A_{VDD1} = A_{VREFP0} = A_{VREFP1},\ V_{SS0} = V_{SS1} = E_{VSS0} = E_{VSS1} = A_{VSS0} = A_{VSS1} = A_{VSS2} = 0 \ V, CL = 50 \ pF)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Condition</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data frame to Data frame</td>
<td>(t_{DR})</td>
<td>Receive data frame</td>
<td>CSI, CSI + HS</td>
<td>237/f&lt;sub&gt;XX&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td></td>
<td>237/f&lt;sub&gt;XX&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(t_{DT})</td>
<td>Send data frame</td>
<td>CSI, CSI + HS</td>
<td>209/f&lt;sub&gt;XX&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status command frame reception to status frame transmission</td>
<td>(t_{SF})</td>
<td>CSI, CSI + HS</td>
<td></td>
<td>1,901/f&lt;sub&gt;XX&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>Status frame transmission to data frame transmission (1)</td>
<td>(t_{D1})</td>
<td>CSI, CSI + HS</td>
<td>1,410/f&lt;sub&gt;XX&lt;/sub&gt; + 121,563/f&lt;sub&gt;XX&lt;/sub&gt; × M + 15 (\mu s)</td>
<td>1,692/f&lt;sub&gt;XX&lt;/sub&gt; + 145,876/f&lt;sub&gt;XX&lt;/sub&gt; × M + 18 (\mu s)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status frame transmission to data frame transmission (2)</td>
<td>(t_{D2})</td>
<td>CSI, CSI + HS</td>
<td>3,774/f&lt;sub&gt;XX&lt;/sub&gt; + 30 (\mu s)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status frame transmission to data frame reception (3)</td>
<td>(t_{D3})</td>
<td>CSI, CSI + HS</td>
<td>1,206/f&lt;sub&gt;XX&lt;/sub&gt; + 14 (\mu s)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td></td>
<td>1,206/f&lt;sub&gt;XX&lt;/sub&gt; + 14 (\mu s)</td>
<td></td>
</tr>
<tr>
<td>Status frame transmission to command frame reception</td>
<td>(t_{COM})</td>
<td>–</td>
<td></td>
<td>842/f&lt;sub&gt;XX&lt;/sub&gt; + 2 (\mu s)</td>
<td></td>
</tr>
</tbody>
</table>

**Note** Successive reception must be enabled for the programmer. Set the programmer time-out time to 3 seconds or more.

**Remarks**

1. \(M\): Number of blocks
   
   \(f_{XX}\): Main clock frequency

2. The waits are defined as follows.
   
   \(<t_{DR}, t_{D2}, t_{COM}>\)
   
   The V850E/IG3 is readied for the next communication after the MIN. time has elapsed after completion of the previous communication.
   
   The programmer must transmit the next data after the MIN. time has elapsed after completion of the previous communication.
   
   \(<t_{DT}, t_{SF}, t_{D2}>\)
   
   The V850E/IG3 is readied for the next communication after the MIN. time has elapsed after completion of the previous communication.
   
   The programmer must receive the next data after the MIN. time has elapsed after completion of the previous communication.
   
   In CSI communication, the programmer must issue the Status command after the MIN. time has elapsed. If ACK is not returned, do not repeat the status check and execute the error processing (time-out processing, etc.).

3. \(<t_{D1}>\)
   
   The V850E/IG3 completes each command processing between the MIN. and MAX. times. If the V850E/IG3 does not complete each command processing after the MAX. time has elapsed, execute the error processing (time-out processing, etc.).
   
   In CSI communication, the programmer must repeat the status check from the MIN. time to MAX. time.
   
   In UART communication, the V850E/IG3 transmits the status frame between the MIN. and MAX. times.
## 9.3 Command characteristics

\( (Ta = -40 \text{ to } +85 ^\circ C, \ V_{DD0} = V_{DD1} = EV_{DD0} = EV_{DD1} = AV_{DD0} = AV_{DD1} = AV_{DD2} = AV_{REFP0} = AV_{REFP1}, \ V_{SS0} = V_{SS1} = EV_{SS0} = EV_{SS1} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0 \ V, \ C_L = 50 \ pF) \)

### Table 9.3-1 Command characteristics

<table>
<thead>
<tr>
<th>Command</th>
<th>Symbol</th>
<th>Condition</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>tWT0</td>
<td>CSI, CSI + HS</td>
<td>(318/f_{XX})</td>
<td>(315,552,246/f_{XX} + 3,233,272 \mu s)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td>Chip Erase</td>
<td>tWT1</td>
<td>–</td>
<td>(16,054,356/f_{XX} + 152,160 \mu s)</td>
<td>(315,552,246/f_{XX} + 3,233,272 \mu s)</td>
</tr>
<tr>
<td>Block Erase</td>
<td>tWT2</td>
<td>–</td>
<td>(4,642/f_{XX} + 15 \mu s + (1,715 \mu s + 12,089 \mu s + 109,665/f_{XX} \times BM + 960 \mu s \times BM) \times (\text{Note 2}))</td>
<td>(5,851/f_{XX} + 30 \mu s + (29,652 \mu s + 241,767 \mu s + 2,193,284/f_{XX} \times BM + 19,200 \mu s \times BM) \times (\text{Note 2}))</td>
</tr>
<tr>
<td>Program</td>
<td>tWT3</td>
<td>CSI, CSI + HS</td>
<td>(3,394/f_{XX} + 30 \mu s)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT4</td>
<td>–</td>
<td>(46,542/f_{XX} + 3,368 \mu s)</td>
<td>(1,009,757/f_{XX} + 54,079 \mu s)</td>
</tr>
<tr>
<td></td>
<td>tWT5</td>
<td>CSI, CSI + HS</td>
<td>(1,572/f_{XX} + 2 \mu s + (285,025/f_{XX} + 2,122 \mu s) \times M)</td>
<td>(1,887/f_{XX} + 3 \mu s + (342,030/f_{XX} + 2,579 \mu s) \times M)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note 4</td>
<td></td>
</tr>
<tr>
<td>Verify</td>
<td>tWT6</td>
<td>CSI, CSI + HS</td>
<td>(567/f_{XX})</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT7</td>
<td>CSI, CSI + HS</td>
<td>(21,122/f_{XX} + 122 \mu s)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note 5</td>
<td></td>
</tr>
<tr>
<td>Block Blank Check</td>
<td>tWT8</td>
<td>–</td>
<td>(2,262/f_{XX} + 16 \mu s (113,314/f_{XX} + 960 \mu s) \times M)</td>
<td>(2,715/f_{XX} + 20 \mu s (135,977/f_{XX} + 1,152 \mu s) \times M)</td>
</tr>
<tr>
<td>Oscillating Frequency Set</td>
<td>tWT9</td>
<td>CSI, CSI + HS</td>
<td>(965/f_{XX})</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td>Note 1</td>
<td></td>
</tr>
</tbody>
</table>

### Notes

1. Reception must be enabled for the programmer before command frame transmission. Set the programmer time-out time to 3 seconds or more.
2. When how many times the simultaneous selection processing is repeated is indicated by BN, perform the calculation in the parentheses, as shown in the Example below.
   **Example** When executing simultaneous processing with changing block size from \(2 \rightarrow 4 \rightarrow 8\)
   
   (Block Erase command’s MIN. value) \((BN = 3)\)
   
   \[
   \frac{4642}{f_{XX}} + 15 \mu s + (\frac{1715}{f_{XX}} + 12089 \mu s + 109665/f_{XX} \times 2 + 960 \mu s \times 2) \\
   + (\frac{1715}{f_{XX}} + 12089 \mu s + 109665/f_{XX} \times 4 + 960 \mu s \times 4) \\
   + (\frac{1715}{f_{XX}} + 12089 \mu s + 109665/f_{XX} \times 8 + 960 \mu s \times 8)
   \]

3. 64-word units
4. Successive reception must be enabled for the programmer. Set the programmer time-out time to 3 seconds or more.
5. Reception must be enabled for the programmer before data frame transmission. Set the programmer time-out time to 3 seconds or more.

### Remark

- **M**: Number of blocks
- **BM**: Number of blocks to be selected and processed simultaneously (blocks)
- **BN**: Number of executions of simultaneous selection and processing (number of repetitions of addition in the parentheses in Table above)
- **f_{XX}**: Main clock frequency
(TA = −40 to +85°C, VDD0 = VDD1 = EVDD0 = EVDD1 = EVDD2 = AVDD0 = AVDD1 = AVDD2 = AVREFP0 = AVREFP1, VSS0 = VSS1 = EVSS0 = EVSS1 = EVSS2 = AVSS0 = AVSS1 = AVSS2 = 0 V, CL = 50 pF)

<table>
<thead>
<tr>
<th>Command</th>
<th>Symbol</th>
<th>Condition</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud Rate Set</td>
<td>tWT10</td>
<td>UART</td>
<td>3,361/fxx</td>
<td></td>
</tr>
<tr>
<td>Silicon Signature</td>
<td>tWT11</td>
<td>CSI, CSI + HS</td>
<td>772/fxx</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td></td>
<td>Note 1</td>
</tr>
<tr>
<td>Version Get</td>
<td>tWT12</td>
<td>CSI, CSI + HS</td>
<td>797/fxx</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td></td>
<td>Note 1</td>
</tr>
<tr>
<td>Security Setting</td>
<td>tWT13</td>
<td>CSI, CSI + HS</td>
<td>665/fxx</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td></td>
<td>Note 1</td>
</tr>
<tr>
<td></td>
<td>tWT14</td>
<td>−</td>
<td>143,252/fxx + 1,990 μs</td>
<td>2,478,131/fxx + 270,801 μs</td>
</tr>
<tr>
<td></td>
<td>tWT15</td>
<td>CSI, CSI + HS</td>
<td>381,091/fxx + 15,214 μs</td>
<td>2,493,904/fxx + 263,132 μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td></td>
<td>Note 2</td>
</tr>
<tr>
<td>Checksum</td>
<td>tWT16</td>
<td>CSI, CSI+HS</td>
<td>944/fxx</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td></td>
<td>Note 1</td>
</tr>
<tr>
<td>Read</td>
<td>tWT17</td>
<td>CSI, CSI + HS</td>
<td>2,066/fxx + 15 μs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td></td>
<td>Note 1</td>
</tr>
<tr>
<td></td>
<td>tWT18&lt;sup&gt;Note 3&lt;/sup&gt;</td>
<td>CSI, CSI + HS</td>
<td>17,849/fxx + 14 μs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UART</td>
<td></td>
<td>Note 4</td>
</tr>
<tr>
<td></td>
<td>tWT19</td>
<td>−</td>
<td>216/fxx</td>
<td></td>
</tr>
</tbody>
</table>

Notes 1. Reception must be enabled for the programmer before command frame transmission. Set the programmer time-out time to 3 seconds or more.

2. Successive reception must be enabled for the programmer. Set the programmer time-out time to 3 seconds or more.

3. 64-word units

4. Reception must be enabled for the programmer before status frame transmission. Set the programmer time-out time to 3 seconds or more.

5. Wait for ACK code of the status frame from the programmer

Remark  fxx: Main clock frequency

<sup>tWT0 to tWT9, tWT11 to tWT19</sup>

- Parameter that both MIN. and MAX. values were specified
  The V850E/IG3 completes each command processing between the MIN. and the MAX. times. If the V850E/IG3 does not complete each command processing after the MAX. time has elapsed, execute the error processing (time-out processing, etc.).
  In CSI communication, the programmer must repeat the status check from the MIN. time to the MAX. time.
  In UART communication, the V850E/IG3 transmits the status frame between the MIN. and the MAX. times.

- Parameter that only MIN. value was specified
  In CSI communication, the programmer must issue the Status command after the MIN. time has elapsed. If ACK is not returned, do not repeat the status check and execute the error processing (time-out processing, etc.).

<sup>tWT10</sup>

The V850E/IG3 is readied for the next communication after the MIN. time has elapsed after completion of the
previous communication. The programmer must transmit the next data after the MIN. time has elapsed after completion of the previous communication.

9.4 UART Communication Mode

(a) Data frame

(b) Programming mode setting

(c) Reset command

(d) Chip Erase command/Block Erase command/Block Blank Check command/Oscillating Frequency Set command

Remark

TxD: TXDA0
RxD: RXDA0
(e) Baud Rate Set command

(f) Silicon Signature command/Version Get command

(g) Checksum command

(h) Programming command

Remark  
TxD: TXDA0  
RxD: RXDA0
(i) Verify command

- Command frame
- Status frame
- Data frame (1)
- Status frame (1)

(j) Security Set command

- Command frame
- Status frame
- Data frame
- Status frame
- Status frame

(k) Read command

- Command frame
- Status frame
- Data frame (1)
- Status frame (1)

(l) Wait before command frame transmission

- Status frame
- Command frame

Remark

- TxD: TXDA0
- RxD: RXDA0
9.5 3-Wire Serial I/O Communication Mode

(a) Data frame

(b) Programming mode setting

(c) Reset command

(d) Chip Erase command/Block Erase command/Block Blank Check command/Oscillating Frequency Set command

(e) Silicon Signature command/Version Get command

Remark

Scr: SCKB0
SO: SOB0
SI: SIB0
(f) Checksum command

(g) Programming command

(h) Verify command

Remark
SCK: SCKB0
SO: SOB0
SI: SIB0
(i) Security Setting command

(ii) Read command

(k) Wait before command frame transmission

Remark

| SCK: SCKB0 |
| SO: SOB0 |
| SI: SIB0 |
9.6 Simultaneous selection block processing

The block erasure, blank check, and internal verification functions are executed by repeating “simultaneous selection and processing”, which processes multiple blocks simultaneously.

The wait time is therefore equal to the total execution time of “simultaneous selection and processing”.

To calculate the total execution time of simultaneous selection and processing, the execution count (BN) and the number of blocks (BM) to be selected and processed simultaneously must first be calculated.

(1) Number of blocks (BM) and execution count (BN) of the simultaneous selection and processing

BN is calculated by obtaining the number of blocks to be processed simultaneously (BM: number of blocks to be selected and processed simultaneously).

The number of blocks to be selected and processed simultaneously (BM) should be 1, 2, 4, 8, 16, 32, 64, or 128, depending on which satisfies all of the following conditions.

[Condition 1]
Number of blocks (ER_BKNUM) processed ≥ Potential number of blocks to be selected and processed simultaneously (SSER_BKNUM)

[Condition 2]
Start block number (ST_BKNO) / Potential number of blocks to be selected and processed simultaneously (SSER_BKNUM) = Remainder is 0

[Condition 3]
The maximum value among the values that satisfy both Conditions 1 and 2

Example of simultaneous selection block processing that satisfies Conditions 1, 2, and 3 is shown below.
Example 1  Processing blocks 1 to 127

<1> The first start block number is 1 and the number of blocks to be processed is 127, so the values that satisfy Condition 1 are as follows.
   1, 2, 4, 8, 16, 32, 64
   The value that satisfies Condition 2 is as follows.
   1
   The value that satisfies Condition 3 is therefore 1, so the number of blocks to be selected and processed simultaneously (BM) is 1. Thus only block 1 is processed.

<2> After block 1 is processed, the next start block number is 2 and the number of blocks to be processed is 126, so the values that satisfy Condition 1 are as follows.
   1, 2, 4, 8, 16, 32, 64
   The values that satisfy Condition 2 are as follows.
   1, 2
   The value that satisfies Condition 3 is therefore 2, so the number of blocks to be selected and processed simultaneously (BM) is 2. Thus blocks 2 and 3 are processed.

<3> After blocks 2 and 3 are processed, the next start block number is 4 and the number of blocks to be processed is 124, so the values that satisfy Condition 1 are as follows.
   1, 2, 4, 8, 16, 32, 64
   The values that satisfy Condition 2 are as follows.
   1, 2, 4
   The value that satisfies Condition 3 is therefore 4, so the number of blocks to be selected and processed simultaneously (BM) is 4. Thus blocks 4 to 7 are processed.

<4> After blocks 4 to 7 are processed, the next start block number is 8 and the number of blocks to be processed is 120, so the values that satisfy Condition 1 are as follows.
   1, 2, 4, 8, 16, 32, 64
   The values that satisfy Condition 2 are as follows.
   1, 2, 4, 8
   The value that satisfies Condition 3 is therefore 8, so the number of blocks to be selected and processed simultaneously (BM) is 8. Thus blocks 8 to 15 are processed.

<5> After blocks 8 to 15 are processed, the next start block number is 16 and the number of blocks to be processed is 112, so the values that satisfy Condition 1 are as follows.
   1, 2, 4, 8, 16, 32, 64
   The values that satisfy Condition 2 are as follows.
   1, 2, 4, 8, 16
   The value that satisfies Condition 3 is therefore 16, so the number of blocks to be selected and processed simultaneously (BM) is 16. Thus blocks 16 to 31 are processed.

<6> After blocks 16 to 31 are processed, the next start block number is 32 and the number of blocks to be processed is 96, so the values that satisfy Condition 1 are as follows.
   1, 2, 4, 8, 16, 32, 64
   The values that satisfy Condition 2 are as follows.
   1, 2, 4, 8, 16, 32
   The value that satisfies Condition 3 is therefore 32, so the number of blocks to be selected and processed simultaneously (BM) is 32. Thus blocks 32 to 63 are processed.
After blocks 32 to 63 are processed, the next start block number is 64 and the number of blocks to be processed is 64, so the values that satisfy Condition 1 are as follows.

1, 2, 4, 8, 16, 32, 64

The values that satisfy Condition 2 are as follows.

1, 2, 4, 8, 16, 32, 64

The value that satisfies Condition 3 is therefore 64, so the number of blocks to be selected and processed simultaneously (BM) is 64. Thus blocks 64 to 127 are processed.

Therefore, simultaneous selection and processing is executed seven times (1, 2 and 3, 4 to 7, 8 to 15, 16 to 31, 32 to 63, and 64 to 127) to erase blocks 1 to 127, so BN = 7 is obtained.
Example 2  Processing blocks 5 to 10

<1> The first start block number is 5 and the number of blocks to be processed is 6, so the values that satisfy Condition 1 are as follows.
   1, 2, 4
   The value that satisfies Condition 2 is as follows.
   1
   The value that satisfies Condition 3 is therefore 1, so the number of blocks to be selected and processed simultaneously (BM) is 1. Thus only block 5 is processed.

<2> After block 5 is processed, the next start block number is 6 and the number of blocks to be processed is 5, so the values that satisfy Condition 1 are as follows.
   1, 2, 4
   The values that satisfy Condition 2 are as follows.
   1, 2
   The value that satisfies Condition 3 is therefore 2, so the number of blocks to be selected and processed simultaneously (BM) is 2. Thus blocks 6 and 7 are processed.

<3> After blocks 6 and 7 are processed, the next start block number is 8 and the number of blocks to be processed is 3, so the values that satisfy Condition 1 are as follows.
   1, 2
   The values that satisfy Condition 2 are as follows.
   1, 2
   The value that satisfies Condition 3 is therefore 2, so the number of blocks to be selected and processed simultaneously (BM) is 2. Thus blocks 8 and 9 are processed.

<4> After blocks 8 and 9 are processed, the next start block number is 10 and the number of blocks to be processed is 1, so the value that satisfies Condition 1 is as follows.
   1
   This also satisfies Conditions 2 and 3, so the number of blocks to be selected and processed simultaneously (BM) is 1. Thus block 10 is processed.

Therefore, simultaneous selection and processing is executed four times (5, 6 and 7, 8 and 9, and 10) to erase blocks 5 to 10, so BN = 4 is obtained.
An example of how to obtain BM and BN satisfying Conditions 1, 2, and 3 is illustrated in the following flowchart.

![Flowchart](image)

**Remark**
- ST_BKNO: Start block number
- END_BKNO: End block number
- ER_BKNUM: Number of blocks to be erased
- SSER_BKNUM: Potential number of blocks to be selected and processed simultaneously
- BM: Number of blocks to be selected and processed simultaneously
- BN: Number of executions of simultaneous selection and processing
APPENDIX A  CIRCUIT DIAGRAM (REFERENCE)

Figure A-1 shows a circuit diagram of the programmer and the V850E/IG3, for reference.
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