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April 1st, 2010
Renesas Electronics Corporation

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This manual explains the sample program functions of the 16-bit timer/event counter Q (TMQ) for the V850E/IA4 microcontroller.

The explanations are based on usage with the V850E/IA4 microcontroller. Refer to this manual when using the V850E/IA3, V850ES/IK1, and V850ES/IE2 microcontrollers.

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NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN
Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

② HANDLING OF UNUSED INPUT PINS
Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD
A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION
Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE
In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.
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INTRODUCTION

Cautions 1. Download the program used in this manual from the NEC Electronics Website (http://www.necel.com/).

2. When using this sample program, reference the following startup file and link directive file and adjust them if as necessary.
   • Startup file: IA4_start.s
   • Link directive file: IA4_link.dir
Conventions  The function lists are structured as follows.

### Hardware name (symbol)

| [Function(s)] | Function description |
| [Function name] | Name of sample function |
| [Argument(s)] | Type and overview of argument(s) |
| [Processing content] | Processing content of sample function |
| [Starting method] | Conditions for calling a function |
| [SFR(s) used] | Register name and setting content |
| [call function(s)] | Name and function of call function(s) |
| [Variable(s)] | Type, name, and overview of variable(s) used in sample function |
| [Interrupt(s)] | Name of function |
| [Interrupt source(s)] | Name |
| [File name] | Name of corresponding sample program file |
| [Caution(s)] | Caution(s) up on function usage |

### Interrupt function

| [Function name] | Name of interrupt function |
| [Overview] | Processing content |
| [Factor(s)] | Name of interrupt and conditions for occurrence |
| [call function(s)] | None |
| [Variable(s)] | Name of variable, function |
| [File name] | Name of corresponding sample program file |
| [Caution(s)] | None |
**Product Differences**

The differences between the V850E/IA4 and the V850E/IA3, V850ES/IK1, and V850ES/IE2 related to the 16-bit timer/event counter Q (TMQ) are shown below.

<table>
<thead>
<tr>
<th>Item</th>
<th>V850E/IA4</th>
<th>V850E/IA3</th>
<th>V850ES/IK1</th>
<th>V850ES/IE2</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOQ10 pin</td>
<td>Provided</td>
<td>Not provided</td>
<td>Provided</td>
<td></td>
</tr>
<tr>
<td>TRGQ0 pin</td>
<td>Provided</td>
<td>Provided</td>
<td>Not provided</td>
<td></td>
</tr>
<tr>
<td>TOQH01 to TOQH03 pins</td>
<td>Not provided</td>
<td>Not provided</td>
<td>Provided</td>
<td></td>
</tr>
<tr>
<td>TOQ00 pin</td>
<td>TOQ00</td>
<td>TOQ00</td>
<td>TOQ00 (CLMER)</td>
<td></td>
</tr>
<tr>
<td>Count clock</td>
<td>fxx/2, fxx/4, fxx/8, fxx/16, fxx/32, fxx/64, fxx/128, fxx/256</td>
<td>fxx/2, fxx/4, fxx/8, fxx/16, fxx/32, fxx/64, fxx/128, fxx/256</td>
<td>fxx, fxx/2, fxx/4, fxx/8, fxx/16, fxx/32, fxx/64, fxx/128</td>
<td></td>
</tr>
</tbody>
</table>

**Remark**  

fxx: Peripheral clock frequency
## Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

### Documents related to V850E/IA3, V850E/IA4, V850ES/IK1, and V850ES/IE2

<table>
<thead>
<tr>
<th>Document Name</th>
<th>Document No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>V850E1 Architecture User's Manual</td>
<td>U14559E</td>
</tr>
<tr>
<td>V850ES/IK1 Hardware User's Manual</td>
<td>U16910E</td>
</tr>
<tr>
<td>V850ES/IE2 Hardware User's Manual</td>
<td>U17716E</td>
</tr>
<tr>
<td>Inverter Control by V850 Series Vector Control by Hole Sensor</td>
<td>U17338E</td>
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<td>Inverter Control by V850 Series Vector Control by Encoder</td>
<td>U17324E</td>
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<td>Inverter Control by V850 Series 120° Excitation Method Control by Zero-Cross Detection</td>
<td>U17209E</td>
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<tr>
<td>Manual for Using Sample Program Functions DMA Functions (V850E/IA3, V850E/IA4) Application Note</td>
<td>U18235E</td>
</tr>
<tr>
<td>Manual for Using Sample Program Functions Timer Q (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note</td>
<td>This manual</td>
</tr>
<tr>
<td>Manual for Using Sample Program Functions Timer ENC (V850E/IA3, V850E/IA4) Application Note</td>
<td>U18240E</td>
</tr>
<tr>
<td>Manual for Using Sample Program Functions Clock Generator (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note</td>
<td>U18242E</td>
</tr>
</tbody>
</table>
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16-bit timer/event counter Q (TMQn) (n = 0, 1)

Interval timer mode

[Functions] Outputs a PWM waveform with a duty factor of 50% whose half cycle is equal to the interval set by the TQ0CCR0 register.

Outputs a PWM waveform, from the TOQ01 pin, whose half cycle is equal to the interval with a duty factor of 50% upon a match between the count values of the TQ0CCR1 register and the 16-bit counter.

Can be implemented with TMQ0 and TMQ1.

[Function name] timerq_interval

[Argument] None

[Processing content] Performs count operation of an fxx/32 count clock, generates an interrupt by inverting the TOQ00 pin output upon the count subsequent to the count whose value matches the value of the TQ0CCR0 register, and clears the counter. Generates an interrupt by inverting the TOQ01 pin output upon the count subsequent to the count whose value matches the value of the TQ0CCR1 register. The TOQ00 and TOQ01 pins start output at high level.

[Starting method] Starts by calling timerq_interval_st function.

[SFRs used] TQ0CTL0 Selects the count clock.

TQ0CTL1 Selects the timer mode.

TQ0IOC0 • Sets the TOQ00 to TOQ03 register pin outputs.

• Sets the TOQ00 to TOQ03 pin output levels.

TQ0CCR0 Compare register of the 16-bit counter

TQ0CCR1 Compare register of the 16-bit counter

[call function] main main function

[Variable] None

[Interrupts] timerq_TQ0CC0_int

timerq_TQ0CC1_int

[Interrupt sources] INTTQ0CC0

INTTQ0CC1

[File name] timerq_interval.timerq_1.c,
timerq_interval.MAIN.C

[Caution] • The following care must be exercised for setting the registers.

TQnCTL1

Bits 5 and 6: Only TMQ0 is settable. TMQ1 must be set to 0.
The interval time can be calculated by the following formula.

\[
\text{Interval} = (\text{Set value of TQ0CCR0 register} + 1) \times \text{Count clock cycle}
\]

[Function name] timerq_interval_st
[Argument] None
[Processing content] Starting function of timerq_interval
[Starting method] Call this function after calling the timerq_interval function.
[SFR used] TQ0CTL0.TQ0CE Controls TMQ0 operation.
[call function] None
[Variable] None
[File name] timerq_interval/timerq_1.c
[Caution] None

Interrupt functions

[Function name] timerq_TQ0CC0_int
[Overview] Defined by the user.
[Factor] INTTQ0CC0 Match between the count value of the 16-bit counter and TQ0CCR0
[call function] None
[Variable] None
[File name] timerq_interval/timerq_1.c
[Caution] None

[Function name] timerq_TQ0CC1_int
[Overview] Defined by the user.
[Factor] INTTQ0CC1 Match between the count value of the 16-bit counter and TQ0CCR1
[call function] None
[Variable] None
[File name] timerq_interval/timerq_1.c
[Caution] None
16-bit timer/event counter Q (TMQn)

Interval timer mode

- Sets internal count clock to \( f_{IO}/32 \)
- Sets timer mode to interval timer mode
- Sets TOQ03 pin output level to low-level start
- Disables TOQ03 pin output
- Sets TOQ02 pin output level to low-level start
- Disables TOQ02 pin output
- Sets TOQ01 pin output level to high-level start
- Enables TOQ01 pin output
- Sets TOQ00 pin output level to high-level start
- Enables TOQ00 pin output
- Sets compare register

main

EI

Enables interrupt

timerq_inteval_init

TMQ0 timer/event counter (setting)

timerq_interval_start

TMQ0 timer/event counter (start)

TQ0CCMK0\(\sim1\), TQ0CCMK1\(\sim0\), TQ0CCMK2\(\sim0\), TQ0CCMK3\(\sim0\)

sets interrupt mask flag

(TOs interrupt servicing of INTTQ0CC0 and INTTQ0CC1)

TQ0CE\(\sim0\)

Disables TMQ0 count operation

PFC1\(\sim0\) 0x00
PFCE1\(\sim0\) 0x01
PMC1\(\sim0\) 0x04

Sets alternate-function pin

TQ0CTL0\(\sim2\) 0x1, TQ0CTL0\(\sim1\) 0x0, TQ0CTL0\(\sim0\) 0x0

TQ0CTL1\(\sim2\) 0x0, TQ0CTL1\(\sim1\) 0x0, TQ0CTL1\(\sim0\) 0x0

Sets internal count clock to \( f_{IO}/32 \)

TQ0CCR0\(\sim0\) 0xFFFF
TQ0CCR1\(\sim0\) 0xFFFF

Sets compare register

TQ0CCR0\(\sim1\) 0xFFFF
TQ0CCR1\(\sim1\) 0xFFFF

• Sets internal count clock to \( f_{IO}/32 \)
• Sets timer mode to interval timer mode
• Sets TOQ03 pin output level to low-level start
• Disables TOQ03 pin output
• Sets TOQ02 pin output level to low-level start
• Disables TOQ02 pin output
• Sets TOQ01 pin output level to high-level start
• Enables TOQ01 pin output
• Sets TOQ00 pin output level to high-level start
• Enables TOQ00 pin output

• Sets compare register

INTTQ0CC0
(Match between values of 16-bit counter and TQ0CCR0)

INTTQOCC1
(Match between values of 16-bit counter and TQ0CCR1)

reti

TQ0CE\(\sim1\)

Enables TMQ0 count operation
16-bit timer/event counter Q (TMQ0)

External event count mode

[Functions] Counts the valid edge of the external event count input (EVTQ0 pin) and generates an interrupt request signal (INTTQ0CC0) for each count set to the TQ0CCR0 register. (Clears the 16-bit counter simultaneously.)
Generates an interrupt request signal (INTTQ0CCR1) upon a compare match between the count value of the 16-bit counter and the value of the TQ0CCR1 register.
Can be implemented with TMQ0.

[Function name] timerq_event_count

[Argument] None

[Processing content] Counts the valid edge of the external event count input, generates an interrupt upon the count subsequent to the count whose value matches the value of the TQ0CCR0 register, and clears the counter.
Generates an interrupt upon the count subsequent to the count whose value matches the value of the TQ0CCR1 register.

[Starting method] Starts by calling the timerq_event_count_st function.

[SFRs used] TQ0CTL0 Selects the count clock.
TQ0CTL1 Selects the timer mode.
TQ0IOC2 • Sets the valid edge of the external event count input signal (EVTQ0 pin).
• Sets the valid edge of the external trigger input signal (TRGQ0 pin).
TQ0CCR0 Compare register of the 16-bit counter
TQ0CCR1 Compare register of the 16-bit counter

[call function] main main function

[Variable] None

[Interrupts] timerq_TQ0CC0_int
timerq_TQ0CC1_int

[Interrupt sources] INTTQ0CC0
INTTQ0CC1

[File name] timerq_event_count	imerq_2.c,
timerq_event_count	MAIN.C

[Cautions] • The TQ0CCR0 to TQ0CCR3 registers must not be set to 0x0000.
• The following care must be exercised for setting the registers.
TQ0IOC0
Set to 0x00.
### Function Name: timerq_event_count_st

**Argument:** None

**Processing Content:** Starting function of timerq_event_count

**Starting Method:** Call this function after calling the timerq_event_count function.

**SFR Used:** TQ0CTL0.TQ0CE

**Call Function:** None

**Variable:** None

**File Name:** timerq_event_count	imerq_2.c

**Caution:** None

---

### Interrupt Functions

#### Function Name: timerq_TQ0CC0_int

**Overview:** Defined by the user.

**Factor:** INTTQ0CC0

**Call Function:** None

**Variable:** None

**File Name:** timerq_event_count	imerq_2.c

**Caution:** None

---

#### Function Name: timerq_TQ0CC1_int

**Overview:** Defined by the user.

**Factor:** INTTQ0CC1

**Call Function:** None

**Variable:** None

**File Name:** timerq_event_count	imerq_2.c

**Caution:** None
### 16-bit timer/event counter Q (TMQ0)

#### External event count mode

- **Enables interrupt**

- **Disables TMQ0 count operation**

- **Sets alternate-function pin**

- **Sets interrupt mask flag (Enables interrupt servicing of INTTQ0CC0 and INTTQ0CC1)**

- **Sets timer mode to external event count mode**

- **Sets valid edge of external event count input to falling edge**

- **Sets compare register**

- **No setting of internal count clock**

- **(Match between values of 16-bit counter and TQ0CCR0)**

- **(Match between values of 16-bit counter and TQ0CCR1)**

### Code Snippet

```c
EI

timerq_event_count_init

TQ0CE = 0

PFC1 = 0x10
PMC1 = 0x10

TQ0CCMK0 = 0
TQ0CCMK1 = 0
TQ0CCMK2 = 1
TQ0CCMK3 = 1

timerq_event_count

ret

INTTQ0CC0

timerq_TQ0CC0_int

reti

INTTQ0CC1

timerq_TQ0CC1_int

reti

TQ0CE = 1

Enables TMQ0 count operation
```

### Diagram

- **Main**
  - **EI**
    - **Timerq_event_count_init**
      - **TQ0CE = 0**
        - **PFC1 = 0x10**
          - **PMC1 = 0x10**
            - **TQ0CCMK0 = 0**
              - **TQ0CCMK1 = 0**
                - **TQ0CCMK2 = 1**
                  - **TQ0CCMK3 = 1**
                    - **Timerq_event_count**
                      - **ret**
```

- **Timerq_event_count_st**
  - **TQ0CE = 1**
    - **ret**
```

**Additional Notes:**
- **No setting of internal count clock**
- **Sets timer mode to external event count mode**
- **Sets valid edge of external event count input to falling edge**
- **Sets compare register**
16-bit timer/event counter Q (TMQ0)
External trigger pulse output mode

[Functions] Starts count operation of the valid edge of the external event count input (EVTQ0 pin) when the valid edge of the external trigger input (TRGQ0 pin) is detected.
Inverts the TOQ00 pin output by clearing the count value of the 16-bit counter upon a compare match with the TQ0CCR0 register.
Inverts the TOQ01 pin output upon a match between the value set by the TQ0CCR1 register and the count value of the 16-bit counter.
Inverts the TOQ01 pin output after the 16-bit counter is cleared.
Can be implemented with TMQ0.

[Function name] timerq_trigger_pulse
[Argument] None
[Processing content] Starts count operation of the valid edge of the external event count input when the valid edge of the external trigger input is detected, generates an interrupt by inverting the TOQ00 and TOQ01 pin outputs upon the count subsequent to the count whose value matches the value of the TQ0CCR0 register, and clears the counter.
Generates an interrupt by inverting the TOQ01 pin output upon the count subsequent to the count whose value matches the value of the TQ0CCR1 register.
TOQ00 and TOQ01 pins start output at high level.

[Starting method] Starts by calling the timerq_trigger_pulse_st function.

[SFRs used] TQ0CTL0 Selects the count clock.
TQ0CTL1 Selects the timer mode.
TQ0IOC0 • Sets the TOQ00 and TOQ03 pin outputs.
• Sets the TOQ00 and TOQ03 pin output levels.
TQ0IOC2 • Sets the valid edge of the external event count input signal (EVTQ0 pin).
• Sets the valid edge of the external trigger input signal (TRGQ0 pin).
TQ0CCR0 Compare register of the 16-bit counter
TQ0CCR1 Compare register of the 16-bit counter

[call function] main main function
[Variable] None
[Interrupts] timerq_TQ0CC0_int
timerq_TQ0CC1_int
[Interrupt sources] INTTQ0CC0
INTTQ0CC1
The active level width, cycle and duty factor of the PWM waveform output from the TOQ01 pin can be calculated by the following formula.

Active level width = (Set value of TQ0CCR1 register) × Count clock cycle

Cycle = (Set value of TQ0CCR0 register + 1) × Count clock cycle

Duty factor = (Set value of TQ0CCR1 register)/(Set value of TQ0CCR0 register + 1)
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<td>Caution</td>
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</table>
16-bit timer/event counter Q (TMQ0)

External trigger pulse output mode

- No setting of internal count clock
- Enables software trigger control as unused
- Enables external event count input operation
- Sets timer mode to external trigger pulse output mode
- Sets TOQ03 pin output level to low-level start
- Disables TOQ03 pin output
- Sets TOQ02 pin output level to low-level start
- Disables TOQ02 pin output
- Sets TOQ01 pin output level to high-level start
- Enables TOQ01 pin output
- Sets TOQ00 pin output level to high-level start
- Enables TOQ00 pin output
- Sets valid edge of external event count input to falling edge
- Sets valid edge of external trigger input to falling edge
- Sets compare register

EI Enables interrupt

TMQ0 timer/event counter (setting)

Disables TMQ0 count operation

Sets alternate-function pin

Sets interrupt mask flag
(Enables interrupt servicing of INTTQ0CC0 and INTTQ0CC1)

TMQ0 timer/event counter (start)

TMQ0 timer/event counter

Enables TMQ0 count operation

PFC1=0x30
PFCE1=0x01
PMC1=0x71

TQ0CCMK0=0
TQ0CCMK1=0
TQ0CCMK2=1
TQ0CCMK3=1

TQ0CCCR0=40
TQ0CCCR1=10
TQ0CCCR2=0xFFFF
TQ0CCCR3=0xFFFF

INTTQ0CC0
(Match between values of 16-bit counter and TQ0CCR0)

INTTQ0CC1
(Match between values of 16-bit counter and TQ0CCR1)

ret
16-bit timer/event counter Q (TMQ0)
One-shot pulse output mode

[Functions] Starts count operation of the valid edge of the external event count input (EVTQ0 pin) when the valid edge of the external trigger input (TRGQ0 pin) is detected.

Stops count operation of the 16-bit counter by inverting the TOQ00 pin output upon a match between the value set by the TQ0CCR0 register and the count value of the 16-bit counter.

Inverts the TOQ01 pin output upon a match between the value set by the TQ0CCR1 register and the count value of the 16-bit counter.

Can be implemented with TMQ0.

[Function name] timerq_1shot_pulse

[Argument] None

[Processing content] Starts count operation of the valid edge of the external event count input upon valid edge detection of the external trigger input, generates an interrupt by inverting the TOQ00 pin output upon the count subsequent to the count whose value matches the value of the TQ0CCR0 register, clears the counter, and stops count operation.

Generates an interrupt by inverting the TOQ01 pin output upon the count subsequent to the count whose value matches the value of the TQ0CCR1 register.

TOQ00 and TOQ01 pins start at high level.

[Starting method] Starts by calling the timerq_1shot_pulse_st function.

[SFRs used] TQ0CTL0 Selects the count clock.

TQ0CTL1 Selects the timer mode.

TQ0IOC0 • Sets the TOQ00 to TOQ03 pin outputs.

• Sets the TOQ00 to TOQ03 pin output levels.

TQ0IOC2 • Sets the valid edge of the external event count input signal (EVTQ0 pin).

• Sets the valid edge of the external trigger input signal (TRGQ0 pin).

TQ0CCR0 Compare register of the 16-bit counter

TQ0CCR1 Compare register of the 16-bit counter

[call function] main main function

[Variable] None

[Interrupts] timerq_TQ0CC0_int

timerq_TQ0CC1_int

[Interrupt sources] INTTQ0CC0

INTTQ0CC1

[File name] timerq_1shot_pulse\timerq_4.c,
timerq_1shot_pulse\MAIN.C

[Caution] None
The output delay period and the active level width of the one-shot pulse can be calculated from the following formula.

Output delay period = (Set value of TQ0CCR1 register) × Count clock cycle

Active level width = (Set value of TQ0CCR0 register − Set value of TQ0CCR1 register + 1) × Count clock cycle

[Function name] timerq_1shot_pulse_st
[Argument] None
[Processing content] Starting function of timerq_1shot_pulse
[Starting method] Call this function after calling the timerq_1shot_pulse function.
[SFR used] TQ0CTL0.TQ0CE Controls TMQ0 operation.
[call function] None
[Variable] None
[File name] timerq_1shot_pulse\timerq_4.c
[Caution] None
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<tr>
<td>call function</td>
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<tr>
<td>Variable</td>
<td>None</td>
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<td>File name</td>
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<td>INTTQ0CC1 Match between the count value of the 16-bit counter and TQ0CCR1</td>
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<tr>
<td>call function</td>
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<td>Caution</td>
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</table>
16-bit timer/event counter Q (TMQ0)

One-shot pulse output mode

- No setting of internal count clock
- Sets software trigger control as unused
- Enables external event count input operation
- Sets timer mode to one-shot pulse output mode
- Sets TOQ03 pin output level to low-level start
- Disables TOQ03 pin output
- Sets TOQ02 pin output level to low-level start
- Enables TOQ02 pin output
- Sets TOQ01 pin output level to high-level start
- Enables TOQ01 pin output
- Enables TOQ00 pin output
- Enables TOQ00 pin output
- Sets valid edge of external event count input to falling edge
- Sets valid edge of external trigger input to falling edge
- Sets compare register
16-bit timer/event counter Q (TMQ0)

PWM output mode

| [Functions] | Starts operation of the 16-bit counter by setting the TQ0CE bit. Outputs a PWM waveform with a 50% duty factor whose half cycle is equal to the set value of the TQ0CCR0 register + 1, by clearing the 16-bit counter upon a compare match with the TQ0CCR0 register and inverting the TOQ00 pin. Inverts the TOQ01 pin output upon a match between the value set by the TQ0CCR1 register and the count value of the 16-bit counter. Inverts the TOQ01 pin output when the 16-bit counter is cleared. Can be implemented with TMQ0. |
| [Function name] | timerq_pwm_output |
| [Argument] | None |
| [Processing content] | Performs count operation of an fxx/32 count clock, generates an interrupt by inverting the TOQ00 and TOQ01 pin outputs upon the count subsequent to the count whose value matches the value of the TQ0CCR0 register, and clears the counter. Generates an interrupt by inverting the TOQ01 pin output upon the count subsequent to the count whose value matches the value of the TQ0CCR1 register. The TOQ00 and TOQ01 pins start output at high level. |
| [Starting method] | Starts by calling the timerq_pwm_output_st function. |
| [SFRs used] | TQ0CTL0  Selects the count clock. TQ0CTL1  • Selects the timer mode.  • Selects the internal count clock or external event count input. TQ0IOC0  • Sets the TOQ00 to TOQ03 pin outputs.  • Sets the TOQ00 to TOQ03 pin output levels. TQ0IOC2  • Sets the valid edge of the external event counter input signal (EVTQ0 pin). TQ0CCR0  Compare register of the 16-bit counter TQ0CCR1  Compare register of the 16-bit counter |
| [call function] | main  main function |
| [Variable] | None |
| [Interrupts] | timerq_TQ0CC0_int  timerq_TQ0CC1_int |
| [Interrupt sources] | INTTQ0CC0  INTTQ0CC1 |
| [File name] | timerq_pwm_output	imerq_pwm_output	imerq_5.c, MAIN.C |
| [Caution] | • The compare register is written in batch write mode. When changing the value of the compare register during timer operation, change the value of the TQ0CCR1 register at the end. |
The active level width, cycle, and duty factor of the PWM waveform output from the TOQ01 pin can be calculated from the following formula.

Active level width = \( (\text{Set value of TQ0CCR1 register}) \times \text{Count clock cycle} \)

Cycle = \( (\text{Set value of TQ0CCR0 register} + 1) \times \text{Count clock cycle} \)

Duty factor = \( (\text{Set value of TQ0CCR1 register})/(\text{Set value of TQ0CCR0 register} + 1) \)

[Function name] timerq_pwm_output_st

[Argument] None

[Processing content] Starting function of timerq_pwm_output

[Starting method] Call this function after calling the timerq_pwm_output function.

[SFR used] TQ0CTL0.TQ0CE Controls TMQ0 operation.

[call function] None

[Variable] None

[File name] timerq_pwm_output:timerq_5.c

[Caution] None
### Interrupt functions

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</tr>
<tr>
<td>call function</td>
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<tr>
<td>Variable</td>
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</tr>
<tr>
<td>File name</td>
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<tr>
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<tr>
<td>Overview</td>
<td>Defined by the user.</td>
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<tr>
<td>Factor</td>
<td>INTTQ0CC1 Match between the count value of the 16-bit counter and TQ0CCR1</td>
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<tr>
<td>call function</td>
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<td>Variable</td>
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<td>File name</td>
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<tr>
<td>Caution</td>
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</table>
16-bit timer/event counter Q (TMQ0)

PWM output mode

- Enables TMQ0 count operation
- Sets internal count clock to f_{VCO}/32
- Enables interrupt
- Disables external event count input operation
- Sets TMQ0 timer/event counter
- Sets timer mode to PWM output mode
- Sets TOQ03 pin output level to low-level start
- Disables TOQ03 pin output
- Sets TOQ02 pin output level to low-level start
- Disables TOQ02 pin output
- Sets TOQ01 pin output level to high-level start
- Enables TOQ01 pin output
- Sets TOQ00 pin output level to high-level start
- Enables TOQ00 pin output
- Sets valid edge of external event count input as external event count invalidated
- Sets compare register

\[
\begin{align*}
\text{TQ0CTL0.2} & = 1, \text{TQ0CTL0.1} = 0, \text{TQ0CTL0.0} = 0 \\
\text{TQ0CTL1.5} & = 0, \text{TQ0CTL1.2} = 1, \text{TQ0CTL1.1} = 0, \text{TQ0CTL1.0} = 0 \\
\text{TQ0IOC0.7} & = 1, \text{TQ0IOC0.6} = 0, \text{TQ0IOC0.5} = 1, \text{TQ0IOC0.4} = 0, \text{TQ0IOC0.3} = 0, \text{TQ0IOC0.2} = 1, \text{TQ0IOC0.1} = 0, \text{TQ0IOC0.0} = 1 \\
\text{TQ0IOC2.3} & = 0, \text{TQ0IOC2.2} = 0 \\
\end{align*}
\]
16-bit timer/event counter Q (TMQ0) (n = 0, 1)

Free-running timer mode

| [Functions] | Inverts the TOQ00 pin output upon a compare match between the TQ0CCR0 register and the count value of the 16-bit counter (compare function).
|            | Stores the count value of the 16-bit counter when the valid edge of the capture trigger input (TIQ01 pin) is detected (capture function).
|            | The compare function can be implemented with TMQ0 and TMQ1.
|            | The capture function can be implemented with TMQ0.

| [Function name] | timerq_free_running
| [Argument] | None

| [Processing content] | Performs count operation of an fxx/32 count clock, generates an interrupt by inverting the TOQ00 pin output upon the count subsequent to the count whose value matches the value of the TQ0CCR0 register, and clears the counter.
| | Generates an interrupt by capturing the count value to the TQ0CCR1 register when the valid edge from the TIQ01 pin is detected.
| | Generates an INTTQ0OV interrupt when a counter overflow is detected.
| | The TOQ00 pin starts output at high level.

| [Starting method] | Starts by calling the timerq_free_running_st function.

| [SFRs used] | TQ0CTL0 Selects the count clock.
| | TQ0CTL1 • Selects the timer mode.
| | • Selects the internal count clock or external event count input.
| | TQ0IOC0 • Sets the TOQ00 to TOQ03 pin outputs.
| | • Sets the TOQ00 to TOQ03 pin output levels.
| | TQ0IOC1 Sets the valid edge of the capture trigger input signal (TIQ00 to TIQ03 pins)
| | TQ0IOC2 • Sets the valid edge of the external event count input signal (EVTQ0 pin).
| | • Sets the valid edge of the external trigger input signal (TRGQ0 pin).
| | TQ0OPT0 Selects the capture or compare function of the TQ0CCR0 to TQ0CCR3 registers.
| | TQ0CCR0 Compare register of the 16-bit counter
| | TQ0CCR1 Compare register of the 16-bit counter

| [call function] | main main function

| [Variable] | None

| [Interrupts] | timerq_TQ0CC0_int
| | timerq_TQ0CC1_int
| | timerq_TQ0OV_int

| [Interrupt sources] | INTTQ0CC0
| | INTTQ0CC1
| | INTTQ0OV
### Application Note U18239EJ1V0AN

**[File name]**
- timerq_free_running\timerq_6.c
- timerq_free_running\MAIN.C

**[Caution]**
- The following care must be exercised for setting the registers.
  - **TQnCTL1**
    - Bits 5 and 6: Only TMQ0 is valid. TMQ1 must be set to 0.
  - **TQnOPT0**
    - Bits 7 to 4: Only TMQ0 is valid. TMP1 must be set to 0.

---

**[Function name]** timerq_free_running_st

**[Argument]** None

**[Processing content]** Starting function of timerq_free_running

**[Starting method]** Call this function after calling the timerq_free_running function.

**[SFR used]**
- TQ0CTL0.TQ0CE Controls TMQ0 operation.

**[call function]** None

**[Variable]** None

**[File name]** timerq_free_running\timerq_6.c

**[Caution]** None
## Interrupt functions

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<td>Call function</td>
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16-bit timer/event counter Q (TMQn)
Free-running timer mode (1/2)

- Sets internal count clock to fxx/32
- Disables external event count input operation
- Sets timer mode to free-running timer mode
- Sets TOQ03 pin output level to low-level start
- Disables TOQ03 pin output
- Sets TOQ02 pin output level to low-level start
- Disables TOQ02 pin output level
- Sets TOQ01 pin output level to low-level start
- Enables TOQ01 pin output
- Sets valid edge of TIQ03 pin capture trigger input as capture operation invalidated
- Sets valid edge of TIQ03 pin capture trigger input as capture operation invalidated
- Sets valid edge of TIQ01 pin capture trigger input to falling edge
- Sets valid edge of TIQ00 pin capture trigger input to falling edge
- Sets valid edge of external event count input as external event count invalidated
- Sets validate edge of external event count input as external event count invalidated
- Sets compare register
- Sets compare register
- Sets compare register
- Sets compare register
- Sets compare register
- Sets compare register
- Sets compare register
- Sets compare register
- Sets compare register
- Sets compare register
- Sets compare register
- Sets compare register
16-bit timer/event counter Q (TMQn)
Free-running timer mode (2/2)

INTTQ0CC0
(Match between values of 16-bit counter and TQ0CCR0)

INTTQ0CC1
(Falling edge detection of TIQ01pin)

INTTQ0OV
(Overflow occurrence of 16-bit counter)
16-bit timer/event counter Q (TMQ0)

Pulse width measurement mode

[Functions] Clears the 16-bit counter by storing the count value to the TQ0CCR0 register when the valid edge of the capture trigger input (TIQ00 pin) is detected.
Measures the valid edge interval of the TIQ00 pin by generating an interrupt when the valid edged of the TIQ00 pin input is detected and reading the TQ0CCR0 register value.
Can be implemented with TMQ0.

[Function name] timerq_pulse_measure

[Argument] None

[Processing content] Performs count operation of an fxx/32 count clock, generates an interrupt by storing the count value of the 16-bit counter to the TQ0CCR0 register when the valid edge of the TIQ00 pin input is detected, and clears the counter.
Generates an INTTQ0OV interrupt when a counter overflow is detected.

[Starting method] Starts by calling the timerq_pulse_measure_st function.

[SFRs used] TQ0CTL0 Selects the count clock.
TQ0CTL1 • Selects the timer mode.
  • Selects the internal count clock or external event count input.
TQ0IOC1 Sets the valid edge of the capture trigger input signal (TIQ00 to TIQ03 pins).
TQ0IOC2 • Sets the valid edge of the external event count input signal (EVTQ0 pin).
  • Sets the valid edge of the external trigger input signal (TRGQ0 pin).
TQ0OPT0 Selects the capture or compare function of the TQ0CCR0 to TQ0CCR3 registers.
TQ0CCR0 Compare register of the 16-bit counter

[call function] main main function

[Variable] None

[Interrupts] timerq_TQ0CC0_int
timerq_TQ0OV_int

[Interrupt sources] INTTQ0CC0
INTTQ0OV

[File name] timerq_pulse_measure\timerq_7.c,
timerq_pulse_measure\MAIN.C

[Cautions] • If a slow clock is selected as the count clock and a capture trigger is input immediately after the TQ0CTL0.TQ0CE bit has been set, 0xFFFF may be captured instead of 0x0000 to the TQ0CCR0 register.
• The following care must be exercised for setting the registers.
  TQ0IOC0
  Set to 0x00.
The pulse width can be calculated by the following formula.

\[
\text{Pulse width} = (\text{Value of TQ0CCR0 register + 1}) \times \text{Count clock cycle}
\]

The pulse width if an overflow of the 16-bit counter is detected can be calculated by the following formula.

\[
\text{Pulse width} = (\text{Value of TQ0CCR0 register + 0x10001}) \times \text{Count clock cycle}
\]

---

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<td>Starting function of timerq_pulse_measure</td>
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<td>[Starting method]</td>
<td>Call this function after calling the timerq_pulse_measure function.</td>
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<tr>
<td>[SFR used]</td>
<td>TQ0CTL0.TQ0CE Controls TMQ0 operation.</td>
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<tr>
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<tr>
<td>[File name]</td>
<td>timerq_pulse_measure\timerq_7.c</td>
</tr>
<tr>
<td>[Caution]</td>
<td>None</td>
</tr>
</tbody>
</table>
## Interrupt functions

<table>
<thead>
<tr>
<th>Function name</th>
<th>timerq_TQ0CC0_int</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overview</td>
<td>Defined by the user.</td>
</tr>
<tr>
<td>Factor</td>
<td>INTTQ0CC0 Match between the count value of the 16-bit counter and TQ0CCR0</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
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<table>
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<tr>
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<th>timerq_TQ0OV_int</th>
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<tr>
<td>Overview</td>
<td>Defined by the user.</td>
</tr>
<tr>
<td>Factor</td>
<td>INTTQ0OV Overflow occurrence of 16-bit counter</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
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</table>
16-bit timer/event counter Q (TMQ0)
Pulse width measurement mode

- Enables interrupt
- TMQ0 timer/event counter (setting)
- TMQ0 timer/event counter (start)
- Clears overflow flag of 16-bit counter
- Disables TMQ0 count operation
- Sets input pin
- Sets interrupt mask flag (Enables interrupt servicing of INTTQ0CC0 and INTTQ0OV)
- TMQ0 timer/event counter
- Enables TMQ0 count operation
- TQ0CE = 1
- Sets internal count clock to fXX/32
- Disables external event count input operation
- Sets timer mode to pulse width measurement mode
- Sets valid edge of TIQ03 pin capture trigger input as capture operation invalidated
- Sets valid edge of TIQ02 pin capture trigger input as capture operation invalidated
- Sets valid edge of TIQ01 pin capture trigger input as capture operation invalidated
- Sets valid edge of TIQ00 pin capture trigger input to falling edge
- Sets valid edge of external event count input as external event count invalidated
- No settings of capture/compare registers

```
EI

timerq_pulse_measure_init

TQ0CE = 0

PFC1 = 0x08
PM1 = 0x08
PSC1 = 0x08

TQ0CCMK0 = 0
TQ0CCMK1 = 1
TQ0CCMK2 = 1
TQ0CCMK3 = 1
TQ0OVMK = 0

timerq_pulse_measure

ret

TQ0OVF = 1?

Yes

TQ0OVF = 0

No

timerq_pulse_measure_init

TQ0CE = 0

INTTQ0CC0 (Falling edge detection of TIQ00 pin)

timerq_TQ0CC0_int

reti

INTTQ0OV (Overflow occurrence of 16-bit counter)

timerq_TQ0OV_int

ret

```
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