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Manual for Using Sample Program Functions Timer P (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2)

This manual explains the sample program functions of the 16-bit timer/event counter P (TMP) for the V850E/IA4 microcontroller.

The explanations are based on usage with the V850E/IA4 microcontroller. Refer to this manual when using the V850E/IA3, V850ES/IK1, and V850ES/IE2 microcontrollers.

Caution

This sample program is provided for reference purposes only and operations are therefore not subject to guarantee by NEC Electronics Corporation. When using this sample program, customers are kindly advised to sufficiently evaluate this product based on their system before usage.

1 VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

(2) HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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INTRODUCTION

- Cautions 1. Download the program used in this manual from the NEC Electronics Website (<u>http://www.necel.com/</u>).
 - 2. When using this sample program, reference the following startup file and link directive file and adjust them if as necessary.
 - Startup file: IA4_start.s
 - Link directive file: IA4_link.dir

Conventions

The function lists are structured as follows.

Hardware name (symbol)

[Function(s)]	Function description		
[Function name]	Name of sample function		
[Argument(s)]	Type and overview of argument(s)		
[Processing content]	Processing content of sample function		
[Starting method]	Conditions for calling a function		
[SFR(s) used]	Register name and setting content		
[call function(s)]	Name and function of call function(s)		
[Variable(s)]	Type, name, and overview of variable(s) used in sample function		
[Interrupt(s)]	Name of function		
[Interrupt source(s)]	Name		
[File name]	Name of corresponding sample program file		
[Caution(s)]	Caution(s) upon function usage		

Interrupt function(s)

[Function name]	Name of interrupt function
[Overview]	Processing content
[Factor(s)]	Name of interrupt and conditions for occurrence
[call function(s)]	None
[Variable(s)]	Name of variable, function
[File name]	Name of corresponding sample program file
[Caution(s)]	None

Product Differences

The differences between the V850E/IA4 and the V850E/IA3, V850ES/IK1, and V850ES/IE2 related to the 16-bit timer/event counter P (TMP) are shown below.

Item	V850E/IA4	V850E/IA3	V850ES/IK1	V850ES/IE2
TOP31 pin	Provided	Provided	Provided	
Count clock	fxx/2, fxx/4, fxx/8,	fxx/2, fxx/4, fxx/8,	fxx, fxx/2, fxx/4, fxx/8, fx	xx/16, fxx/32, fxx/64,
	fxx/16, fxx/32, fxx/64,	fxx/16, fxx/32, fxx/64,	fxx/128	
	fxx/128, fxx/256	fxx/128, fxx/256		

Remark fxx: Peripheral clock frequency

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850E/IA3, V850E/IA4, V850ES/IK1, and V850ES/IE2

V/05051 Architecture Llease Manuel	
V850E1 Architecture User's Manual	U14559E
V850E/IA3, V850E/IA4 Hardware User's Manual	U16543E
V850ES Architecture User's Manual	U15943E
V850ES/IK1 Hardware User's Manual	U16910E
V850ES/IE2 Hardware User's Manual	U17716E
Inverter Control by V850 Series Vector Control by Hole Sensor Application Note	U17338E
Inverter Control by V850 Series Vector Control by Encoder Application Note	U17324E
Inverter Control by V850 Series 120° Excitation Method Control by Zero-Cross Detection	U17209E
Application Note	
Manual for Using Sample Program Functions Serial Communication (UARTA)	U18233E
(V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	
Manual for Using Sample Program Functions Serial Communication (CSIB) (V850E/IA3,	U18234E
V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	
Manual for Using Sample Program Functions DMA Functions (V850E/IA3, V850E/IA4)	U18235E
Application Note	
Manual for Using Sample Program Functions Timer M (V850E/IA3, V850E/IA4,	U18236E
V850ES/IK1, V850ES/IE2) Application Note	
Manual for Using Sample Program Functions Watchdog Timer (V850E/IA3, V850E/IA4,	U18237E
V850ES/IK1, V850ES/IE2) Application Note	
Manual for Using Sample Program Functions Timer P (V850E/IA3, V850E/IA4,	This manual
V850ES/IK1, V850ES/IE2) Application Note	
Manual for Using Sample Program Functions Timer Q (V850E/IA3, V850E/IA4,	U18239E
V850ES/IK1, V850ES/IE2) Application Note	
Manual for Using Sample Program Functions Timer ENC (V850E/IA3, V850E/IA4)	U18240E
Manual for Using Sample Program Functions Port Functions (V850E/IA3, V850E/IA4,	U18241E
V850ES/IK1, V850ES/IE2) Application Note	
Manual for Using Sample Program Functions Clock Generator (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	U18242E
Manual for Using Sample Program Functions Standby Functions (V850E/IA3, V850E/IA4,	U18243E
V850ES/IK1, V850ES/IE2) Application Note	U IUZHUL
Manual for Using Sample Program Functions Interrupt Functions (V850E/IA3, V850E/IA4,	U18244E
V850ES/IK1, V850ES/IE2) Application Note	
Manual for Using Sample Program Functions A/D Converters 0 and 1 (V850E/IA3,	U18245E
V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	
Manual for Using Sample Program Functions A/D Converter 2 (V850E/IA3, V850E/IA4)	U18246E
Application Note	

CONTENTS

16-bit timer/event counter P (TMPn) (n = 0 to 3)	
Interval timer mode	
16-bit timer/event counter P (TMPk) ($k = 0, 2$)	
External event counter mode	
16-bit timer/event counter P (TMPm) (m = 0, 2, 3)	
External trigger pulse output mode	
16-bit timer/event counter P (TMPm) (m = 0, 2, 3)	
One-shot pulse output mode	
16-bit timer/event counter P (TMPm) (m = 0, 2, 3)	
PWM output mode	
16-bit timer/event counter P (TMPn) (n = 0 to 3)	
Free-running timer mode	
16-bit timer/event counter P (TMPk) ($k = 0, 2$)	
Pulse width measurement mode	

16-bit timer/event counter P (TMPn) (n = 0 to 3) Interval timer mode

[Functions]	Outputs a PWM waveform with a duty factor of 50% from the TOP00 pin at an interval set by the TP0CCR0 register. Inverts the TOP01 pin output when the value set by the TP0CCR1 register and the count value of the 16-bit counter match. Can be implemented with TMP0 to TMP3.	
[Function name]	timerp_interval	
[Argument]	None	
[Processing content]	TOP00 pin outpo value of the TP00 Generates an int the count whose	operation of an fxx/32 count clock, generates an interrupt by inverting the ut upon the count subsequent to the count whose value matches the CCR0 register, and clears the counter. terrupt by inverting the TOP01 pin output upon the count subsequent to value matches the value of the TP0CCR1 register. TOP01 pins start output at high level.
[Starting method]	Starts by calling t	the timerp_interval_st function.
[SFRs used]	TP0CTL0 TP0CTL1 TP0IOC0 TP0CCR0 TP0CCR1	 Selects the count clock. Selects the timer mode. Sets the TOP00 and TOP01 pin outputs. Sets the TOP00 and TOP01 pin output levels. Compare register of the 16-bit counter Compare register of the 16-bit counter
[call function]	main main fun	ction
[Variable]	None	
[Interrupts]	timerp_TP0CC0_ timerp_TP0CC1_	
[Interrupt sources]	INTTP0CC0 INTTP0CC1	
[File name]	timerp_interval\ti timerp_interval\N	

(1/2)

[Cautions]	The following care must be exercised for setting the registers. TPnCTL1(n = 0 to 3)
	Bit 7: Only TMP0 and TMP1 are settable. TMP2 and TMP3 must be set to 0.
	Bit 6: Only TMP0, TMP2, and TMP3 are settable. TMP1 must be set to 0.
	Bit 5: Only TMP0 and TMP2 are settable. TMP1 and TMP3 must be set to 0.
	TPmIOC0 (m = 0, 2, 3)
	Bits 1 and 0: Only TMP0 is valid. TMP2 and TMP3 must be set to 0.

The interval time can be calculated by the following formula.

Interval = (Set value of TP0CCR0 register + 1) \times Count clock cycle

[Function name]	timerp_interval_st	
[Argument]	None	
[Processing content]	Starting function of timerp_int	rerval
[Starting method]	Call this function after calling	the timerp_interval function.
[SFR used]	TP0CTL0.TP0CE	Controls TMP0 operation.
[call function]	None	
[Variable]	None	
[File name]	timerp_interval\timerp_1.c	
[Caution]	None	

(2/2)

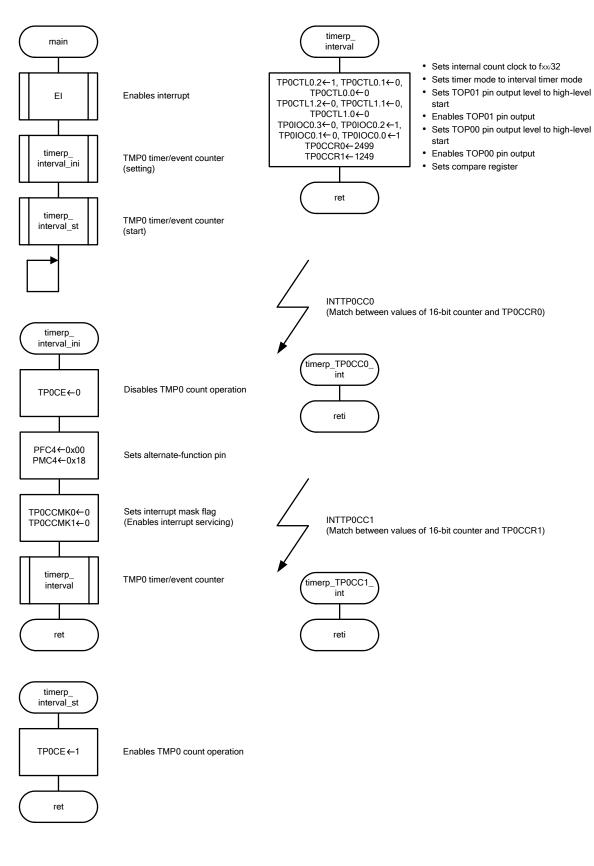
Interrupt functions

[Function name]	timerp_TP0CC0_int		
[Overview]	Defined by the user.		
[Factor]	INTTP0CC0	Match between the count value of the 16-bit counter and TP0CCR0	
[call function]	None		
[Variable]	None		
[File name]	timerp_interval\t	imerp_1.c	
[Caution]	None		

[Function name]	timerp_TP0CC1_int		
[Overview]	Defined by the user.		
[Factor]	INTTP0CC1	Match between the count value of the 16-bit counter and TP0CCR1	
[call function]	None		
[Variable]	None		
[File name]	timerp_interval\ti	imerp_1.c	
[Caution]	None		

16-bit timer/event counter P (TMPn)

Interval timer mode



16-bit timer/event counter P (TMPk) (k = 0, 2) External event counter mode

[Functions]	Counts the valid edge of the external event count input (TIP00 pin) and generates an interrupt request signal (INTTP0CC0) for each count set to the TP0CCR0 register. (Clears the 16-bit counter simultaneously.) Generates an interrupt request signal (INTTP0CCR1) upon a compare match between the count value of the 16-bit counter and the value of the TP0CCR1 register. Can be implemented with TMP0 and TMP2.		
[Function name]	timerp_event_count		
[Argument]	None		
[Processing content]	Counts the valid edge of the external event count input, generates an interrupt upon the count subsequent to the count whose value matches the value of the TP0CCR0 register, and clears the counter. Generates an interrupt upon the count subsequent to the count whose value matches the value of the TP0CCR1 register.		
[Starting method]	Starts by calling the timerp_event_count_st function.		
[SFRs used]	TPOCTL0Selects the count clock.TPOCTL1Selects the timer mode.TPOIOC2• Sets the valid edge of the external event count input signal (TIP00 pin). • Sets the valid edge of the external trigger input signal (TIP00 pin).TPOCCR0Compare register of the 16-bit counterTPOCCR1Compare register of the 16-bit counter		
[call function]	main main function		
[Variable]	None		
[Interrupts]	timerp_TP0CC0_int timerp_TP0CC1_int		
[Interrupt sources]	INTTP0CC0 INTTP0CC1		
[File name]	timerp_event_count\timerp_2.c, timerp_event_count\MAIN.C		
[Cautions]	 The TP0CCR0 and TP0CCR1 registers must not be set to 0x0000. The following care must be exercised for setting the registers. TPkCTL1 Bit 7: Only TMP0 settable. TMP2 must be set to 0. TPkIOC0 Set to 0x00. 		

[Function name]	timerp_event_count_st
[Argument]	None
[Processing content]	Starting function of timerp_event_count
[Starting method]	Call this function after calling the timerp_event_count function.
[SFR used]	TP0CTL0.TP0CE Controls TMP0 operation.
[call function]	None
[Variable]	None
[File name]	timerp_event_count\timerp_2.c
[Caution]	None

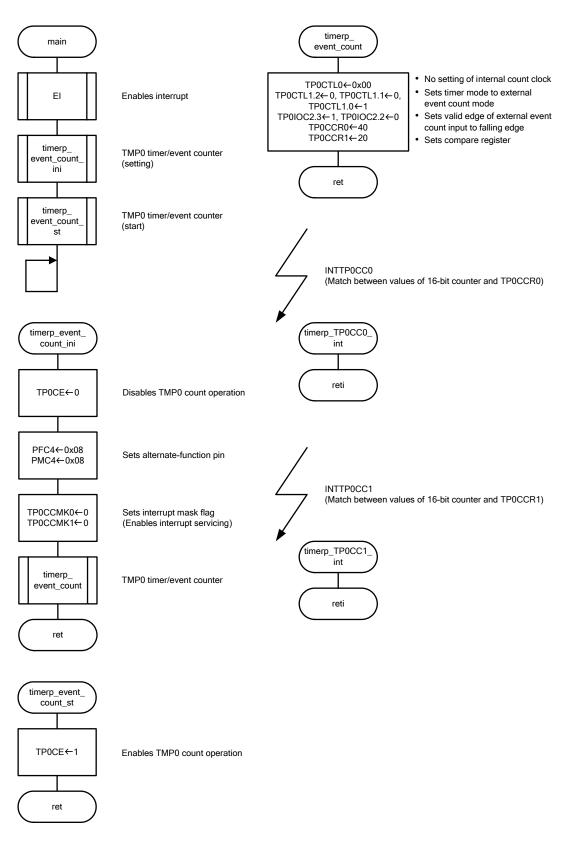
Interrupt functions

[Function name]	timerp_TP0CC0_i	nt
[Overview]	Defined by the use	er.
[Factor]	INTTP0CC0	Match between the count value of the 16-bit counter and TP0CCR0
[call function]	None	
[Variable]	None	
[File name]	timerp_event_cou	nt\timerp_2.c
[Caution]	None	

[Function name]	timerp_TP0CC1_ir	ıt
[Overview]	Defined by the use	r.
[Factor]	INTTP0CC1	Match between the count value of the 16-bit counter and TP0CCR1
[call function]	None	
[Variable]	None	
[File name]	timerp_event_cour	nt\timerp_2.c
[Caution]	None	

16-bit timer/event counter P (TMPk)

External event counter mode



16-bit timer/event counter P (TMPm) (m = 0, 2, 3) External trigger pulse output mode

	(1/2
[Functions]	Starts operation of the 16-bit counter when the valid edge of the external trigger input (TIP00) is detected. Clears the 16-bit counter upon a compare match with the TP0CCR0 register. Inverts the TOP01 pin output upon a match between the value set by the TP0CCR1 register and the count value of the 16-bit counter.
	Inverts the TOP01 pin output when the 16-bit counter is cleared. Can be implemented with TMP0, TMP2, and TMP3 (software trigger only for TMP3).
[Function name]	timerp_trigger_pulse
[Argument] [Processing content]	None Starts count operation of an fxx/32 count clock when the valid edge of the external trigger input is detected, generates an interrupt upon the count subsequent to the count whose value matches the value of the TP0CCR0 register, and clears the counter. Generates an interrupt by inverting the TOP01 pin output upon the count subsequent to the count whose value matches the value of the TP0CCR1 register. TOP01 pin starts output at high level.
[Starting method]	Starts by calling the timerp_trigger_pulse_st function.
[SFRs used]	 TPOCTL0 Selects the count clock. TPOCTL1 Selects the timer mode. TPOIOC0 • Sets the TOP00 and TOP01 pin outputs. • Sets the TOP00 and TOP01 pin output levels. TPOIOC2 • Sets the valid edge of the external event count input signal (TIP00 pin). • Sets the valid edge of the external trigger input signal (TIP00 pin). TPOCCR0 Compare register of the 16-bit counter TPOCCR1 Compare register of the 16-bit counter
[call function]	main main function
[Variable]	None
[Interrupts]	timerp_TP0CC0_int timerp_TP0CC1_int
[Interrupt sources]	INTTPOCC0 INTTPOCC1
[File name]	timerp_trigger_pulse\timerp_3.c, timerp_trigger_pulse\MAIN.C

 [Cautions]
 The compare register is written in batch write mode. When changing the value of the compare register during timer operation, change the value of the TP0CCR1 register at the end.
 The following care must be exercised for setting the registers. TPmCTL1 Bit 7: Only TMP0 is settable. TMP2 and TMP3 must be set to 0. Bit 5: Only TMP0 and TMP2 are settable. TMP3 must be set to 0 TPmIOC0 Bits 1 and 0: Only TMP0 is valid. TMP2 and TMP3 must be set to 0.

(2/2)

The active level width, cycle and duty factor of the PWM waveform can be calculated by the following formula.

```
Active level width = (Set value of TP0CCR1 register) \times Count clock cycle
```

```
Cycle = (Set value of TP0CCR0 register + 1) \times Count clock cycle
```

```
Duty factor = (Set value of TP0CCR1 register)/(Set value of TP0CCR0 register + 1)
```

[Function name]	timerp_trigger_pulse_st
[Argument]	None
[Processing content]	Starting function of timerp_trigger_pulse
[Starting method]	Call this function after calling the timerp_trigger_pulse function.
[SFR used]	TP0CTL0.TP0CE Controls TMP0 operation.
[call function]	None
[Variable]	None
[File name]	timerp_trigger_pulse\timerp_3.c
[Caution]	None

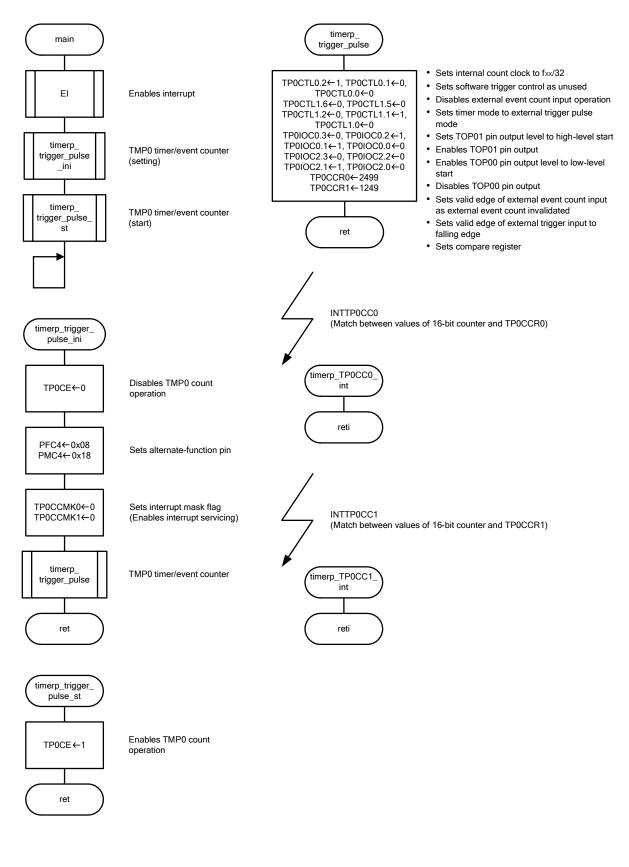
Interrupt functions

[Function name]	timerp_TP0CC0_	_int
[Overview]	Defined by the us	ser.
[Factor]	INTTP0CC0	Match between the count value of the 16-bit counter and TP0CCR0
[call function]	None	
[Variable]	None	
[File name]	timerp_trigger_p	ulse\timerp_3.c
[Caution]	None	

[Function name]	timerp_TP0CC1	_int
[Overview]	Defined by the u	ser.
[Factor]	INTTP0CC1	Match between the count value of the 16-bit counter and TP0CCR1
[call function]	None	
[Variable]	None	
[File name]	timerp_trigger_p	ulse\timerp_3.c
[Caution]	None	

16-bit timer/event counter P (TMPm)

External trigger pulse output mode



16-bit timer/event counter P (TMPm) (m = 0, 2, 3) One-shot pulse output mode

[Functions]	Starts operation of the 16-bit counter when the valid edge of the external trigger input
	(TIP00 pin) is detected. Stops the count when the 16-bit counter is cleared upon a compare match with the
	TP0CCR0 register.
	Inverts the TOP01 pin output upon a match between the value set by the TP0CCR1 register and the count value of the 16-bit counter.
	Inverts the TOP01 pin output when the 16-bit counter is cleared.
	Can be implemented with TMP0, TMP2, and TMP3 (software trigger only for TMP3).
[Function name]	timerp_1shot_pulse
[Argument]	None
[Processing content]	Starts count operation of an fxx/32 count clock upon valid edge detection of the external
	trigger input, generates an interrupt by inverting the TOP01 pin output upon the count
	subsequent to the count whose value matches the value of the TP0CCR0 register, clears
	the counter, and stops count operation.
	Generates an interrupt by inverting the TOP01 pin output upon the count subsequent to the count whose value matches the value of the TP0CCR1 register.
	TOP01 pin starts output at high level.
[Starting method]	Starts by calling the timerp_1shot_pulse_st function.
[SFRs used]	TP0CTL0 Selects the count clock.
	TP0CTL1 Selects the timer mode.
	TP0IOC0 • Sets the TOP00 and TOP01 pin outputs.
	Sets the TOP00 and TOP01 pin output levels.
	TP0IOC2 • Sets the valid edge of the external event count input signal (TIP00 pin).
	 Sets the valid edge of the external trigger input signal (TIP00 pin). TP0CCR0 Compare register of the 16-bit counter
	TPOCCR0 Compare register of the 16-bit counter
[call function]	main main function
[Variable]	None
[Interrupts]	timerp_TP0CC0_int
	timerp_TP0CC1_int
[Interrupt sources]	INTTP0CC0
	INTTP0CC1
[File name]	timerp_1shot_pulse\timerp_4.c,
	timerp_1shot_pulse\MAIN.C

(1/2)

[Caution]	 The following care must be exercised for setting the registers.
	TPmCTL1
	Bit 7: Only TMP0 is settable. TMP2 and TMP3 must be set to 0.
	Bit 5: Only TMP0 and TMP2 are settable. TMP3 must be set to 0
	TPmIOC0
	Bits 1 and 0: Only TMP0 is valid. TMP2 and TMP3 must be set to 0.

The output delay period and the active level width of the one-shot pulse can be calculated from the following formula.

Output delay period = (Set value of TP0CCR1 register) × Count clock cycle Active level width = (Set value of TP0CCR0 register – Set value of TP0CCR1 register + 1) × Count clock cycle

[Function name]	timerp_1shot_pulse_st
[Argument]	None
[Processing content]	Starting function of timerp_1shot_pulse
[Starting method]	Call this function after calling the timerp_1shot_pulse function.
[SFR used]	TP0CTL0.TP0CE Controls TMP0 operation.
[call function]	None
[Variable]	None
[File name]	timerp_1shot_pulse\timerp_4.c
[Cautions]	None

(2/2)

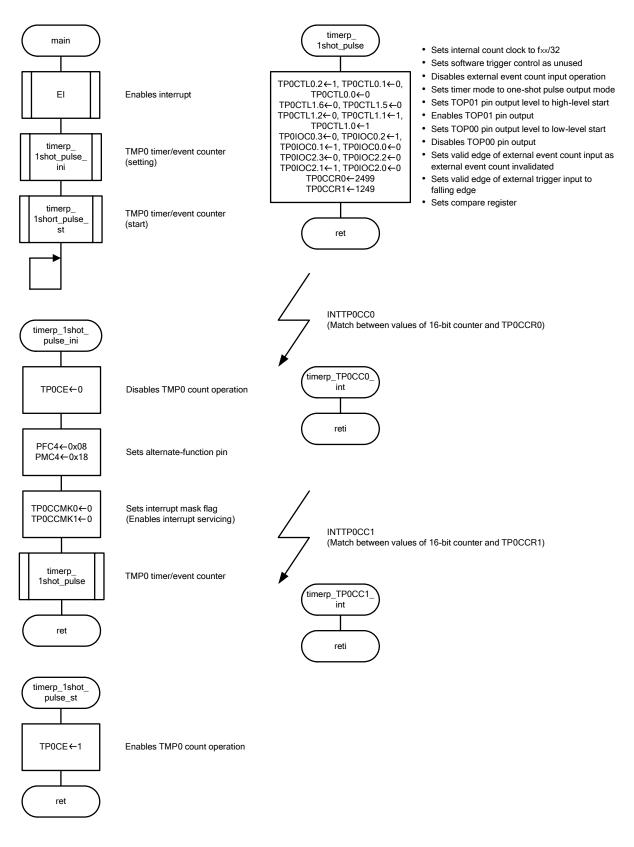
Interrupt functions

[Function name]	timerp_TP0CC0	_int
[Overview]	Defined by the u	ser.
[Factor]	INTTP0CC0	Match between the count value of the 16-bit counter and TP0CCR0
[call function]	None	
[Variable]	None	
[File name]	timerp_1shot_pu	ulse\timerp_4.c
[Caution]	None	

[Function name]	timerp_TP0CC1	_int
[Overview]	Defined by the u	ser.
[Factor]	INTTP0CC1	Match between the count value of the 16-bit counter and TP0CCR1
[call function]	None	
[Variable]	None	
[File name]	timerp_1shot_pu	ulse\timerp_4.c
[Caution]	None	

16-bit timer/event counter P (TMPm)

One-shot pulse output mode



16-bit timer/event counter P (TMPm) (m = 0, 2, 3) PWM output mode

		(1		
[Functions]	Starts operation of the 16-bit counter by setting the TP0CE bit.			
	Outputs a PWM waveform with a 50% duty factor whose half cycle is equal to the set			
	value of the TP0CCR0 register + 1, by clearing the 16-bit counter upon a compare match			
	with the TP0CCR0 register and inverting the TOP00 pin.			
	Inverts the TOP01 pin output upon a match between the value set by the TP0C	CR1		
	register and the count value of the 16-bit counter.			
	Inverts the TOP01 pin output when the 16-bit counter is cleared.			
	Can be implemented with TMP0, TMP2, and TMP3.			
[Function name]	timerp_pwm_output			
[Argument]	None			
[Processing content]	Performs count operation of an fxx/32 count clock, generates an interrupt by inverting	; the		
	TOP00 and TOP01 pin outputs upon the count subsequent to the count whose v	alue		
	matches the value of the TP0CCR0 register, and clears the counter.			
	Generates an interrupt by inverting the TOP01 pin output upon the count subsequent to			
	the count whose value matches the value of the TP0CCR1 register.			
	The TOP00 and TOP01 pins start output at high level.			
[Starting method]	Starts by calling the timerp_pwm_output_st function.			
[SFRs used]	TP0CTL0 Selects the count clock.			
	TP0CTL1 Selects the timer mode.			
	• Sets the TOP00 and TOP01 pin outputs.			
	 Sets the TOP00 and TOP01 pin output levels. 			
	TP0IOC2 • Sets the valid edge of the external event counter input signal (TIP00 p	in).		
	 Sets the valid edge of the external trigger input signal (TIP00 pin). 			
	TP0CCR0 Compare register of the 16-bit counter			
	TP0CCR1 Compare register of the 16-bit counter			
[call function]	main main function			
[Variable]	None			
[Interrupts]	timerp_TP0CC0_int			
	timerp_TP0CC1_int			
[Interrupt sources]	INTTP0CC0			
	INTTP0CC1			
[File name]	timerp_pwm_output\timerp_5.c,			
	timerp_pwm_output\MAIN.C			

[Cautions]	The compare register is written in batch write mode.
	When changing the value of the compare register during timer operation, change the
	value of the TP0CCR1 register at the end.
	 The following care must be exercised for setting the registers.
	TPmCTL1
	Bit 7: Only TMP0 is settable. TMP2 and TMP3 must be set to 0.
	Bit 5: Only TMP0 and TMP2 are settable. TMP3 must be set to 0
	TPmIOC0
	Bits 1 and 0: Only TMP0 is valid. TMP2 and TMP3 must be set to 0.

<u>(2/</u>2)

The active level width, cycle, and duty factor of the PWM waveform output from the TOP01 pin can be calculated from the following formula.

Active level width = (Set value of TP0CCR1 register) \times Count clock cycle

Cycle = (Set value of TP0CCR0 register + 1) \times Count clock cycle

Duty factor = (Set value of TP0CCR1 register)/(Set value of TP0CCR0 register + 1)

[Function name]	timerp_pwm_output_st		
[Argument]	None		
[Processing content]	Starting function of timerp_	pwm_output	
[Starting method]	Call this function after calling	g the timerp_ pwm_output function.	
[SFR used]	TP0CTL0.TP0CE	Controls TMP0 operation.	
[call function]	None		
[Variable]	None		
[File name]	timerp_pwm_output\timerp_	_5.c	
[Caution]	None		

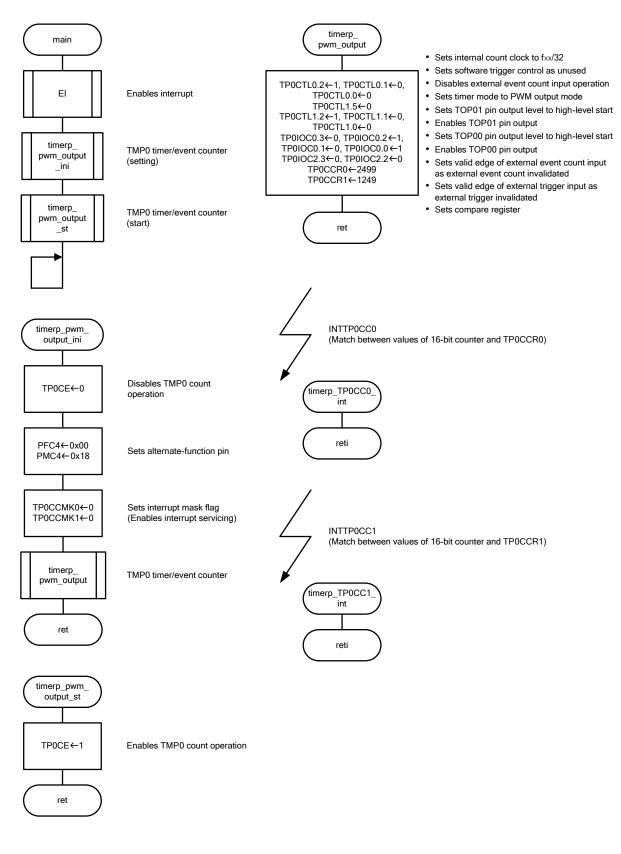
Interrupt functions

[Function name]	timerp_TP0CC0_int	
[Overview]	Defined by the user.	
[Factor]	INTTP0CC0 Match between the count value of the 16-bit counter and TP0CCR0	
[call function]	None	
[Variable]	None	
[File name]	timerp_pwm_output\timerp_5.c	
[Caution]	None	

[Function name]	timerp_TP0CC1_int	
[Overview]	Defined by the user.	
[Factor]	INTTP0CC1 Match between the count value of the 16-bit counter and TP0CCR1	
[call function]	None	
[Variable]	None	
[File name]	timerp_pwm_output\timerp_5.c	
[Caution]	None	

16-bit timer/event counter P (TMPm)

PWM output mode



16-bit timer/event counter P (TMPn) (n = 0 to 3) Free-running timer mode

e-running timer mode

i		
[Functions]	Inverts the TOP00 pin output upon a compare match between the TP0CCR0 register and the count value of the 16-bit counter (compare function). Stores the count value of the 16-bit counter when the valid edge of the capture trigger input (TIP01 pin) is detected (capture function). The compare function can be implemented with TMP0 to TMP3. The capture function can be implemented with TMP0 and TMP2.	
[Function name]	timerp_free_running	
[Argument]	None	
[Processing content]	Performs count operation of an fxx/32 count clock, generates an interrupt by inverting the TOP00 pin output upon the count subsequent to the count whose value matches the value of the TP0CCR0 register, and clears the counter. Generates an interrupt by capturing the count value to the TP0CCR1 register when the valid edge from the TIP01 pin is detected. Generates an INTTP0OV interrupt when a counter overflow is detected. The TOP00 pin starts output at high level.	
[Starting method]	Starts by calling the timerp_free_running_st function.	
[SFRs used]	 TPOCTL0 Selects the count clock. TPOCTL1 Selects the timer mode. TPOIOC0 • Sets the TOP00 and TOP01 pin outputs. • Sets the TOP00 and TOP01 pin output levels. TPOIOC1 Sets the valid edge of the capture trigger input signal (TIP00 and TIP01 pins) TPOIOC2 • Sets the valid edge of the external event count input signal (TIP00 pin). • Sets the valid edge of the external trigger input signal (TIP00 pin). TPOOPT0 Selects the capture/compare functions of the TP0CCR0 and TP0CCR1 registers. TP0CCR0 Compare register of the 16-bit counter TP0CCR1 Compare register of the 16-bit counter 	
[call function]	main main function	
[Variable]	None	
[Interrupts]	timerp_TP0CC0_int timerp_TP0CC1_int timerp_TP0OV_int	
[Interrupt sources]	INTTPOCCO INTTPOCC1 INTTPOOV	

(1/2)

[File name]	timerp_free_running\timerp_6.c,
	timerp_free_running\MAIN.C
[Caution]	The following care must be exercised for setting the registers.
	TPnCTL1
	Bit 7: Only TMP0 and TMP1 are settable. TMP2 and TMP3 must be set to 0.
	Bit 6: Only TMP0, TMP2, and TMP3 are settable. TMP1 must be set to 0.
	Bit 5: Only TMP0 and TMP2 are settable. TMP1 and TMP3 must be set to 0.
	TPmIOC0 (m = 0, 2, 3)
	Bits 1 and 0: Only TMP0 is valid. TMP2 and TMP3 must be set to 0.
	TPnOPT0
	Bits 5 and 4: Only TMP0 and TMP2 are valid. TMP1 and TMP3 must be set to 0.

[Function name]	timerp_free_running_st
[Argument]	None
[Processing content]	Starting function of timerp_free_running
[Starting method]	Call this function after calling the timerp_free_running function.
[SFR used]	TP0CTL0.TP0CE Controls TMP0 operation.
[call function]	None
[Variable]	None
[File name]	timerp_free_running\timerp_6.c
[Caution]	None

(2/2)

Interrupt functions

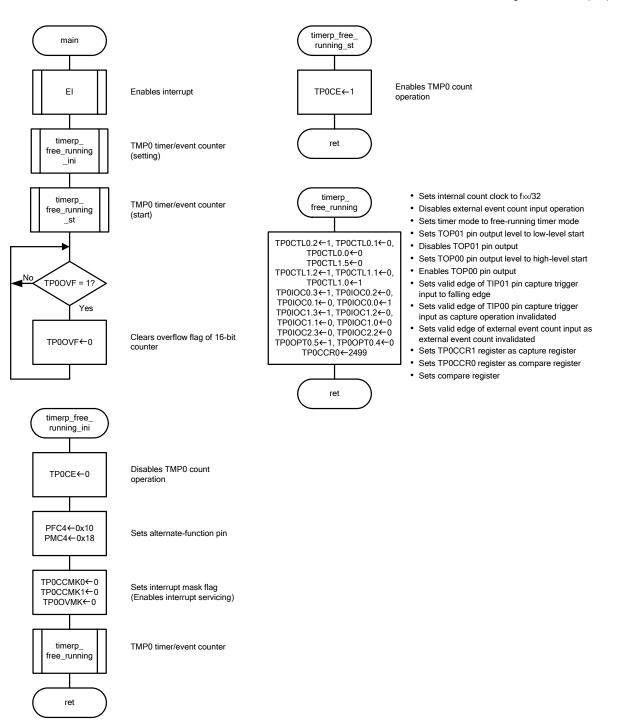
[Function name]	timerp_TP0CC0_int	
[Overview]	Defined by the user.	
[Factor]	INTTP0CC0 Match between the count value of the 16-bit counter and TP0CCR0	
[call function]	None	
[Variable]	None	
[File name]	timerp_free_running\timerp_6.c	
[Caution]	None	

[Function name]	timerp_TP0CC1_int	
[Overview]	Defined by the user.	
[Factor]	INTTP0CC1 Detects the valid edge of the TIP01 pin input.	
[call function]	None	
[Variable]	None	
[File name]	timerp_free_running\timerp_6.c	
[Caution]	None	

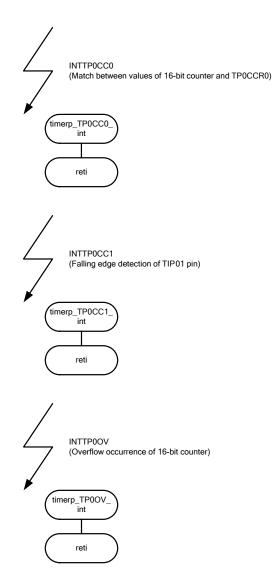
[Function name]	timerp_TP0OV_int	
[Overview]	Defined by the user.	
[Factor]	INTTP0OV	Overflow occurrence of 16-bit counter
[call function]	None	
[Variable]	None	
[File name]	timerp_free_runr	ning\timerp_6.c
[Caution]	None	

16-bit timer/event counter P (TMPn)

Free-running timer mode (1/2)



16-bit timer/event counter P (TMPn) Free-running timer mode (2/2)



16-bit timer/event counter P (TMPk) (k = 0, 2) Pulse width measurement mode

[Functions]	Clears the 16-bit counter by storing the count value to the TP0CCR0 register when the valid edge of the capture trigger input (TIP00 pin) is detected. Measures the valid edge interval of the TIP00 pin by generating an interrupt when the valid edge of the TIP00 pin input is detected and reading the TP0CCR0 register value. Can be implemented with TMP0 and TMP2.		
[Function name]	timerp_pulse_measure		
[Argument] [Processing content]	None Performs count operation of an fxx/32 count clock, generates an interrupt by storing the count value of the 16-bit counter to the TP0CCR0 register when the valid edge of the TIP00 pin input is detected, and clears the counter. Generates an INTTP0OV interrupt when a counter overflow is detected.		
[Starting method]	Starts by calling the timerp_pulse_measure_st function.		
[SFRs used]	 TP0CTL0 Selects the count clock. TP0CTL1 Selects the timer mode. TP0IOC1 Sets the valid edge of the capture trigger input signal (TIP00 and TIP01 pins). TP0IOC2 • Sets the valid edge of the external event counter input signal (TIP00 pin). • Sets the valid edge of the external trigger input signal (TIP00 pin). TP0OPT0 Selects between the capture/compare functions of the TP0CCR0 and TP0CCR1 registers. 		
	TP0CCR0 Capture register of the 16-bit counter		
[call function]	main main function		
[Variable]	None		
[Interrupts]	timerp_TP0CC0_int timerp_TP0OV_int		
[Interrupt sources]	INTTPOCCO INTTPOOV		
[File name]	timerp_pulse_measure\timerp_7.c, timerp_pulse_measure\MAIN.C		
[Cautions]	If a slow clock is selected as the count clock and a capture trigger is input immediately after the TP0CTL0.TP0CE bit has been set, 0xFFFF may be captured instead of 0x0000 to the TP0CCR0 register. The following care must be exercised for setting the registers. TPkCTL1 Bit 7: Only TMP0 is settable. TMP2 must be set to 0. TPkIOC0 Set to 0x00.		

The pulse width can be calculated by the following formula.

Pulse width = (Value of TP0CCR0 register + 1) \times Count clock cycle

The pulse width if an overflow of the 16-bit counter is detected can be calculated by the following formula.

Pulse width = (Value of TP0CCR0 register + 0x10001) × Count clock cycle

[Function name]	timerp_pulse_measure_st	
[Argument]	None	
[Processing content]	Starting function of timerp_pulse_measure	
[Starting method]	Call this function after calling	the timerp_pulse_measure function.
[SFR used]	TP0CTL0.TP0CE	Controls TMP0 operation.
[call function]	None	
[Variable]	None	
[File name]	timerp_pulse_measure\timerp_7.c	
[Caution]	None	

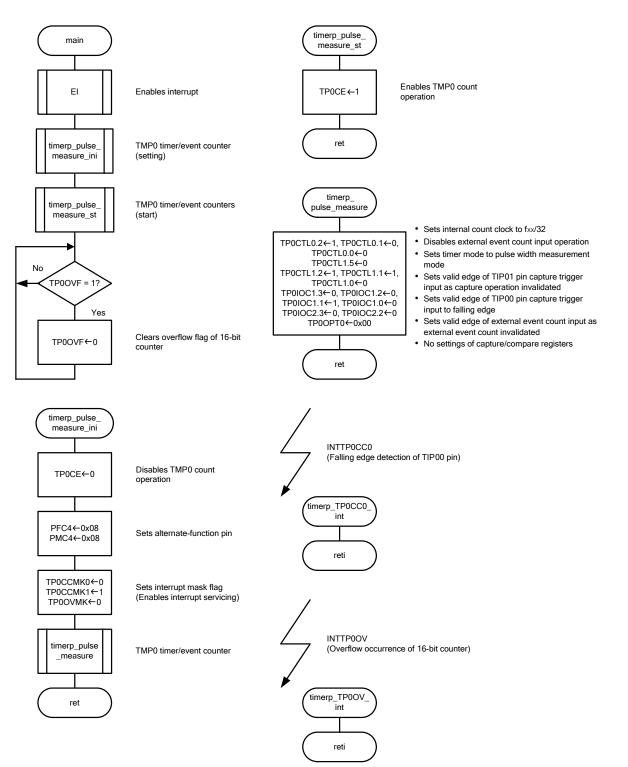
Interrupt functions

[Function name]	timerp_TP0CC0_int	
[Overview]	Defined by the user.	
[Factor]	INTTP0CC0 Valid edge detection of TIP00 pin input	
[call function]	None	
[Variable]	None	
[File name]	timerp_pulse_measure\timerp_7.c	
[Caution]	None	

[Function name]	timerp_TP0OV_int		
[Overview]	Defined by the user.		
[Factor]	INTTP0OV	Overflow occurrence of 16-bit counter	
[call function]	None		
[Variable]	None		
[File name]	timerp_pulse_measure\timerp_7.c		
[Caution]	None		

16-bit timer/event counter P (TMPk)

Pulse width measurement mode



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