To our customers,

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Renesas Electronics website: http://www.renesas.com

April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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This manual explains the sample program functions of the 16-bit timer/event counter P (TMP) for the V850E/IA4 microcontroller.

The explanations are based on usage with the V850E/IA4 microcontroller. Refer to this manual when using the V850E/IA3, V850ES/IK1, and V850ES/IE2 microcontrollers.

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This sample program is provided for reference purposes only and operations are therefore not subject to guarantee by NEC Electronics Corporation. When using this sample program, customers are kindly advised to sufficiently evaluate this product based on their system before usage.
NOTES FOR CMOS DEVICES

1. VOLTAGE APPLICATION WAVEFORM AT INPUT PIN
Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN).

2. HANDLING OF UNUSED INPUT PINS
Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

3. PRECAUTION AGAINST ESD
A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

4. STATUS BEFORE INITIALIZATION
Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

5. POWER ON/OFF SEQUENCE
In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

6. INPUT OF SIGNAL DURING POWER OFF STATE
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.
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Cautions 1. Download the program used in this manual from the NEC Electronics Website (http://www.necel.com/).

2. When using this sample program, reference the following startup file and link directive file and adjust them if as necessary.
   • Startup file: IA4_start.s
   • Link directive file: IA4_link.dir
Conventions  The function lists are structured as follows.

**Hardware name (symbol)**

<table>
<thead>
<tr>
<th>[Function(s)]</th>
<th>Function description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Function name]</td>
<td>Name of sample function</td>
</tr>
<tr>
<td>[Argument(s)]</td>
<td>Type and overview of argument(s)</td>
</tr>
<tr>
<td>[Processing content]</td>
<td>Processing content of sample function</td>
</tr>
<tr>
<td>[Starting method]</td>
<td>Conditions for calling a function</td>
</tr>
<tr>
<td>[SFR(s) used]</td>
<td>Register name and setting content</td>
</tr>
<tr>
<td>[call function(s)]</td>
<td>Name and function of call function(s)</td>
</tr>
<tr>
<td>[Variable(s)]</td>
<td>Type, name, and overview of variable(s) used in sample function</td>
</tr>
<tr>
<td>[Interrupt(s)]</td>
<td>Name of function</td>
</tr>
<tr>
<td>[Interrupt source(s)]</td>
<td>Name</td>
</tr>
<tr>
<td>[File name]</td>
<td>Name of corresponding sample program file</td>
</tr>
<tr>
<td>[Caution(s)]</td>
<td>Caution(s) upon function usage</td>
</tr>
</tbody>
</table>

**Interrupt function(s)**

<table>
<thead>
<tr>
<th>[Function name]</th>
<th>Name of interrupt function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Overview]</td>
<td>Processing content</td>
</tr>
<tr>
<td>[Factor(s)]</td>
<td>Name of interrupt and conditions for occurrence</td>
</tr>
<tr>
<td>[call function(s)]</td>
<td>None</td>
</tr>
<tr>
<td>[Variable(s)]</td>
<td>Name of variable, function</td>
</tr>
<tr>
<td>[File name]</td>
<td>Name of corresponding sample program file</td>
</tr>
<tr>
<td>[Caution(s)]</td>
<td>None</td>
</tr>
</tbody>
</table>

**Product Differences**  The differences between the V850E/IA4 and the V850E/IA3, V850ES/IK1, and V850ES/IE2 related to the 16-bit timer/event counter P (TMP) are shown below.

<table>
<thead>
<tr>
<th>Item</th>
<th>V850E/IA4</th>
<th>V850E/IA3</th>
<th>V850ES/IK1</th>
<th>V850ES/IE2</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP31 pin</td>
<td>Provided</td>
<td>Provided</td>
<td>Provided</td>
<td></td>
</tr>
<tr>
<td>Count clock</td>
<td>fxx/2, fxx/4, fxx/8, fxx/16, fxx/32, fxx/64, fxx/128, fxx/256</td>
<td>fxx/2, fxx/4, fxx/8, fxx/16, fxx/32, fxx/64, fxx/128, fxx/256</td>
<td>fxx, fxx/2, fxx/4, fxx/8, fxx/16, fxx/32, fxx/64, fxx/128, fxx/256</td>
<td>fxx/128</td>
</tr>
</tbody>
</table>

**Remark**  fxx: Peripheral clock frequency
Related Documents  The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

<table>
<thead>
<tr>
<th>Documents related to V850E/IA3, V850E/IA4, V850ES/IK1, and V850ES/IE2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Document Name</strong></td>
</tr>
<tr>
<td>V850E1  Architecture  User’s Manual</td>
</tr>
<tr>
<td>V850E/IA3, V850E/IA4  Hardware  User’s Manual</td>
</tr>
<tr>
<td>V850ES  Architecture  User’s Manual</td>
</tr>
<tr>
<td>V850ES/IK1  Hardware  User’s Manual</td>
</tr>
<tr>
<td>V850ES/IE2  Hardware  User’s Manual</td>
</tr>
<tr>
<td>Inverter Control by V850 Series  Vector Control by Hole Sensor  Application Note</td>
</tr>
<tr>
<td>Inverter Control by V850 Series  Vector Control by Encoder  Application Note</td>
</tr>
<tr>
<td>Inverter Control by V850 Series  120° Excitation Method Control by Zero-Cross Detection Application Note</td>
</tr>
<tr>
<td>Manual for Using Sample Program Functions  DMA Functions (V850E/IA3, V850E/IA4) Application Note</td>
</tr>
<tr>
<td>Manual for Using Sample Program Functions  Timer P (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2)  Application Note</td>
</tr>
<tr>
<td>Manual for Using Sample Program Functions  Timer ENC (V850E/IA3, V850E/IA4) Application Note</td>
</tr>
<tr>
<td>Manual for Using Sample Program Functions  Clock Generator (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2)  Application Note</td>
</tr>
</tbody>
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16-bit timer/event counter P (TMPn) (n = 0 to 3)
Interval timer mode

<table>
<thead>
<tr>
<th>[Functions]</th>
<th>Outputs a PWM waveform with a duty factor of 50% from the TOP00 pin at an interval set by the TP0CCR0 register.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Inverts the TOP01 pin output when the value set by the TP0CCR1 register and the count value of the 16-bit counter match.</td>
</tr>
<tr>
<td></td>
<td>Can be implemented with TMP0 to TMP3.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>[Function name]</th>
<th>timerp_interval</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Argument]</td>
<td>None</td>
</tr>
</tbody>
</table>

| [Processing content] | Performs count operation of an fxx/32 count clock, generates an interrupt by inverting the TOP00 pin output upon the count subsequent to the count whose value matches the value of the TP0CCR0 register, and clears the counter. |
|                      | Generates an interrupt by inverting the TOP01 pin output upon the count subsequent to the count whose value matches the value of the TP0CCR1 register. |
|                      | The TOP00 and TOP01 pins start output at high level. |

<table>
<thead>
<tr>
<th>[Starting method]</th>
<th>Starts by calling the timerp_interval_st function.</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>[SFRs used]</th>
<th>TP0CTL0</th>
<th>Selects the count clock.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TP0CTL1</td>
<td>Selects the timer mode.</td>
</tr>
<tr>
<td></td>
<td>TP0IOC0</td>
<td>• Sets the TOP00 and TOP01 pin outputs.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Sets the TOP00 and TOP01 pin output levels.</td>
</tr>
<tr>
<td></td>
<td>TP0CCR0</td>
<td>Compare register of the 16-bit counter</td>
</tr>
<tr>
<td></td>
<td>TP0CCR1</td>
<td>Compare register of the 16-bit counter</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>[call function]</th>
<th>main</th>
<th>main function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Variable]</td>
<td>None</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>[Interrupts]</th>
<th>timerp_TP0CC0_int</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>timerp_TP0CC1_int</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>[Interrupt sources]</th>
<th>INTTP0CC0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>INTTP0CC1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>[File name]</th>
<th>timerp_interval\timerp_1.c,</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>timerp_interval\MAIN.C</td>
</tr>
</tbody>
</table>
### [Cautions]

The following care must be exercised for setting the registers.

TPnCTL1 (n = 0 to 3)

- **Bit 7:** Only TMP0 and TMP1 are settable. TMP2 and TMP3 must be set to 0.
- **Bit 6:** Only TMP0, TMP2, and TMP3 are settable. TMP1 must be set to 0.
- **Bit 5:** Only TMP0 and TMP2 are settable. TMP1 and TMP3 must be set to 0.

TPmIOC0 (m = 0, 2, 3)

- Bits 1 and 0: Only TMP0 is valid. TMP2 and TMP3 must be set to 0.

The interval time can be calculated by the following formula.

\[
\text{Interval} = (\text{Set value of TP0CCR0 register} + 1) \times \text{Count clock cycle}
\]

<table>
<thead>
<tr>
<th>[Function name]</th>
<th>timerp_interval_st</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Argument]</td>
<td>None</td>
</tr>
<tr>
<td>[Processing content]</td>
<td>Starting function of timerp_interval</td>
</tr>
<tr>
<td>[Starting method]</td>
<td>Call this function after calling the timerp_interval function.</td>
</tr>
<tr>
<td>[SFR used]</td>
<td>TP0CTL0.TP0CE</td>
</tr>
<tr>
<td>[call function]</td>
<td>None</td>
</tr>
<tr>
<td>[Variable]</td>
<td>None</td>
</tr>
<tr>
<td>[File name]</td>
<td>timerp_interval\timerp_1.c</td>
</tr>
<tr>
<td>[Caution]</td>
<td>None</td>
</tr>
</tbody>
</table>
## Interrupt functions

<table>
<thead>
<tr>
<th>Function name</th>
<th>timerp_TP0CC0_int</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overview</td>
<td>Defined by the user.</td>
</tr>
<tr>
<td>Factor</td>
<td>INTTP0CC0 Match between the count value of the 16-bit counter and TP0CCR0</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>timerp_interval/timerp_1.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Function name</th>
<th>timerp_TP0CC1_int</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overview</td>
<td>Defined by the user.</td>
</tr>
<tr>
<td>Factor</td>
<td>INTTP0CC1 Match between the count value of the 16-bit counter and TP0CCR1</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>timerp_interval/timerp_1.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>
16-bit timer/event counter P (TMPn)

Interval timer mode

- Sets internal count clock to \( f_{XX}/32 \)
- Sets timer mode to interval timer mode
- Sets TOP01 pin output level to high-level start
- Enables TOP01 pin output
- Enables TOP00 pin output
- Sets compare register

- Sets internal count clock to \( f_{XX}/32 \)
- Sets timer mode to interval timer mode
- Sets TOP01 pin output level to high-level start
- Enables TOP01 pin output
- Enables TOP00 pin output
- Sets compare register
External event counter mode

[Functions] Counts the valid edge of the external event count input (TIP00 pin) and generates an interrupt request signal (INTTP0CC0) for each count set to the TP0CCR0 register. (Clears the 16-bit counter simultaneously.)
Generates an interrupt request signal (INTTP0CCR1) upon a compare match between the count value of the 16-bit counter and the value of the TP0CCR1 register.
Can be implemented with TMP0 and TMP2.

[Function name] timerp_event_count

[Argument] None

[Processing content] Counts the valid edge of the external event count input, generates an interrupt upon the count subsequent to the count whose value matches the value of the TP0CCR0 register, and clears the counter.
Generates an interrupt upon the count subsequent to the count whose value matches the value of the TP0CCR1 register.

[Starting method] Starts by calling the timerp_event_count_st function.

[SFRs used] TP0CTL0 Selects the count clock.
TP0CTL1 Selects the timer mode.
TP0IOC2 • Sets the valid edge of the external event count input signal (TIP00 pin).
• Sets the valid edge of the external trigger input signal (TIP00 pin).
TP0CCR0 Compare register of the 16-bit counter
TP0CCR1 Compare register of the 16-bit counter

[call function] main main function

[Variable] None

[Interrupts] timerp_TP0CC0_int
timerp_TP0CC1_int

[Interrupt sources] INTTP0CC0
INTTP0CC1

[File name] timerp_event_count	imerp_2.c,
timerp_event_count	MAIN.C

[Cautions] • The TP0CCR0 and TP0CCR1 registers must not be set to 0x0000.
• The following care must be exercised for setting the registers.
  TPkCTL1
  Bit 7: Only TMP0 settable. TMP2 must be set to 0.
  TPkIOC0
  Set to 0x00.
### Starting function of `timerp_event_count`

**Function name**: `timerp_event_count_st`  
**Argument**: None  
**Processing content**: Starting function of `timerp_event_count`  
**Starting method**: Call this function after calling the `timerp_event_count` function.  
**SFR used**: TP0CTL0.TP0CE - Controls TMP0 operation.  
**call function**: None  
**Variable**: None  
**File name**: `timerp_event_count_Timerp_2.c`  
**Caution**: None

### Interrupt functions

#### `timerp_TP0CC0_int`

**Function name**: `timerp_TP0CC0_int`  
**Overview**: Defined by the user.  
**Factor**: INTTP0CC0 - Match between the count value of the 16-bit counter and TP0CCR0  
**call function**: None  
**Variable**: None  
**File name**: `timerp_event_count_Timerp_2.c`  
**Caution**: None

#### `timerp_TP0CC1_int`

**Function name**: `timerp_TP0CC1_int`  
**Overview**: Defined by the user.  
**Factor**: INTTP0CC1 - Match between the count value of the 16-bit counter and TP0CCR1  
**call function**: None  
**Variable**: None  
**File name**: `timerp_event_count_Timerp_2.c`  
**Caution**: None
16-bit timer/event counter P (TMPk)

External event counter mode

- **TP0CE** = 0
  - Disables TMP0 count operation
- **TP0CE** = 1
  - Enables TMP0 count operation
- **PFC4** = 0x08
  - Sets alternate-function pin
- **PMC4** = 0x08
  - Sets interrupt mask flag (Enables interrupt servicing)
- **TP0CCMK0** = 0
  - Sets timer mode to external event count mode
- **TP0CCMK1** = 0
  - Sets valid edge of external event count input to falling edge
- **TP0CCR0** = 40
  - Sets compare register
- **TP0CCR1** = 20
  - No setting of internal count clock

**INTTP0CC0**
(Match between values of 16-bit counter and TP0CCR0)

**INTTP0CC1**
(Match between values of 16-bit counter and TP0CCR1)

**timerp_event_count**
- Enables interrupt
- TMP0 timer/event counter (setting)
- TMP0 timer/event counter (start)
- **ret**

**timerp_event_count_st**

**reti**

**timerp_event_count_in**

**reti**

**main**

**EI**

**timerp_event_count_in**

**TP0CE** = 0

**timerp_event_count**

**TP0CE** = 1

**ret**

**TP0CTL0** = 0x00
**TP0CTL1.1** = 1
**TP0IOC2.3** = 1
**TP0IOC2.2** = 0
**TP0CCR0** = 40
**TP0CCR1** = 20
### Functions

Starts operation of the 16-bit counter when the valid edge of the external trigger input (TIP00) is detected.

Clears the 16-bit counter upon a compare match with the TP0CCR0 register.

Inverts the TOP01 pin output upon a match between the value set by the TP0CCR1 register and the count value of the 16-bit counter.

Inverts the TOP01 pin output when the 16-bit counter is cleared.

Can be implemented with TMP0, TMP2, and TMP3 (software trigger only for TMP3).

### Function name

timerp_trigger_pulse

### Argument

None

### Processing content

Starts count operation of an fxx/32 count clock when the valid edge of the external trigger input is detected, generates an interrupt upon the count subsequent to the count whose value matches the value of the TP0CCR0 register, and clears the counter.

Generates an interrupt by inverting the TOP01 pin output upon the count subsequent to the count whose value matches the value of the TP0CCR1 register.

TOP01 pin starts output at high level.

### Starting method

Starts by calling the timerp_trigger_pulse_st function.

### SFRs used

- **TP0CTL0**: Selects the count clock.
- **TP0CTL1**: Selects the timer mode.
- **TP0IOC0**: Sets the valid edge of the external trigger input signal (TIP00 pin).
- **TP0IOC1**: Sets the TOP00 and TOP01 pin outputs.
- **TP0IOC2**: Sets the valid edge of the external event count input signal (TIP00 pin).
- **TP0CCR0**: Compare register of the 16-bit counter.
- **TP0CCR1**: Compare register of the 16-bit counter.

### call function

main function

### Variable

None

### Interrupts

timerp_TP0CC0_int

timerp_TP0CC1_int

### Interrupt sources

INTTP0CC0

INTTP0CC1

### File name

timerp_trigger_pulse

timerp_trigger_pulse

MAIN.C
[Cautions]

- The compare register is written in batch write mode.
  When changing the value of the compare register during timer operation, change the value of the TP0CCR1 register at the end.
- The following care must be exercised for setting the registers.
  TPmCTL1
    Bit 7: Only TMP0 is settable. TMP2 and TMP3 must be set to 0.
    Bit 5: Only TMP0 and TMP2 are settable. TMP3 must be set to 0
  TPmIOC0
    Bits 1 and 0: Only TMP0 is valid. TMP2 and TMP3 must be set to 0.

The active level width, cycle and duty factor of the PWM waveform can be calculated by the following formula.

Active level width = (Set value of TP0CCR1 register) × Count clock cycle
Cycle = (Set value of TP0CCR0 register + 1) × Count clock cycle
Duty factor = (Set value of TP0CCR1 register)/(Set value of TP0CCR0 register + 1)

[Function name] timerp_trigger_pulse_st
[Argument] None
[Processing content] Starting function of timerp_trigger_pulse
[Starting method] Call this function after calling the timerp_trigger_pulse function.
[SFR used] TP0CTL0.TP0CE Controls TMP0 operation.
[call function] None
[Variable] None
[File name] timerp_trigger_pulse_stimerp_3.c
[Caution] None
Interrupt functions

<table>
<thead>
<tr>
<th>Function name</th>
<th>timerp_TP0CC0_int</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overview</td>
<td>Defined by the user.</td>
</tr>
<tr>
<td>Factor</td>
<td>INTTP0CC0 Match between the count value of the 16-bit counter and TP0CCR0</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>timerp_trigger_pulse\timerp_3.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Function name</th>
<th>timerp_TP0CC1_int</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overview</td>
<td>Defined by the user.</td>
</tr>
<tr>
<td>Factor</td>
<td>INTTP0CC1 Match between the count value of the 16-bit counter and TP0CCR1</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>timerp_trigger_pulse\timerp_3.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>
16-bit timer/event counter P (TMPm)

External trigger pulse output mode

- Sets internal count clock to fXX/32
- Sets software trigger control as unused
- Disables external event count input operation
- Sets timer mode to external trigger pulse mode
- Sets TOP01 pin output level to high-level start
- Enables TOP01 pin output
- Enables TOP00 pin output level to low-level start
- Disables TOP00 pin output
- Sets valid edge of external event count input as external event count invalidated
- Sets valid edge of external trigger input to falling edge
- Sets compare register

Disables TMP0 count operation

Sets alternate-function pin

Sets interrupt mask flag (Enables interrupt servicing)

Enables TMP0 count operation
### 16-bit timer/event counter P (TMPm) (m = 0, 2, 3)

**One-shot pulse output mode**

<table>
<thead>
<tr>
<th>[Functions]</th>
<th>Starts operation of the 16-bit counter when the valid edge of the external trigger input (TIP00 pin) is detected. Stops the count when the 16-bit counter is cleared upon a compare match with the TP0CCR0 register. Inverts the TOP01 pin output upon a match between the value set by the TP0CCR1 register and the count value of the 16-bit counter. Inverts the TOP01 pin output when the 16-bit counter is cleared. Can be implemented with TMP0, TMP2, and TMP3 (software trigger only for TMP3).</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Function name]</td>
<td>timerp_1shot_pulse</td>
</tr>
<tr>
<td>[Argument]</td>
<td>None</td>
</tr>
<tr>
<td>[Processing content]</td>
<td>Starts count operation of an fxx/32 count clock upon valid edge detection of the external trigger input, generates an interrupt by inverting the TOP01 pin output upon the count subsequent to the count whose value matches the value of the TP0CCR0 register, clears the counter, and stops count operation. Generates an interrupt by inverting the TOP01 pin output upon the count subsequent to the count whose value matches the value of the TP0CCR1 register. TOP01 pin starts output at high level.</td>
</tr>
<tr>
<td>[Starting method]</td>
<td>Starts by calling the timerp_1shot_pulse_st function.</td>
</tr>
<tr>
<td>[SFRs used]</td>
<td>TP0CTL0 Selects the count clock. TP0CTL1 Selects the timer mode. TP0IOC0 • Sets the TOP00 and TOP01 pin outputs. • Sets the TOP00 and TOP01 pin output levels. TP0IOC2 • Sets the valid edge of the external event count input signal (TIP00 pin). • Sets the valid edge of the external trigger input signal (TIP00 pin). TP0CCR0 Compare register of the 16-bit counter TP0CCR1 Compare register of the 16-bit counter</td>
</tr>
<tr>
<td>[call function]</td>
<td>main function</td>
</tr>
<tr>
<td>[Variable]</td>
<td>None</td>
</tr>
<tr>
<td>[Interrupts]</td>
<td>timerp_TP0CC0_int timerp_TP0CC1_int</td>
</tr>
<tr>
<td>[Interrupt sources]</td>
<td>INTTP0CC0 INTTP0CC1</td>
</tr>
<tr>
<td>[File name]</td>
<td>timerp_1shot_pulse timerp_4.c, timerp_1shot_pulse MAIN.C</td>
</tr>
</tbody>
</table>
The output delay period and the active level width of the one-shot pulse can be calculated from the following formula.

Output delay period = \( (\text{Set value of TP0CCR1 register}) \times \text{Count clock cycle} \)

Active level width = \( (\text{Set value of TP0CCR0 register} - \text{Set value of TP0CCR1 register} + 1) \times \text{Count clock cycle} \)

[Function name] timerp_1shot_pulse_st
[Argument] None
[Processing content] Starting function of timerp_1shot_pulse
[Starting method] Call this function after calling the timerp_1shot_pulse function.
[SFR used] TP0CTL0.TP0CE Controls TMP0 operation.
[call function] None
[Variable] None
[File name] timerp_1shotpulse_timerp_4.c
[Cautions] None
### Interrupt functions

<table>
<thead>
<tr>
<th>Function name</th>
<th>timerp_TP0CC0_int</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overview</td>
<td>Defined by the user.</td>
</tr>
<tr>
<td>Factor</td>
<td>INTTP0CC0 Match between the count value of the 16-bit counter and TP0CCR0</td>
</tr>
<tr>
<td>Call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>timerp_1shot_pulse\timerp_4.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Function name</th>
<th>timerp_TP0CC1_int</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overview</td>
<td>Defined by the user.</td>
</tr>
<tr>
<td>Factor</td>
<td>INTTP0CC1 Match between the count value of the 16-bit counter and TP0CCR1</td>
</tr>
<tr>
<td>Call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>timerp_1shot_pulse\timerp_4.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>
16-bit timer/event counter P (TMPm)

One-shot pulse output mode

- Enables interrupt
- Sets internal count clock to fXX/32
- Sets software trigger control as unused
- Disables external event count input operation
- Sets timer mode to one-shot pulse output mode
- Sets TOP01 pin output level to high-level start
- Enables TOP01 pin output
- Sets TOP00 pin output level to low-level start
- Enables TOP00 pin output
- Sets valid edge of external event count input as external event count invalidated
- Sets valid edge of external trigger input to falling edge
- Sets compare register

TP0CC0 = 2499
TP0CC1 = 1249

INTTP0CC0 (Match between values of 16-bit counter and TP0CCR0)
INTTP0CC1 (Match between values of 16-bit counter and TP0CCR1)

TP0CTL0.2 = 1, TP0CTL0.1 = 0,
TP0CTL0.0 = 0
TP0CTL1.6 = 0, TP0CTL1.5 = 0
TP0IOC0.3 = 0, TP0IOC0.2 = 1,
TP0IOC0.1 = 1, TP0IOC0.0 = 0
TP0IOC2.3 = 0, TP0IOC2.2 = 0
TP0IOC2.1 = 1, TP0IOC2.0 = 0
TP0CCR0 = 2499
TP0CCR1 = 1249

TP0CE = 1
Enables TOP0 count operation

TP0CE = 0
Disables TOP0 count operation

PFC4 = 0x08
PMC4 = 0x18

TP0CCMK0 = 0
TP0CCMK1 = 0

TP0IOC3 = 0, TP0IOC2 = 1,
TP0IOC1 = 1, TP0IOC0 = 0
TP0IOC2 = 0, TP0IOC1 = 0
TP0IOC0 = 1

TP0CCR0 = 2499
TP0CCR1 = 1249

TP0CE = 1
Enables TOP0 count operation

TP0CE = 0
Disables TOP0 count operation
16-bit timer/event counter P (TMPm) \((m = 0, 2, 3)\)

**PWM output mode**

| Functions | Starts operation of the 16-bit counter by setting the TP0CE bit. Outputs a PWM waveform with a 50% duty factor whose half cycle is equal to the set value of the TP0CCR0 register + 1, by clearing the 16-bit counter upon a compare match with the TP0CCR0 register and inverting the TOP0 pin. Inverts the TOP01 pin output upon a match between the value set by the TP0CCR1 register and the count value of the 16-bit counter. Inverts the TOP01 pin output when the 16-bit counter is cleared. Can be implemented with TMP0, TMP2, and TMP3. |
| Function name | timerp_pwm_output |
| Argument | None |
| Processing content | Performs count operation of an fxx/32 count clock, generates an interrupt by inverting the TOP00 and TOP01 pin outputs upon the count subsequent to the count whose value matches the value of the TP0CCR0 register, and clears the counter. Generates an interrupt by inverting the TOP01 pin output upon the count subsequent to the count whose value matches the value of the TP0CCR1 register. The TOP00 and TOP01 pins start output at high level. |
| Starting method | Starts by calling the timerp_pwm_output_st function. |
| SFRs used | TP0CTL0 Selects the count clock. TP0CTL1 Selects the timer mode. TP0IOC0 • Sets the TOP00 and TOP01 pin outputs. • Sets the TOP00 and TOP01 pin output levels. TP0IOC2 • Sets the valid edge of the external event counter input signal (TIP00 pin). • Sets the valid edge of the external trigger input signal (TIP00 pin). TP0CCR0 Compare register of the 16-bit counter TP0CCR1 Compare register of the 16-bit counter |
| Call function | main main function |
| Variable | None |
| Interrupts | timerp_TP0CC0_int timerp_TP0CC1_int |
| Interrupt sources | INTTP0CC0 INTTP0CC1 |
| File name | timerp_pwm_output timerp_5.c, timerp_pwm_output MAIN.C |
[Cautions]

- The compare register is written in batch write mode. When changing the value of the compare register during timer operation, change the value of the TP0CCR1 register at the end.
- The following care must be exercised for setting the registers.

TPmCTL1

  Bit 7: Only TMP0 is settable. TMP2 and TMP3 must be set to 0.
  Bit 5: Only TMP0 and TMP2 are settable. TMP3 must be set to 0

TPmIOC0

  Bits 1 and 0: Only TMP0 is valid. TMP2 and TMP3 must be set to 0.

The active level width, cycle, and duty factor of the PWM waveform output from the TOP01 pin can be calculated from the following formula.

Active level width = (Set value of TP0CCR1 register) × Count clock cycle

Cycle = (Set value of TP0CCR0 register + 1) × Count clock cycle

Duty factor = (Set value of TP0CCR1 register)/(Set value of TP0CCR0 register + 1)

---

**[Function name]** timerp_pwm_output_st

**[Argument]** None

**[Processing content]** Starting function of timerp_pwm_output

**[Starting method]** Call this function after calling the timerp_pwm_output function.

**[SFR used]**

  TP0CTL0.TP0CE Controls TMP0 operation.

**[call function]** None

**[Variable]** None

**[File name]** timerp_pwm_output_timerp_5.c

**[Caution]** None
## Interrupt functions

<table>
<thead>
<tr>
<th>Function name</th>
<th>timerp_TP0CC0_int</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Overview</strong></td>
<td>Defined by the user.</td>
</tr>
<tr>
<td><strong>Factor</strong></td>
<td>INTTP0CC0 Match between the count value of the 16-bit counter and TP0CCR0</td>
</tr>
<tr>
<td><strong>call function</strong></td>
<td>None</td>
</tr>
<tr>
<td><strong>Variable</strong></td>
<td>None</td>
</tr>
<tr>
<td><strong>File name</strong></td>
<td>timerp_pwm_output/timerp_5.c</td>
</tr>
<tr>
<td><strong>Caution</strong></td>
<td>None</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Function name</th>
<th>timerp_TP0CC1_int</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Overview</strong></td>
<td>Defined by the user.</td>
</tr>
<tr>
<td><strong>Factor</strong></td>
<td>INTTP0CC1 Match between the count value of the 16-bit counter and TP0CCR1</td>
</tr>
<tr>
<td><strong>call function</strong></td>
<td>None</td>
</tr>
<tr>
<td><strong>Variable</strong></td>
<td>None</td>
</tr>
<tr>
<td><strong>File name</strong></td>
<td>timerp_pwm_output/timerp_5.c</td>
</tr>
<tr>
<td><strong>Caution</strong></td>
<td>None</td>
</tr>
</tbody>
</table>
16-bit timer/event counter P (TMP\textsubscript{m})

PWM output mode

- Sets internal count clock to \( f_{\text{sys}}/32 \)
- Sets software trigger control as unused
- Disables external event count input operation
- Sets timer mode to PWM output mode
- Sets TOP01 pin output level to high-level start
- Enables TOP01 pin output
- Sets TOP00 pin output level to high-level start
- Enables TOP00 pin output
- Sets valid edge of external event count input as external event count invalidated
- Sets valid edge of external trigger input as external trigger invalidated
- Enables compare register

```
main
  EI
  timerp_pwm_output
    timerp_pwm_output_init
      TP0CE \leftarrow 0
      PFC4 \leftarrow 0x00
      PMC4 \leftarrow 0x18
      TP0CCMK0 \leftarrow 0
      TP0CCMK1 \leftarrow 0
      timerp_pwm_output
        ret
      reti
    timerp_pwm_output_start
      TP0CE \leftarrow 1
      ret

timerp_pwm_output
  PFC4 \leftarrow 0x00
  PMC4 \leftarrow 0x18
  TP0CCMK0 \leftarrow 0
  TP0CCMK1 \leftarrow 0
  timerp_pwm_output
    ret
  reti
```

- Enables interrupt
- Sets interrupt mask flag (Enables interrupt servicing)
- Sets valid edge of external event count input as external event count invalidated
- Sets valid edge of external trigger input as external trigger invalidated
- Enables compare register
16-bit timer/event counter P (TMPn) (n = 0 to 3)
Free-running timer mode

<table>
<thead>
<tr>
<th>Functions</th>
<th>Inverts the TOP00 pin output upon a compare match between the TP0CCR0 register and the count value of the 16-bit counter (compare function). Stores the count value of the 16-bit counter when the valid edge of the capture trigger input (TIP01 pin) is detected (capture function). The compare function can be implemented with TMP0 to TMP3. The capture function can be implemented with TMP0 and TMP2.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function name</td>
<td>timerp_free_running</td>
</tr>
<tr>
<td>Argument</td>
<td>None</td>
</tr>
<tr>
<td>Processing content</td>
<td>Performs count operation of an fxx/32 count clock, generates an interrupt by inverting the TOP00 pin output upon the count subsequent to the count whose value matches the value of the TP0CCR0 register, and clears the counter. Generates an interrupt by capturing the count value to the TP0CCR1 register when the valid edge from the TIP01 pin is detected. Generates an INTTP0OV interrupt when a counter overflow is detected. The TOP00 pin starts output at high level.</td>
</tr>
<tr>
<td>Starting method</td>
<td>Starts by calling the timerp_free_running_st function.</td>
</tr>
<tr>
<td>SFRs used</td>
<td>TP0CTL0 Selects the count clock. TP0CTL1 Selects the timer mode. TP0IOC0 • Sets the TOP00 and TOP01 pin outputs. • Sets the TOP00 and TOP01 pin output levels. TP0IOC1 Sets the valid edge of the capture trigger input signal (TIP00 and TIP01 pins) TP0IOC2 • Sets the valid edge of the external event count input signal (TIP00 pin). • Sets the valid edge of the external trigger input signal (TIP00 pin). TP0OPT0 Selects the capture/compare functions of the TP0CCR0 and TP0CCR1 registers. TP0CCR0 Compare register of the 16-bit counter TP0CCR1 Compare register of the 16-bit counter</td>
</tr>
<tr>
<td>call function</td>
<td>main main function</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>Interrupts</td>
<td>timerp_TP0CC0_int timerp_TP0CC1_int timerp_TP0OV_int</td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>INTTP0CC0 INTTP0CC1 INTTP0OV</td>
</tr>
</tbody>
</table>
[File name]  timerp_free_running\timerp_6.c,
timerp_free_running\MAIN.C

[Caution]  • The following care must be exercised for setting the registers.

TPnCTL1
   Bit 7: Only TMP0 and TMP1 are settable. TMP2 and TMP3 must be set to 0.
   Bit 6: Only TMP0, TMP2, and TMP3 are settable. TMP1 must be set to 0.
   Bit 5: Only TMP0 and TMP2 are settable. TMP1 and TMP3 must be set to 0.

TPmIOC0 (m = 0, 2, 3)
   Bits 1 and 0: Only TMP0 is valid. TMP2 and TMP3 must be set to 0.

TPnOPT0
   Bits 5 and 4: Only TMP0 and TMP2 are valid. TMP1 and TMP3 must be set to 0.

[Function name]  timerp_free_running_st

[Argument]  None

[Processing content]  Starting function of timerp_free_running

[Starting method]  Call this function after calling the timerp_free_running function.

[SFR used]  TP0CTL0.TP0CE  Controls TMP0 operation.

[call function]  None

[Variable]  None

[File name]  timerp_free_running\timerp_6.c

[Caution]  None
## Interrupt functions

<table>
<thead>
<tr>
<th>Function name</th>
<th>timerp_TP0CC0_int</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overview</td>
<td>Defined by the user.</td>
</tr>
<tr>
<td>Factor</td>
<td>INTTP0CC0 Match between the count value of the 16-bit counter and TP0CCR0</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>timerp_free_running/timerp_6.c</td>
</tr>
<tr>
<td>Caution</td>
<td>None</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Function name</th>
<th>timerp_TP0CC1_int</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overview</td>
<td>Defined by the user.</td>
</tr>
<tr>
<td>Factor</td>
<td>INTTP0CC1 Detects the valid edge of the TIP01 pin input.</td>
</tr>
<tr>
<td>call function</td>
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<tr>
<td>Variable</td>
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</tr>
<tr>
<td>File name</td>
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<td>Caution</td>
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<tr>
<td>Overview</td>
<td>Defined by the user.</td>
</tr>
<tr>
<td>Factor</td>
<td>INTTP0OV Overflow occurrence of 16-bit counter</td>
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<tr>
<td>call function</td>
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</tr>
<tr>
<td>Variable</td>
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<td>Caution</td>
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</table>
16-bit timer/event counter P (TMPn)
Free-running timer mode (1/2)

- Enables interrupt
- Enables TMP0 count operation
- Sets TP0OVF = 1?
- Clears overflow flag of 16-bit counter
- Disables TMP0 count operation
- Sets alternate-function pin
- Sets interrupt mask flag (Enables interrupt servicing)
- Sets internal count clock to fXX/32
- Disables external event count input operation
- Sets timer mode to free-running timer mode
- Enables TOP00 pin output
- Enables TOP00 pin output
- Sets valid edge of TOP01 pin capture trigger input as external event count invalidated
- Enables TOP00 pin output
- Sets valid edge of external event count input as external event count invalidated
- Enables TOP00 pin output
- Sets TP0CCR0 register as compare register
- Sets TP0CCR1 register as capture register
- Sets compare register
- Sets TOP00 pin output level to high-level start
- Enables TOP00 pin output
- Sets valid edge of TIP00 pin capture trigger input as capture operation invalidated
- Enables TOP00 pin output
- Sets valid edge of TIP01 pin capture trigger input as external event count input as capture operation invalidated
- Enables TOP00 pin output
- Sets valid edge of external event count input as external event count invalidated
- Enables TOP00 pin output
- Sets valid edge of TIP00 pin capture trigger input as capture operation invalidated
- Enables TOP00 pin output
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- Sets valid edge of TIP01 pin capture trigger input as external event count input as capture operation invalida
16-bit timer/event counter P (TMPn)
Free-running timer mode (2/2)

INTTP0CC0
(Match between values of 16-bit counter and TP0CCR0)

INTTP0CC1
(Falling edge detection of TIP01 pin)

INTTP0OV
(Overflow occurrence of 16-bit counter)
16-bit timer/event counter P (TMPk) (k = 0, 2)
Pulse width measurement mode

[Functions] Clears the 16-bit counter by storing the count value to the TP0CCR0 register when the valid edge of the capture trigger input (TIP00 pin) is detected. Measures the valid edge interval of the TIP00 pin by generating an interrupt when the valid edge of the TIP00 pin input is detected and reading the TP0CCR0 register value. Can be implemented with TMP0 and TMP2.

[Function name] timerp_pulse_measure

[Argument] None

[Processing content] Performs count operation of an fx/32 count clock, generates an interrupt by storing the count value of the 16-bit counter to the TP0CCR0 register when the valid edge of the TIP00 pin input is detected, and clears the counter. Generates an INTTP0OV interrupt when a counter overflow is detected.

[Starting method] Starts by calling the timerp_pulse_measure_st function.

[SFRs used] TP0CTL0 Selects the count clock.
TP0CTL1 Selects the timer mode.
TP0IOC1 Sets the valid edge of the capture trigger input signal (TIP00 and TIP01 pins).
TP0IOC2 • Sets the valid edge of the external event counter input signal (TIP00 pin).
• Sets the valid edge of the external trigger input signal (TIP00 pin).
TP0OPT0 Selects between the capture/compare functions of the TP0CCR0 and TP0CCR1 registers.
TP0CCR0 Capture register of the 16-bit counter

[call function] main main function

[Variable] None

[Interrupts] timerp_TP0CC0_int
timerp_TP0OV_int

[Interrupt sources] INTTP0CC0
INTTP0OV

[File name] timerp_pulse_measure\timerp_7.c,
timerp_pulse_measure\MAIN.C

[Cautions] • If a slow clock is selected as the count clock and a capture trigger is input immediately after the TP0CTL0.TP0CE bit has been set, 0xFFFF may be captured instead of 0x0000 to the TP0CCR0 register.
• The following care must be exercised for setting the registers.
TPkCTL1
Bit 7: Only TMP0 is settable. TMP2 must be set to 0.
TPkIOC0
Set to 0x00.
The pulse width can be calculated by the following formula.

\[
\text{Pulse width} = (\text{Value of TP0CCR0 register} + 1) \times \text{Count clock cycle}
\]

The pulse width if an overflow of the 16-bit counter is detected can be calculated by the following formula.

\[
\text{Pulse width} = (\text{Value of TP0CCR0 register} + 0x10001) \times \text{Count clock cycle}
\]

- **Function name**: timerp_pulse_measure_st
- **Argument**: None
- **Processing content**: Starting function of timerp_pulse_measure
- **Starting method**: Call this function after calling the timerp_pulse_measure function.
- **SFR used**: TP0CTL0.TP0CE  Controls TMP0 operation.
- **call function**: None
- **Variable**: None
- **File name**: timerp_pulse_measure\timerp_7.c
- **Caution**: None
## Interrupt functions

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<td>INTTP0CC0</td>
</tr>
<tr>
<td></td>
<td>Valid edge detection of TIP00 pin input</td>
</tr>
<tr>
<td>call function</td>
<td>None</td>
</tr>
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16-bit timer/event counter P (TMPk)
Pulse width measurement mode

main

EI

Enables interrupt

timerp_pulse_measure_init

TMP0 timer/event counter (setting)

timerp_pulse_measure_init

TMP0 timer/event counters (start)

TP0OVF = 1?

Yes

No

TP0OVF = 0

Clears overflow flag of 16-bit counter

ret

TP0CE ← 0

Disables TMP0 count operation

PFC4 ← 0x08
PMC4 ← 0x08

TP0CCMK0 ← 0
TP0CCMK1 ← 1
TP0OVMK ← 0

TP0IC0C1.3 ← 0, TP0IC0C1.2 ← 0, TP0IC0C1.1 ← 1, TP0IC0C1.0 ← 0
TP0IC0C2.3 ← 0, TP0IC0C2.2 ← 0
TP0OPT0 ← 0x00

ret

timerp_pulse_measure

TP0CE ← 1

Enables TMP0 count operation

timerp_pulse_measure

* Sets internal count clock to fCLK/32
* Disables external event count input operation
* Sets timer mode to pulse width measurement mode
* Sets valid edge of TP00 pin capture trigger input as capture operation invalidated
* Sets valid edge of TP00 pin capture trigger input to falling edge
* Sets valid edge of external event count input as external event count invalidated
* No settings of capture/compare registers

INTP0CC0
(Falling edge detection of TP00 pin)

timerp_TP0CC0_init

reti

INTTP0OV
(Overflow occurrence of 16-bit counter)

timerp_TP0OV_init

reti

TP0OVF ← 0
Clears overflow flag of 16-bit counter

• Sets internal count clock to fCLK/32
• Disables external event count input operation
• Sets timer mode to pulse width measurement mode
• Sets valid edge of TP01 pin capture trigger input as capture operation invalidated
• Sets valid edge of TP00 pin capture trigger input to falling edge
• Sets valid edge of external event count input as external event count invalidated
• No settings of capture/compare registers

Ret
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