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April 1st, 2010
Renesas Electronics Corporation

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This manual explains the sample program functions of the clock generator for the V850E/IA4 microcontroller. The explanations are based on usage with the V850E/IA4 microcontroller. Refer to this manual when using the V850E/IA3, V850ES/IK1, and V850ES/IE2 microcontrollers.

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NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN
Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

② HANDLING OF UNUSED INPUT PINS
Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD
A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION
Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE
In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.
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INTRODUCTION

Cautions

1. Download the program used in this manual from the NEC Electronics Website (http://www.necel.com/).
2. When using this sample program, reference the following startup file and link directive file and adjust them if as necessary.
   - Startup file: IA4_start.s
   - Link directive file: IA4_link.dir

Conventions

The function lists are structured as follows.

<table>
<thead>
<tr>
<th>Hardware name</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Function] Function description</td>
</tr>
<tr>
<td>[Function name] Name of sample function</td>
</tr>
<tr>
<td>[Argument] Type and overview of argument</td>
</tr>
<tr>
<td>[Processing content] Processing content of sample function</td>
</tr>
<tr>
<td>[Starting method] Conditions for calling a function</td>
</tr>
<tr>
<td>[SFR(s) used] Register name and setting content</td>
</tr>
<tr>
<td>[call function(s)] Name and function of call function(s)</td>
</tr>
<tr>
<td>[Variable(s)] Type, name, and overview of variable(s) used in sample function</td>
</tr>
<tr>
<td>[Interrupt(s)] Name of function</td>
</tr>
<tr>
<td>[Interrupt source(s)] Name</td>
</tr>
<tr>
<td>[File name] Name of corresponding sample program file</td>
</tr>
<tr>
<td>[Caution(s)] Caution(s) upon function usage</td>
</tr>
</tbody>
</table>

Product Differences

The differences between the V850E/IA4 and the V850E/IA3, V850ES/IK1, and V850ES/IE2 related to the clock generator are shown below.

<table>
<thead>
<tr>
<th>Item</th>
<th>V850E/IA4</th>
<th>V850E/IA3</th>
<th>V850ES/IK1</th>
<th>V850ES/IE2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resonator</td>
<td>4 to 8 MHz resonator connectable (external clock input prohibited)</td>
<td>4 to 8 MHz resonator connectable (external clock input prohibited)</td>
<td>2.5 to 4 MHz resonator connectable (external clock input prohibited)</td>
<td>2.5 MHz resonator connectable (external clock input prohibited)</td>
</tr>
<tr>
<td>Multiplication function by PLL clock synthesizer</td>
<td>Fixed to multiplication by eight, fxx = 32 to 64 MHz</td>
<td>Fixed to multiplication by eight, fxx = 32 to 64 MHz</td>
<td>Fixed to multiplication by eight, fxx = 20 to 32 MHz</td>
<td>Fixed to multiplication by eight, fxx = 20 MHz</td>
</tr>
<tr>
<td>PLL operation specifiable by PLLSIN pin</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>

Remark

fxx: System clock frequency
### Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

### Documents related to V850E/IA3, V850E/IA4, V850ES/IK1, and V850ES/IE2

<table>
<thead>
<tr>
<th>Document Name</th>
<th>Document No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>V850E1 Architecture User’s Manual</td>
<td>U14559E</td>
</tr>
<tr>
<td>V850E/IA3, V850E/IA4 Hardware User’s Manual</td>
<td>U16543E</td>
</tr>
<tr>
<td>V850ES Architecture User’s Manual</td>
<td>U15943E</td>
</tr>
<tr>
<td>V850ES/IK1 Hardware User’s Manual</td>
<td>U16910E</td>
</tr>
<tr>
<td>V850ES/IE2 Hardware User’s Manual</td>
<td>U17716E</td>
</tr>
<tr>
<td>Inverter Control by V850 Series Vector Control by Hole Sensor Application Note</td>
<td>U17338E</td>
</tr>
<tr>
<td>Inverter Control by V850 Series Vector Control by Encoder Application Note</td>
<td>U17324E</td>
</tr>
<tr>
<td>Inverter Control by V850 Series 120° Excitation Method Control by Zero-Cross Detection Application Note</td>
<td>U17209E</td>
</tr>
<tr>
<td>Manual for Using Sample Program Functions DMA Functions (V850E/IA3, V850E/IA4) Application Note</td>
<td>U18235E</td>
</tr>
<tr>
<td>Manual for Using Sample Program Functions Timer ENC (V850E/IA3, V850E/IA4) Application Note</td>
<td>U18240E</td>
</tr>
<tr>
<td>Manual for Using Sample Program Functions Clock Generator (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) This manual</td>
<td></td>
</tr>
</tbody>
</table>
CONTENTS

Clock generator

PLL mode ................................................................. 7

Clock generator

Clock monitor mode .................................................. 11
Clock generator

PLL mode

[Function] Sets the clock frequency by setting the CPU operation clock (PLL mode) and the PCC register which is a special register.

[Function name] pll_main

[Argument] None

[Processing content] Calls the PLL setting function by stopping all DMAs in use.

[Starting method] None

[SFR used] None

[call functions] clock_pll_mode, clock_pcc_mode

[Variable] None

[Interrupt] None

[Interrupt source] None

[File name] clock_generator1.c

[Caution] Note that if the pll_main function is called the maskable interrupt request will not be enabled (EI).

[Function name] clock_pll_mode

[Processing content] Sets to PLL mode by the PLLCTL register.

[SFR used] PLLCTL: 0x03 (Sets to PLL mode.)

[call function] None

[Variable] None

[File name] clock_generator1.c

[Caution] None
[Function name]           clock_pcc_mode
[Processing content]    Sets the PCC register by forcibly terminating DMA transfer.
[SFRs used]             DCHC0.TC0         DMA0 transfer status bit
                        DCHC0.E00:    1 (Enables DMA0 transfer.)
                        DCHC0.INIT0: 1 (Forcibly terminates DMA0 transfer.)
                        DCHC1.TC1     DMA1 transfer status bit
                        DCHC1.E11:    1 (Enables DMA1 transfer.)
                        DCHC1.INIT1:  1 (Forcibly terminates DMA1 transfer.)
                        DCHC2.TC2     DMA2 transfer status bit
                        DCHC2.E22:    1 (Enables DMA2 transfer.)
                        DCHC2.INIT2:  1 (Forcibly terminates DMA2 transfer.)
                        DCHC3.TC3     DMA3 transfer status bit
                        DCHC3.E33:    1 (Enables DMA3 transfer.)
                        DCHC3.INIT3:  1 (Forcibly terminates DMA3 transfer.)
                        PRCMD:        0x00 (Writes to command register
                                        (used when writing to a special register).)
                        PCC:          0x00 (Selects clock as fXX.)
[call function]         None
[Variable]              None
[File name]             clock_generator1.c
[Caution]               • DMA transfer is forcibly terminated in this sample program, because all DMA transfers
                        must be terminated before performing data setting to the special register.
                        • Set the PCC register after switching to the PLL mode. The PCC register is a special
                          register and can therefore only be written in a combination of specific sequences.
Clock generator
PLL mode (1/2)

pll_main

DI

Disables maskable interrupt request

clock_pll_mode

PLL mode setting function

clock_pcc_mode

PCC register setting function

PRERR == 1

No

Checks protection error flag

Yes

ret
Clock generator
PLL mode (2/2)

PLL mode setting function

**clock_pll_mode**

PLLCTL = 0x03

Sets CPU operation clock to PLL mode

ret

PCC register setting function

**clock_pcc_mode**

TC0 == 0 && E00 == 1

Yes

INIT0 = 1

No

Checks DMA0 transfer

Forcibly terminates DMA0

TC1 == 0 && E11 == 1

Yes

INIT1 = 1

No

Checks DMA1 transfer

Forcibly terminates DMA1

TC2 == 0 && E22 == 1

Yes

INIT2 = 1

No

Checks DMA2 transfer

Forcibly terminates DMA2

TC3 == 0 && E33 == 1

Yes

INIT3 = 1

No

Checks DMA3 transfer

Forcibly terminates DMA3

PRCMD = 0x00

Writes to command register

PCC = 0x00

Selects clock as fXX

NOP instruction × 5

Inserts five NOP instructions

ret

Clock_pcc_mode

PRCMD = 0x00

Sets CPU operation clock to PLL mode

ret
# Clock generator

## Clock monitor mode

<table>
<thead>
<tr>
<th>Function</th>
<th>Performs clock monitor operation.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function name</td>
<td>clock_monitor_main</td>
</tr>
<tr>
<td>Argument</td>
<td>None</td>
</tr>
<tr>
<td>Processing content</td>
<td>Enables operation of the clock monitor mode by calling the clock monitor mode function.</td>
</tr>
<tr>
<td>Starting method</td>
<td>None</td>
</tr>
<tr>
<td>SFR used</td>
<td>None</td>
</tr>
<tr>
<td>call function</td>
<td>clock_monitor_mode</td>
</tr>
<tr>
<td>Variable</td>
<td>None</td>
</tr>
<tr>
<td>Interrupt</td>
<td>None</td>
</tr>
<tr>
<td>Interrupt source</td>
<td>None</td>
</tr>
<tr>
<td>File name</td>
<td>clock_generator2.c</td>
</tr>
<tr>
<td>Caution</td>
<td>Note that if the clock_monitor_main function is called the maskable interrupt request will not be enabled (EI).</td>
</tr>
</tbody>
</table>
[Function name] clock_monitor_mode

[Processing content] Sets the operation mode of the clock monitor via the CLM register, by forcibly terminating DMA transfer.

[SFRs used]
- DCHC0.TC0 DMA0 transfer status bit
- DCHC0.E00: 1 (Enables DMA0 transfer.)
- DCHC0.INIT0: 1 (Forcibly terminates DMA0 transfer.)
- DCHC1.TC1 DMA1 transfer status bit
- DCHC1.E11: 1 (Enables DMA1 transfer.)
- DCHC1.INIT1: 1 (Forcibly terminates DMA1 transfer.)
- DCHC2.TC2 DMA2 transfer status bit
- DCHC2.E22: 1 (Enables DMA2 transfer.)
- DCHC2.INIT2: 1 (Forcibly terminates DMA2 transfer.)
- DCHC3.TC3 DMA3 transfer status bit
- DCHC3.E33: 1 (Enables DMA3 transfer.)
- DCHC3.INIT3: 1 (Forcibly terminates DMA3 transfer.)
- PRCMD: 0x01 (Writes to command register (used when writing to a special register.).)
- CLM: 0x01 (Sets to operation enable.)

[call function] None

[Variable] None

[File name] clock_generator2.c

[Cautions]
- DMA transfer is forcibly terminated in this sample program, because all DMA transfers must be terminated before performing data setting to the special register.
- The CLM register is a special register and can therefore only be written in a combination of specific sequences.
Clock generator
Clock monitor mode (1/2)

1. DI
   - Disables maskable interrupt request

2. clock_monitor_mode
   - Clock monitor mode setting
3. PRERR $\equiv$ 1
   - Checks protection error flag
   - Yes
   - No
4. ret
Clock monitor mode setting

clock_monitor_mode

TC0 == 0 && E00 == 1

No

Checks DMA0 transfer

Yes

INIT0 = 1

Forcibly terminates DMA0

TC1 == 0 && E11 == 1

No

Checks DMA1 transfer

Yes

INIT1 = 1

Forcibly terminates DMA1

TC2 == 0 && E22 == 1

No

Checks DMA2 transfer

Yes

INIT2 = 1

Forcibly terminates DMA2

TC3 == 0 && E33 == 1

No

Checks DMA3 transfer

Yes

INIT3 = 1

Forcibly terminates DMA3

PRCMD = 0x01

Writes to command register

CLM = 0x01

Enables clock monitor operation

NOP instruction \times 5

Inserts five NOP instructions

ret
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