Application Note

32

CAN Configuration with PLL

V850E2/Fx4

32-bit Microcontroller

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   – The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at power-on

   The state of the product is undefined at the moment when power is supplied.

   – The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited.

   – The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   – When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   – The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Table of Contents

Chapter 1 Methods to define the CAN Jitter

Currently, two different methods are known how to define a maximum allowed jitter of a CAN protocol engine (transfer layer). Both methods have different targets and calculations.

While the “protocol oriented” method defines a maximum jitter, which is below a resynchronisation threshold in worst case, the “OEM” method is related to a single bit timing directly.

1.1 The protocol oriented jitter definition

Definition The jitter must be less than 1 time quanta (*TQ*) within 10 bits of the given baud rate of the CAN bus.
Thus, the *reference time interval* is 10 CAN bus bits.

Note 10 bits are corresponding with the maximum distance between subsequent resynchronisation phases within a CAN frame. The *time quanta* is the elementary resolution of the CAN bus protocol. If the jitter is below 1 TQ, any participant on the CAN bus will not see the jitter at all, because no resynchronisation takes place, which would have been caused by the jitter. In worst case, a bit consists of 25 TQ, which is TQ_{max}.

Values for this calculation must be taken with peak-to-peak values, because in worst case the jitter may accumulate in the same direction along with the whole time of 10 bits.

1.2 The OEM jitter definition

Definition The jitter must be less than x_{OEM}% of the length one CAN bus bit.
Thus, the *reference time interval* is one CAN bus bit.

This method is easily verifyable, which is its main advantage. On the other hand, this method typically defines the limit in such a way, that it is harder to fulfill. In addition, the method is not related to the CAN protocol itself, so that a violation of this limit does not have a consequent impact on the CAN bus function.

Values for this calculation must be taken with peak-to-peak values, because in worst case the jitter may accumulate in the same direction along with the whole time of one bit.

Chapter 2 Maximum Deviation for V850E2/Fx4

2.1 Involved parts

To calculate a worst case deviation of a node on the CAN bus, the following values have to be added:

- the jitter peak-to-peak values of the oscillator during the *reference time interval*.
- the jitter peak-to-peak values of the (optionally) used PLL during the *reference time interval.*
- the aging, voltage and temperature effects on clock deviation for quartz and oscillator.

2.2 Properties of V850E2/Fx4[1]

- Oscillator deviation: 0 ppm $= d_{OSC}$
  No voltage depencency,
  No temperature dependency,
  No aging dependency.
- Oscillator jitter: 0 (no jitter) $= j_{OSC}$
- PLL jitter: 1.275 ns / µs $= j_{PLL}$

2.3 Properties of the quartz[2]

- Initial tolerance: 50 ppm $= d_{QI}$
- Temperature dependency: 150 ppm $= d_{QT}$
- Aging deviation: 100 ppm $= d_{QA}$

1) According to data sheet
2) Typical example values

2.4 Calculation results

For both jitter definition cases, the peak-to-peak worst case is considered by a multiplication factor of 2 for the V850E2/Fx4 deviation.

2.4.1 Protocol oriented jitter at baud rate *b* = 500 kbit/s

The maximum *allowed* deviation caused by deviations and jitter is:

$1 / b / TQ_{max}$ =

1 / (500 kbit/s) / (25 / bit) = **80 ns**

The deviation of V850E2/Fx4 including the quartz is:

$2 * ((d_{QI} + d_{QT} + d_{QA} + d_{OSC}) / b + ((j_{PLL} + j_{OSC}) * 10 / b))$ =

2 * ((300 ppm) / 500 kbit/s + ((1.275 ns / µs) * 10 / 500 kbit/s)) = **25.5 ns**

Conclusion **The deviation of V850E2/Fx4including quartz is within the limit.**

2.4.2 OEM jitter 0.4% at baud rate *b* = 500 kbit/s

Note The limit of 0.4% applies for the baud rate of 500 kbit/s, if the bit resolution is equal or higher than 10 TQ/bit.

The maximum *allowed* deviation caused by deviations and jitter is:

$1 / b * x_{OEM}\%$ =

1 / (500 kbit/s) * 0.4% = **8 ns**

The deviation of V850E2/Fx4 including the quartz is:

$2 * ((d_{QI} + d_{QT} + d_{QA} + d_{OSC}) / b + ((j_{PLL} + j_{OSC}) / b))$ =

2 * ((300 ppm) / 500 kbit/s + ((1.275 ns / µs) / 500 kbit/s)) = **6.3 ns**

Conclusion **The deviation of V850E2/Fx4including quartz is within the limit.**

Chapter 3 Final Conclusion

The clock deviation of V850E2/Fx4 does not exceed the limits for CAN usage, even if the PLL is used as a clock source for the CAN controller. This deviation includes tolerances of the oscillator, an external quartz (with assumed 300 ppm in total), voltage and temperature drift within the allowed operating range, aging, and the jitter of oscillator and PLL in worst case.

For this reason the usage of the V850E2/Fx4 PLL as a clock source for the CAN controller is allowed.

Regarding the OEM jitter definition criteria, the current definition values have to be considered. In this document, a baud rate of 500 kbit/s and a bit resolution of at least 10 TQ/bit has been assumed to be checked with an actual OEM requirements definition.

Revision History

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