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H8/300H Tiny Series

Using Timer Z Input Capture Function to Count Pulse Cycles

Introduction

Timer Z input capture function is used to measure the period of the pulse input through the input-capture pin (FTIOA0).

Target Device

H8/3687

Contents

1. Specifications

1. As shown in figure 1.1, the timer input capture function is used to measure the period of the pulse input from the input-capture pin A0 (FTIOA0).
2. Timer counter 0 (TCNT0) counts the clock cycles between rising edges of the pulse, and the result is stored in RAM. The period of the pulse is thus measured in terms of this counter value in RAM.
3. The maximum period that can be measured is 32.768 ms with the accuracy of ±0.5 µs.

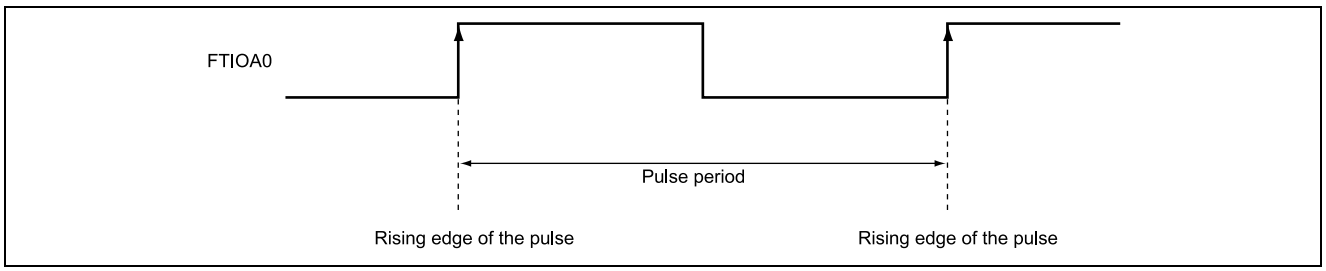


Figure 1.1 Input Pulse Period Measurement

2. Description of Functions

1. In this sample task, timer Z input capture function is used to measure the period of a pulse input from the input-capture pin A0 (FTIOA0). Figure 2.1 is a block diagram of timer Z input capture function. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ. PSS is incremented every cycle.
- Timer control register 0 (TCR0) selects TCNT0 input clock and method of clearing TCNT0. In this sample task, the TCNT0 input clock is specified as ϕ/8, the TCNT0 counts the rising edge of the clock, and the TCNT0 is cleared by the compare-match/input-capture with GRA0.
- Timer I/O control register A0 (TIORA0) controls GRA0 and GRB0. In this sample task, GRA0 is used as an input-capture register and the TCNT0 value is transferred to GRA0 at the rising edge on the FTIOA0 pin.
- Timer status register 0 (TSR0) indicates the timer Z status. In this sample task, the overflow flag (OVF) is set to 1 when the GRA0 overflows and the input-capture/compare-match flag A (IMFA) is set to 1 when a GRA0 input capture occurs.
- Timer interrupt enable register 0 (TIER0) enables or disables various interrupt requests. In this sample task, interrupt requests by the OVF and IMFA flags of TSR0 are enabled and other interrupt requests are disabled.
- Timer counter 0 (TCNT0) is a 16-bit readable/writable upward counter that is incremented by an internal clock or external clock input. In this sample task, TCNT0 is incremented on the rising edge of ϕ/8.
- General register A0 (GRA0) a 16-bit readable/writable register. In this sample task, GRA0 is used as an input-capture register to which the TCNT0 value is transferred at the rising edge on the FTIOA0 pin.
- Timer start register (TSTR) starts or stops the TCNT0 and TCNT1 operation. In this sample task, TCNT0 is specified to start counting and TCNT1 is specified to stop counting.
- Timer mode register (TMDR) selects synchronous or independent operation of TCNT0 and TCNT1. In this sample task, TCNT0 operates independently of TCNT1.
- Timer function control register (TFCR) specifies operation modes and selects an output level. In this sample task, channels 0 and 1 are specified for normal operation.
- Input-capture/output-compare A0 pin (FTIOA0) is set to be an input-capture pin. The value of TCNT0 is transferred to GRA0 at the rising edge on this pin.

Period of an input pulse
= (TCNT0 value stored in prdhl) × (period of TCNT0 input clock)
= (TCNT0 value stored in prdhl) × (1/ (ϕ/PSS))
= (TCNT0 value stored in prdhl) × (1/ (16 MHz/8))
= (TCNT0 value stored in prdhl) × 0.5 µs

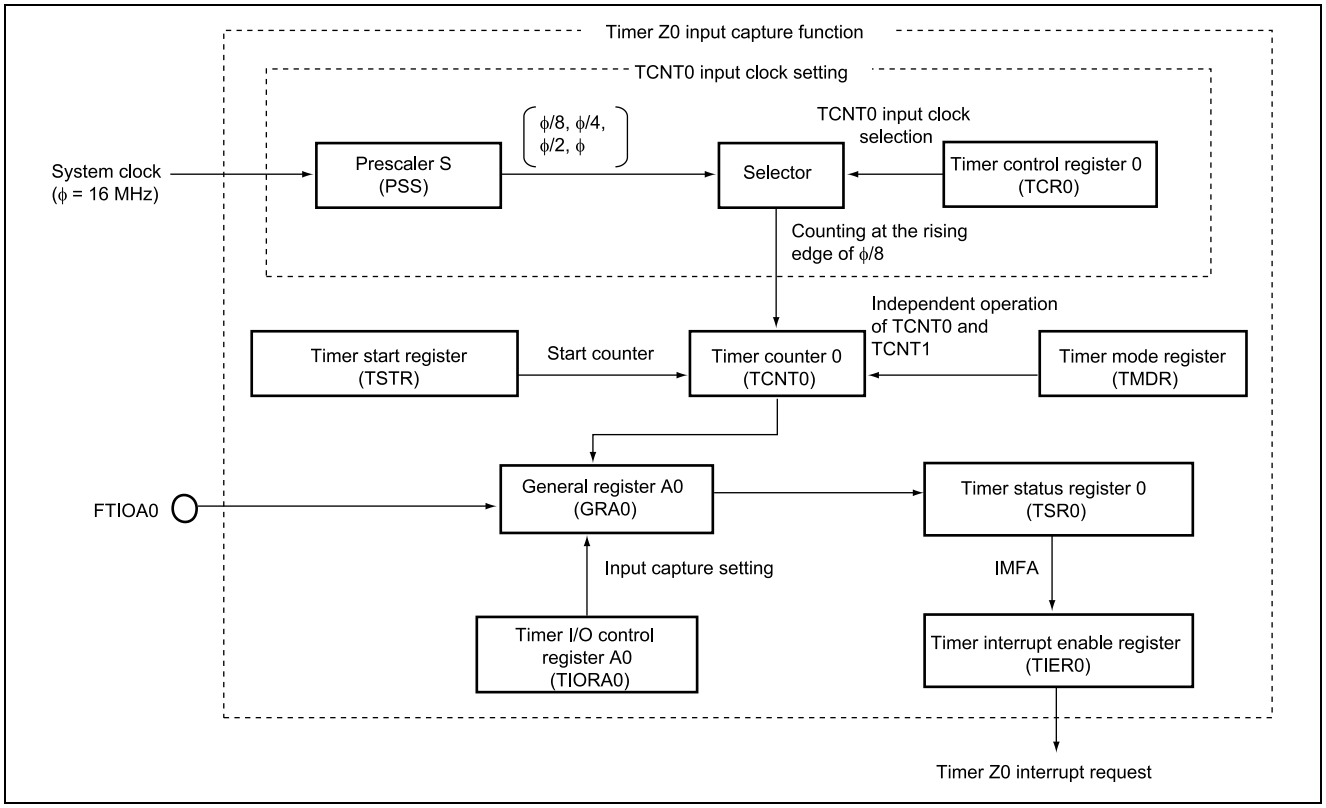


Figure 2.1 Block Diagram of Timer Z0

2. Table 2.1 lists the function allocation for this sample task. The functions listed in this table are allocated so as to implement pulse period measurement.

Table 2.1 Function Allocation

Function	Description
PSS	13-bit counter with system clock input
TCR0	Specifies the TCNT0 input clock.
TIORA0	Specifies GRA0 as an input-capture register.
TSR0	Flag control by GRA0 input capture and TCNT0 overflow
TIER0	Enables GRA0 input capture and TCNT0 overflow interrupt requests.
TCNT0	16-bit counter that is incremented at the rising edge of ϕ/8.
GRA0	TCNT0 value is transferred to this register at the rising edge on the FTIOA0 pin.
TSTR	Controls TCNT0 count start and stop.
TMDR	Selects independent operation of TCNT0 and TCNT1.
TFCR	Sets channels 0 and 1 in normal operation mode.

3. Description of Operation

Operation of this sample task is described in figure 3.1. Hardware and software processing are applied in the way shown in figure 3.1 to measure the pulse period.

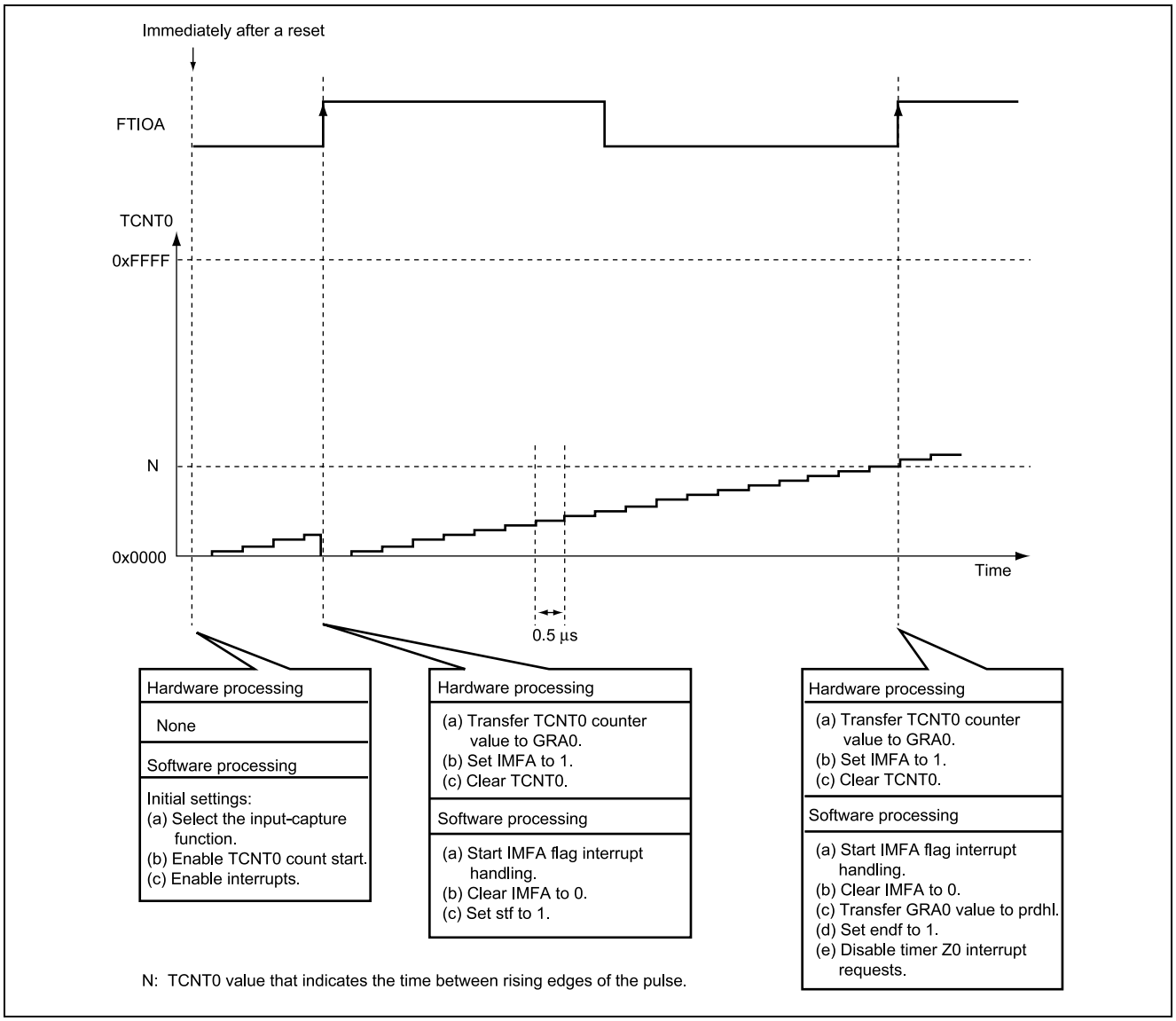


Figure 3.1 Principle of Operation

4. Description of Software

4.1 Modules

Table 4.1 lists the modules used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Selects timer Z0 input capture function, starts counting by TCNT0, and provides settings for interrupts.
Period measurement end	tz0int	Performs timer Z0 interrupt handling. Stores period measurement result to RAM. Clears the OVF and IMFA flags.

4.2 Arguments

This sample task uses no arguments.

4.3 Internal Registers

The internal registers used in this sample task are described below.

- TCR0 Timer control register 0 Address: 0xF700

Bit	Bit Name	Setting	Function
7	CCLR2	CCLR2 = 0	Counter clear 2 to 0
6	CCLR1	CCLR1 = 0	CCLR2 = 0, CCLR1 = 0, CCLR0 = 1:
5	CCLR0	CCLR0 = 1	Clears the TCNT0 on compare-match/input-capture with GRA0.
4	CKEG1	CKEG1 = 0	Clock edge 1 to 0
3	CKEG0	CKEG0 = 0	CKEG1 = 0, CKEG0 = 0: Counts at the rising edge of the clock.
2	TPSC2	TPSC2 = 0	Timer prescaler 2 to 0
1	TPSC1	TPSC1 = 1	TPSC2 = 0, TPSC1 = 0, TPSC0 = 1: Counts by ϕ/8
0	TPSC0	TPSC0 = 1	

- TIORA0 Timer I/O control register A0 Address: 0xF701

Bit	Bit Name	Setting	Function
2	IOA2	IOA2 = 1	I/O control A2 to A0
1	IOA1	IOA1 = 0	IOA2 = 1, IOA1 = 0, IOA0 = 0:
0	IOA0	IOA0 = 0	Specifies the GRA as an input-capture register and transfers TCNT0 value to the GRA0 at the rising edge on the FTIOA0 pin

- TSR0 Timer status register 0 Address: 0xF703

Bit	Bit Name	Setting	Function
4	OVF	0	Overflow flag OVF = 0: Indicates that TCNT0 overflow has not occurred. OVF = 1: Indicates that TCNT0 overflow has occurred.
0	IMFA	0	Input-capture/compare-match flag A Indicates whether or not the TCNT0 value has been transferred to the GRA0 by the input capture signal when the GRA is operating as an input-capture register. IMFA = 0: Indicates that the TCNT0 value has not been transferred to GRA0. IMFA = 1: Indicates that the TCNT0 value has been transferred to GRA0.

- TIER0 Timer interrupt enable register 0 Address: 0xF704

Bit	Bit Name	Setting	Function
7	OVIE	1	Timer overflow interrupt enable OVIE = 0: Disables interrupts by the OVF and UDF flags of TSR0. OVIE = 1: Enables interrupts by the OVF and UDF flag of TSR0.
0	IMIEA	1	Input-capture/compare-match interrupt enable A IMIEA = 0: Disables interrupts by the IMFA flag of TSR0. IMIEA = 1: Enables interrupts by the IMFA flag of TSR0.

- TCNT0 Timer counter 0 Address: 0xF706
  Function: A 16-bit up-counter that is incremented at the rising edge of $\phi/8$.
  Setting: 0x0000

- GRA0 General register A0 Address: 0xF708
  Function: In input-capture operation, the TCNT0 value is transferred to the GRA0 at the rising edge on the FTIOA0 pin.
  Setting: —

- TSTR Timer start register Address: 0xF720

Bit	Bit Name	Setting	Function
0	STR0	0	Channel 0 counter start STR0 = 0: Stops counting by TCNT0. STR0 = 1: Starts counting by TCNT0.

- TMDR Timer mode register Address: 0xF721

Bit	Bit Name	Setting	Function
0	SYNC	0	Timer synchronization SYNC = 0: TCNT0 operates independently of TCNT1. SYNC = 1: TCNT0 operates synchronously with TCNT1.

- TFCR Timer function control register Address: 0xF723

Bit	Bit Name	Setting	Function
1	CMD1	CMD1 = 0	Combination mode 1 and 0
0	CMD0	CMD0 = 0	CMD1 = 0, CMDk0 = 0: Channels 0 and 1 operates in normal operation mode.

4.4 Description of RAM

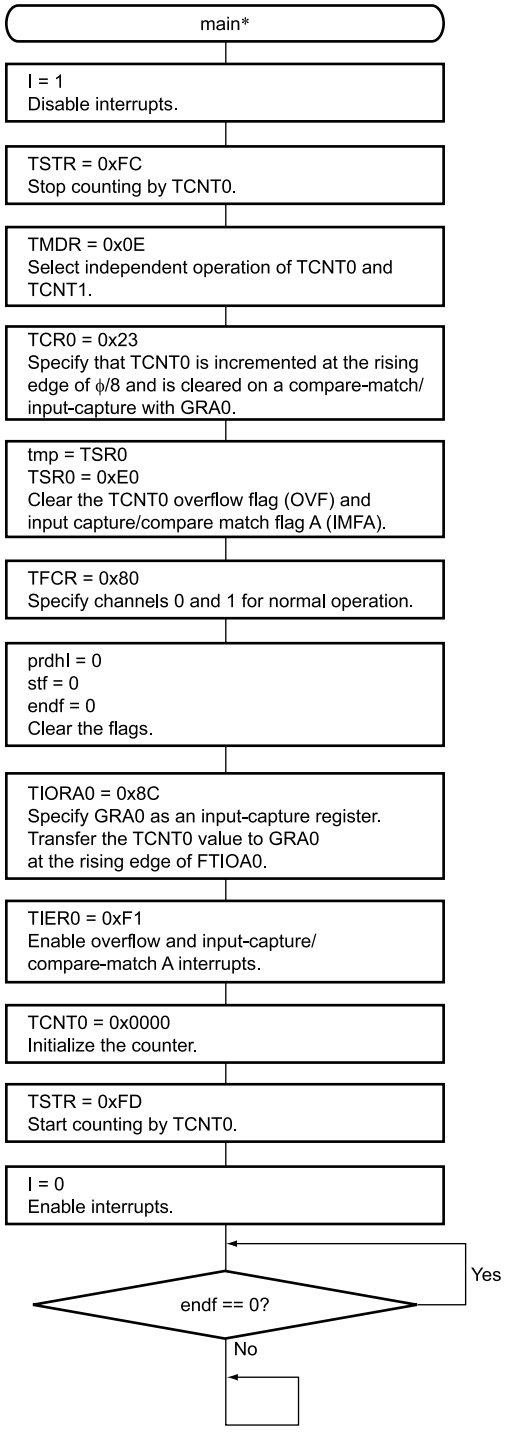
Table 4.2 describes the RAM used in this sample task.

Table 4.2 Description of RAM

Label Name	Function	Size	Used in
prdhl	Pulse period measurement result	2 bytes	Main routine Period measurement end
stf	A flag indicating whether the 2nd timer Z0 interrupt has occurred.	1 byte	Main routine Period measurement end
endf	A flag indicating whether the period measurement has been completed.	1 byte	Main routine Period measurement end

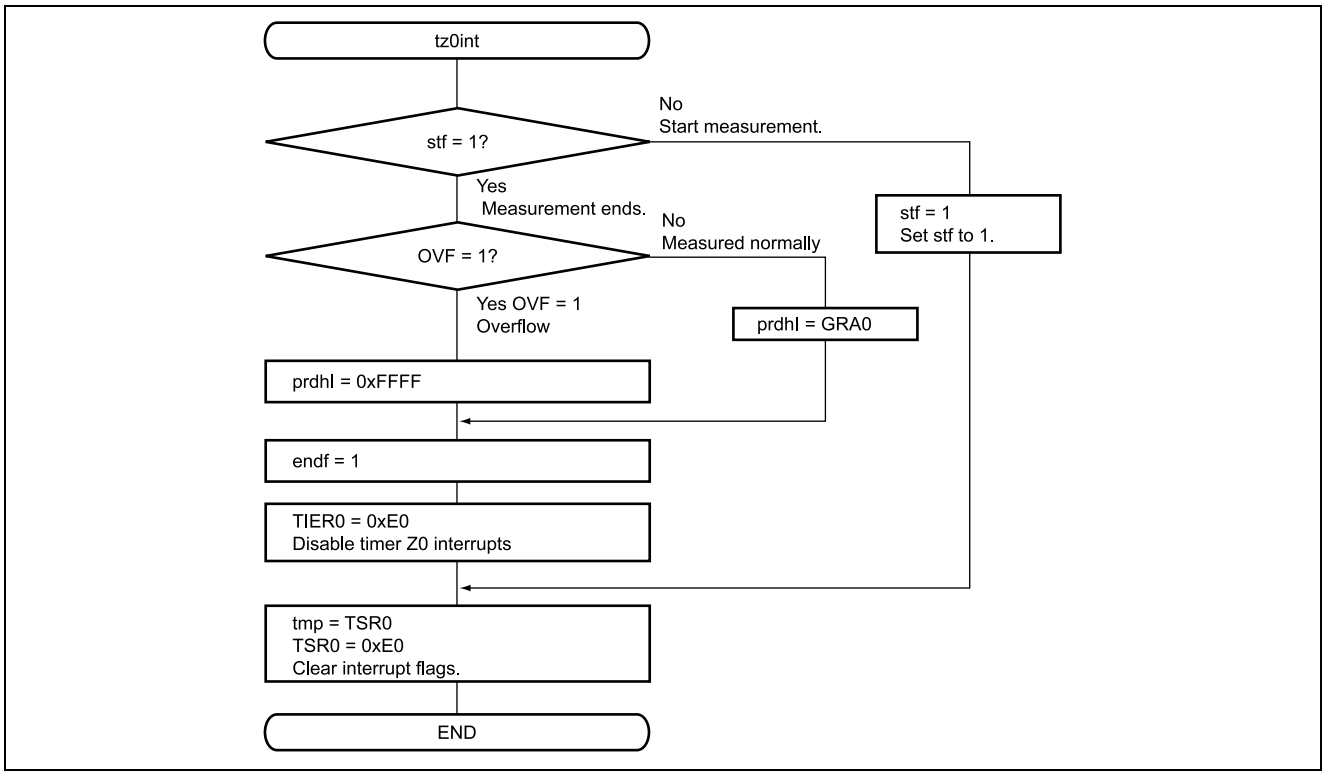
5. Flowcharts

1. Main routine



Note: * The stack pointer is specified by INIT.SRC (assembly language).

2. Period measurement end



6. Program List

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3687-                                                                                          */
/*   Application Note                                                                                                   */
/*                                                                                                                      */
/*   'Pulse Period Measurement by Input Caputure Function'                                                              */
/*                                                                                                                      */
/*   Function                                                                                                           */
/*   : Timer Z Input Caputure                                                                                           */
/*                                                                                                                      */
/*   External Clock :    16MHz                                                                                          */
/*   Internal Clock :    16MHz                                                                                          */
/*   Sub Clock :         32.768kHz                                                                                      */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;         /* bit7 */
     unsigned char   b6:1;         /* bit6 */
     unsigned char   b5:1;         /* bit5 */
     unsigned char   b4:1;         /* bit4 */
     unsigned char   b3:1;         /* bit3 */
     unsigned char   b2:1;         /* bit2 */
     unsigned char   b1:1;         /* bit1 */
     unsigned char   b0:1;         /* bit0 */
};

#define        TCR0           *(volatile unsigned char *)0xF700                /* Timer control register_0               */
#define        TIORA0         *(volatile unsigned char *)0xF701                /* Timer I/O Control Register A_0         */
#define        TSR0           *(volatile unsigned char *)0xF703                /* Timer status register_0                */
#define        TSR0_BIT       (*(struct BIT *)0xF703)                          /* Timer status register_0                */
#define        OVF            TSR0_BIT.b4                                      /* Over flow flag                         */
#define        IMFB           TSR0_BIT.b1                                      /* Input Capture/Compare Match FlagB      */
#define        IMFA           TSR0_BIT.b0                                      /* Input Capture/Compare Match FlagA      */
#define        TIER0          *(volatile unsigned char *)0xF704                /* Timer interrupt enable register0       */
#define        TIER0_BIT      (*(struct BIT *)0xF704)                          /* Timer interrupt enable register0       */
#define        IMIEA          TIER0_BIT.b0                                     /* Input Capture/Compare Match            */
                                                                               /* Interrupt Enable A                     */
#define        TCNT0          *(volatile unsigned short *)0xF706               /* Timer counter_0                        */
#define        GRA0           *(volatile unsigned short *)0xF708               /* General register A_0                   */
#define        GRB0           *(volatile unsigned short *)0xF70A               /* General register B_0                   */
#define        TSTR           *(volatile unsigned char *)0xF720                /* Timer start register                   */
#define        TMDR           *(volatile unsigned char *)0xF721                /* Timer mode register                    */
#define        TPMR           *(volatile unsigned char *)0xF722                /* Timer PWM mode register                */
#define        TFCR           *(volatile unsigned char *)0xF723                /* Timer function control register        */
#define        TOER           *(volatile unsigned char *)0xF724                /* Timer output master enable register    */
#define        TOCR           *(volatile unsigned char *)0xF725                /* Timer output control register          */

#pragma interrupt   (tz0int)
```

```
/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void );                                          /* SP Set                                           */
void main ( void );
void tz0int ( void );

/************************************************************************************************************************/
/*   RAM define                                                                                                         */
/************************************************************************************************************************/
volatile unsigned char  stf;                                        /* Start Flag                                       */
volatile unsigned char  endf;                                       /* End Flag                                         */
volatile unsigned short prdhl;                                      /* Pulse Period                                     */

/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                              /* VECTOR SECTOIN SET                               */
void (*const VEC_TBL1[])(void) = {                                  /* 0x00 - 0x0f                                      */
     INIT                                                           /* 00 Reset                                         */
};
#pragma section     V2                                              /* VECTOR SECTOIN SET                               */
void (*const VEC_TBL2[])(void) = {
     tz0int                                                         /* 34 Timer Z0 Interrupt                            */
};

#pragma section                                                     /* P                                                */

/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     unsigned char tmp;

     set_imask_ccr(1);                                              /* Interrupt Disable                                */

     TSTR = 0xFC;                                                   /* TCNT0 count stop                                 */
     TMDR = 0x0E;                                                   /* TCNT0,TCNT1 Single Mode                          */
     TCR0 = 0x23;                                                   /* Rising edge, phi/8 Clock count                   */
     tmp = TSR0;
     TSR0 = 0xE0;                                                   /* Interrupt Flag Clear                             */
     TFCR = 0x80;                                                   /* Channel 0,1 operate normally                     */

     prdhl = 0;
     stf = 0;
     endf = 0;
     TIORA0 = 0x8C;                                                 /* Input capture to GRA                             */
                                                                    /* at the rising edge                               */
     TIER0 = 0xF1;                                                  /* OVF,IMFA Interrupt Enable                        */
     TCNT0 = 0x0000;                                                /* Clear TCNT0                                      */
     TSTR = 0xFD;                                                   /* TCNT0 count start                                */

     set_imask_ccr(0);                                              /* Interrupt Enable                                 */

     while(endf == 0);

     while(1);
}
```

```
/************************************************************************************************************************/
/*   Timer Z0 Interrupt                                                                                                 */
/************************************************************************************************************************/
void tz0int ( void )
{
     unsigned char tmp;

     if(stf == 1){                                                    /* Interrupt by IMFA flag                 */
          if(OVF == 1)
               prdhl = 0xFFFF;
          else
               prdhl = GRA0;                                        /* Set Pulse Period                       */

          endf = 1;                                                 /* Set end flag                           */
          TIER0 = 0xE0;                                             /* OVF,IMFA Interrupt Disable             */
     }
     else{
          stf = 1;                                                  /* Set start flag                         */
     }

     tmp = TSR0;
     TSR0 = 0xE0;                                                   /* Interrupt Flag Clear                   */
}
```

Link address specifications

Section Name	Address
CV1	0x0000
CV2	0x0034
P	0x0100
B	0xFB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.29.03	—	First edition issued

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