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H8S/20103, H8S/20203, and H8S/20223 Groups

Using Timer RG and Port Output for Timing Pattern Controller Operation

Introduction

The event link controller (ELC) is used to set up the compare match A signal from the timer RG module in products of the H8S/20103, H8S/20203, and H8S/20223 Groups such that operation as a programmable timing pattern controller (TPC) is realized through port event-input and port event-generation without CPU intervention.

Target Devices

H8S/20103 (R4F20103)

H8S/20203 (R4F20203)

H8S/20223 (R4F20223)

Frequency Used in Confirming Operation

System clock $\phi = \phi osc = 20$ MHz

Contents

1. Specifications

Specifications of this sample task are as given below. The compare match A signal from timer RG provides the time base for the output of pulses as desired without CPU intervention.

Figure 1 gives a schematic view of how the event controller sets up timer RG and output port pins for timing pattern controller operation and figure 2 shows the port output in timing pattern controller operation.

1. A table containing values for the timing of pulse output with respect to compare match A of timer RG as the time base is placed in ROM.
2. Settings are made so that timer RG is placed in timer mode, and TRGCNT counts clock source ϕ and is cleared on a compare match with GRA.
3. GRA is specified as a compare match register.
4. The period of timer RG is set in GRA (setting to control timing of pulse output).
5. TRGCNT is cleared to H'0000.
6. Settings are made to place the DTC in repeat mode with incrementation of transfer source addresses, a fixed transfer destination address, a repeated area on the source side, and “byte” as the unit of data transfer.
7. The source address for data transfer is specified as the first address of the pulse output pattern table that has been placed in ROM.
8. The destination address for data transfer is specified as the address of PDBF1.
9. The compare match A interrupt from timer RG is set as the activation source for the DTC.
10. PDR30 to PDR34 are set to "H" and the output direction is selected for pins P30 to P34.
11. Pins P30 to P34 are specified for use as output port group 1.
12. Initial value B'10000 to be transferred to PDR30 to PDR34 on event input is set in PDBF10 to PDBF14.
13. Settings are made so that the value from the buffer is output on port group 1 when the event signal is input.
14. For event operation of output port group 1, the compare match A signal from timer RG is specified as the event signal.
15. Event linkage is enabled.
16. The compare match A interrupt signal from timer RG is enabled.
17. Timer RG is activated.
18. Every time the compare match signal for a match between the counter of timer RG and GRA is generated, pulse output patterns are output from P30 to P34 without CPU intervention.

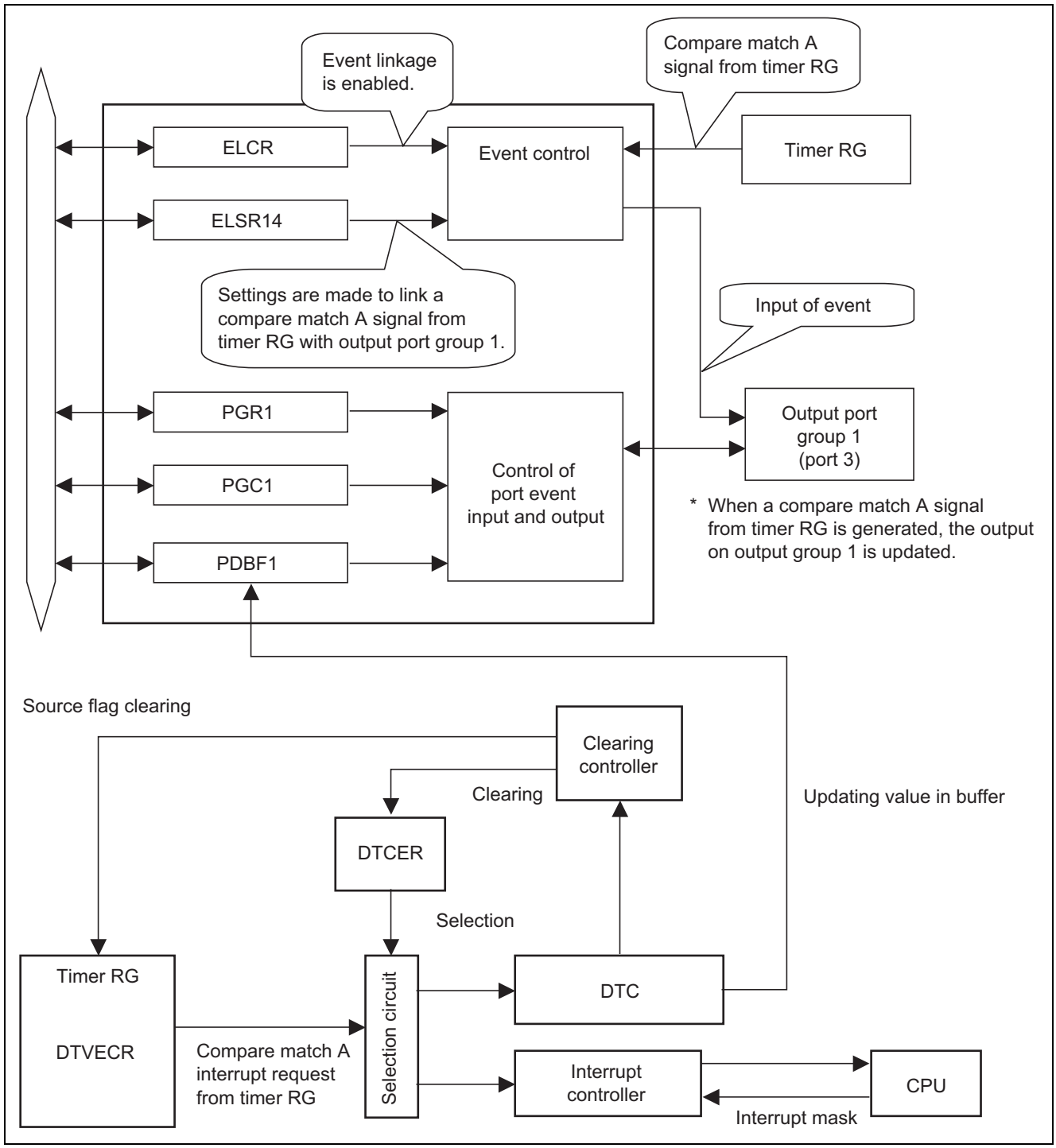


Figure 1 Schematic View of How Timer RG and Port Group Output are Used to Set up TPC Operation

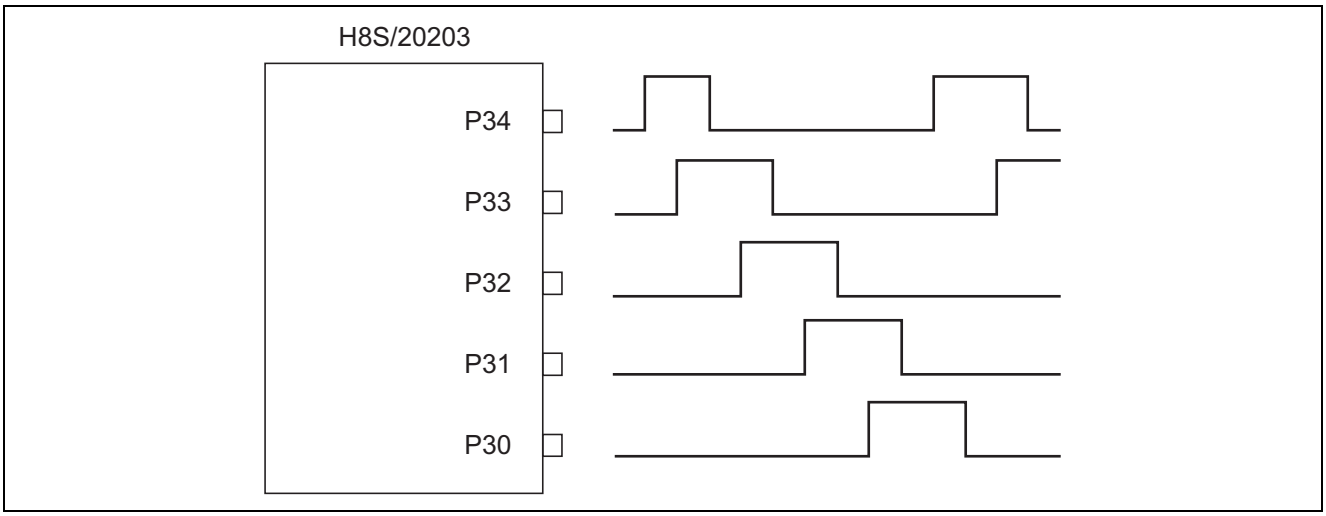


Figure 2 Port Group Output in Timing Pattern Controller Operation

2. Description of Modules Used

2.1 Event Link Controller (ELC)

The features of the ELC are described below. Figure 3 is a block diagram of the ELC.

The ELC connects events generated by the various peripheral modules to other modules. This function allows direct cooperation between modules, without CPU intervention.

- Fifty-nine event signals can be directly connected to modules.
- The operation of timer modules can be selected when an event is input to the timer module.
- Events can be connected to ports 3 and 6.
- Settings for ports enable the generation of events in the form of signals on port pins.
- A single bit or any grouping of several bits can be set up for event connection on the ports used for connecting events.
- The event generation timer can be used to set up the generation of signals on four channels as events with the desired intervals.

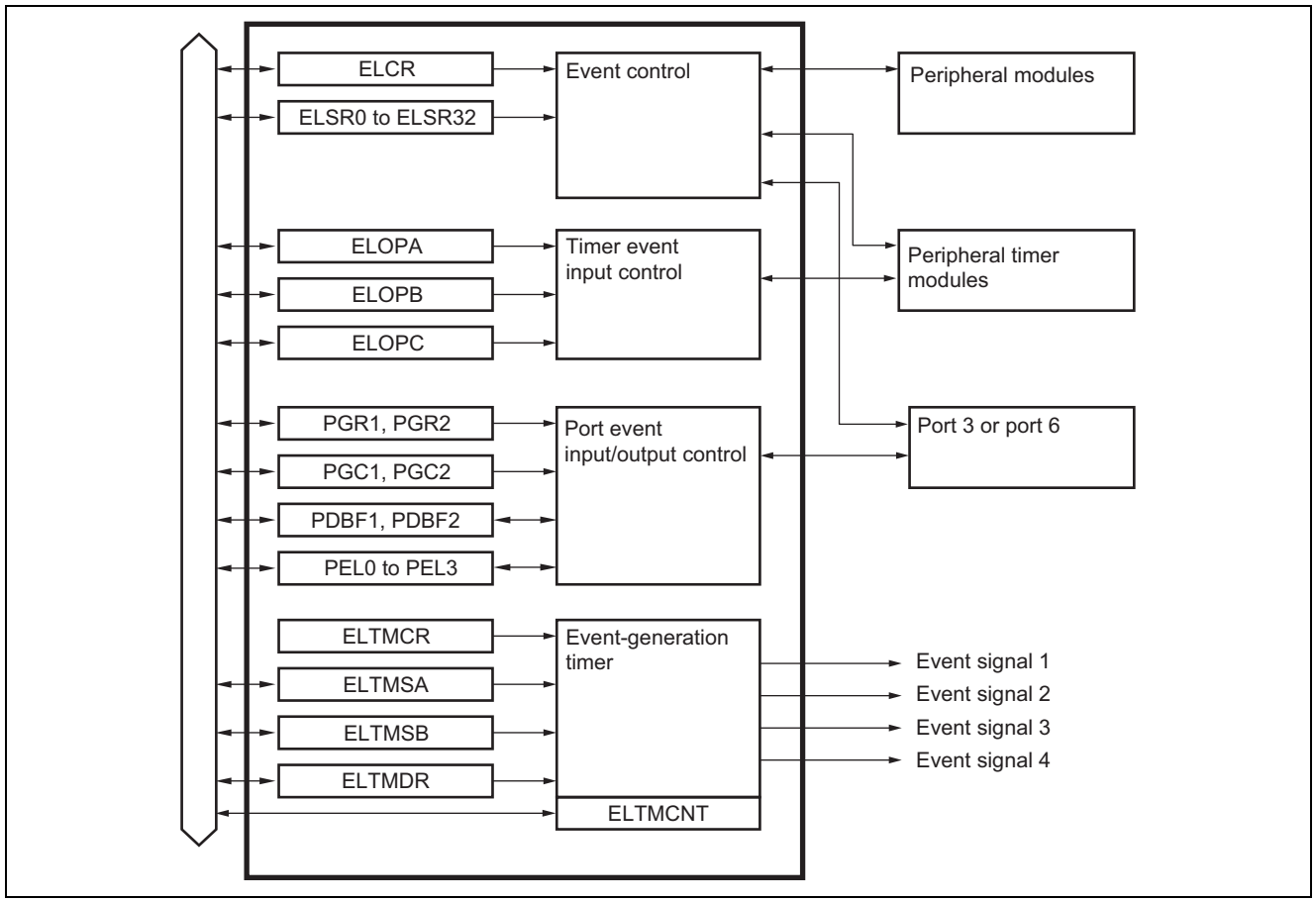


Figure 3 Block Diagram of Event Link Controller

2.1.1 Operation of Peripheral Timer Modules at the Time of Event Input

Timer modules may perform any of three operations in response to the input of a signal indicating an event (event signal below). The operation depends on the ELOP settings.

1. Starting the timer counter
   When the event signal is input, the count start bit* in the given timer control register is set to 1 to make the timer start counting. Input of the event signal while the count start bit is 1 is ineffective.
2. Counting events
   The event signal is selected as the clock source for the timer so that the timer counts the events.
3. Input capture
   Input of the event signal makes the timer perform input-capture operation.

Note: * See the descriptions of the bits in the relevant sections on timers.

2.2 Timer RG

Timer RG is a 16-bit timer with output compare and input capture functions. Among other functions of this multifunctional timer for use in various applications, timer RG is capable of counting cycles of an external clock signal and producing output pulses with desired duty cycles by using compare-match signals produced by matches between the timer counter and the values in two general registers. Figure 4 is a block diagram of timer RG.

- Selection from among seven counter clock sources
  Internal clocks:ϕ, ϕ/2, ϕ/4, ϕ/8, ϕ/32 and ϕ/40
  External clocks: TCLKA, TCLKB
- Timer mode
  Waveform output by compare match (Selection of 0 output, 1 output, or toggled output)
  Input capture function (Rising edge, falling edge, or both edges)
- PWM mode
  Generates pulses with a desired period and duty cycle.
- Phase counting mode
  Detects phase difference between two external clock inputs and increments/decrements the TCNT.
- Fast access via internal 16-bit bus
  Performs high-speed accesses to the timer counter and general registers using the 16-bit bus interface.
- Four interrupt sources
  TRGCNT overflow, TRGCNT underflow, compare match, and input capture

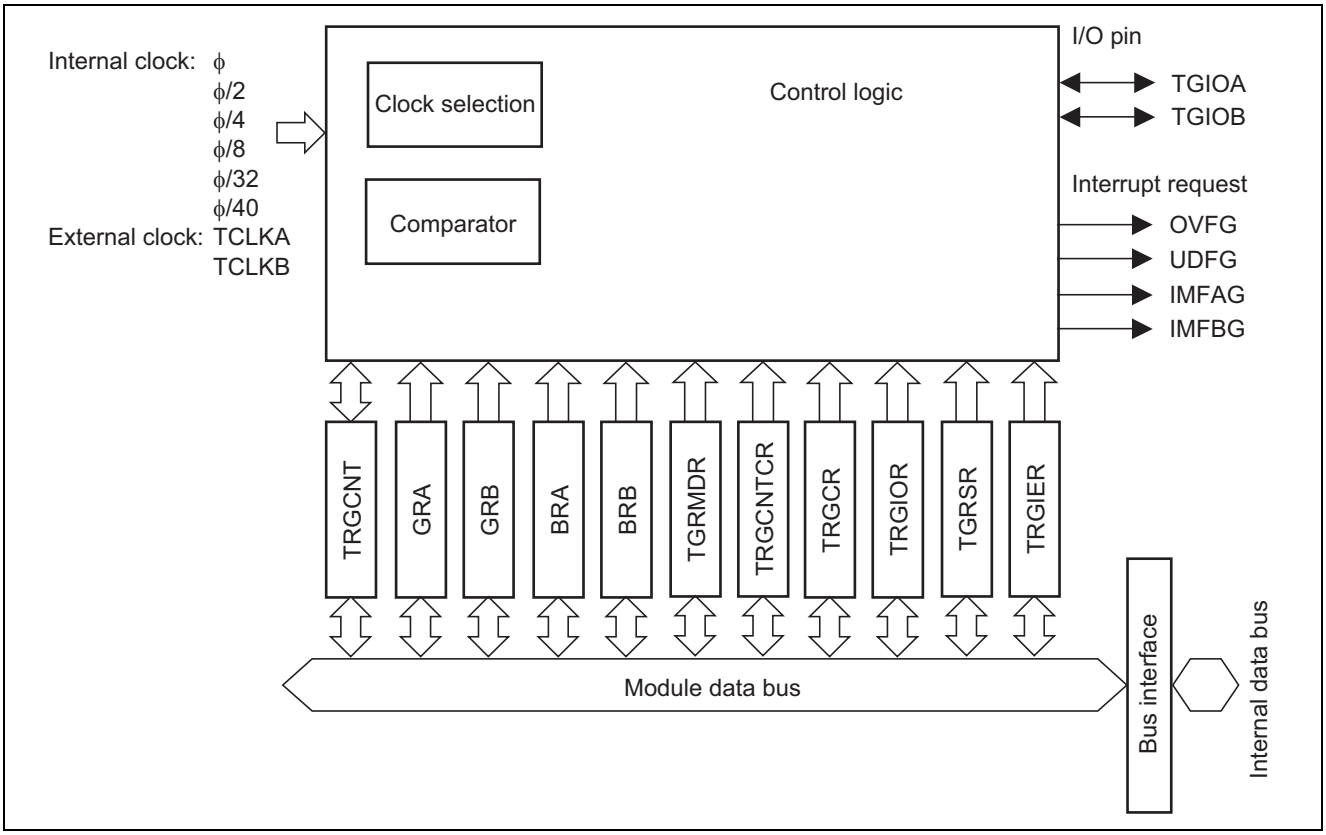


Figure 4 Block Diagram of Timer RG

2.2.1 Operation Controlled by Event Links

Using the event link controller (ELC), timer RG can be made to operate in the following ways in relation to events occurring in other modules.

1. Staring counter operation
   The start of counting operations by timer RG can be selected by ELOPC of the ELC. When the event specified by ELSR8 occurs, the STR bit in TRGMDR is set to 1, which starts counting by timer RG. However, if the specified event occurs when the STR bit has already been set to 1, the event is not effective.

2. Counting event
   The counting of events by timer RG can be selected by ELOPC of the ELC. When the event specified in ELSR8 occurs, event counter operation proceeds with that event as the source to drive counting, regardless of the setting of TPSC[2:0] bits in TRGCR. When the value of the counter is read, the value read out is the actual number of input events.

3. Input capture
   Input capture operation of timer RG can be selected by ELOPC of the ELC. When the event specified in ELSR8 occurs, GRB captures the value of TRGCNT. When input capture operation initiated by an event link is in use, set IOB[2:0] = B'101 in the TRGIOR register of timer RG, set the STR bit in TRGMDR to 1, and then start the counter. Since input on the TGIOB pin becomes valid at the same time, fix the input to the TGIOB pin or take other measures such as not allocating the TGIOB pin to the port in the PMC, etc.

2.3 Data Transfer Controller (DTC)

The features of the DTC are described below.

This LSI includes a data transfer controller (DTC). The DTC can be activated by an interrupt or software to transfer data.

Figure 5 is a block diagram of the DTC.

- Transfer possible over any number of channels
- Three transfer modes
  1. Normal mode
     One operation transfers one byte or one word of data.
     Memory address is incremented or decremented by 1 or 2.
     From 1 to 65,536 transfers can be specified.
  2. Repeat mode
     One operation transfers one byte or one word of data.
     Memory address is incremented or decremented by 1 or 2.
     Once the specified number of transfers (1 to 256) has ended, the initial state is restored, and transfer is repeated.
  3. Block transfer mode
     One operation transfers specified one block of data.
     The block size is 1 to 256 bytes or words.
     From 1 to 65,536 transfers can be specified.
     Either the transfer source or the transfer destination is designated as a block area.
- One activation source can trigger a number of data transfers (chained transfer)
- Direct specification of 16-Mbyte address space possible
- Activation by software is possible.
- Transfer can be set in byte or word units.
- A CPU interrupt can be requested for the interrupt that activated the DTC.
- Module standby mode can be set.

The DTC's register information is stored in the on-chip RAM. A 32-bit bus connects the DTC to the on-chip RAM, enabling 32-bit/1-state reading and writing of the DTC register information.

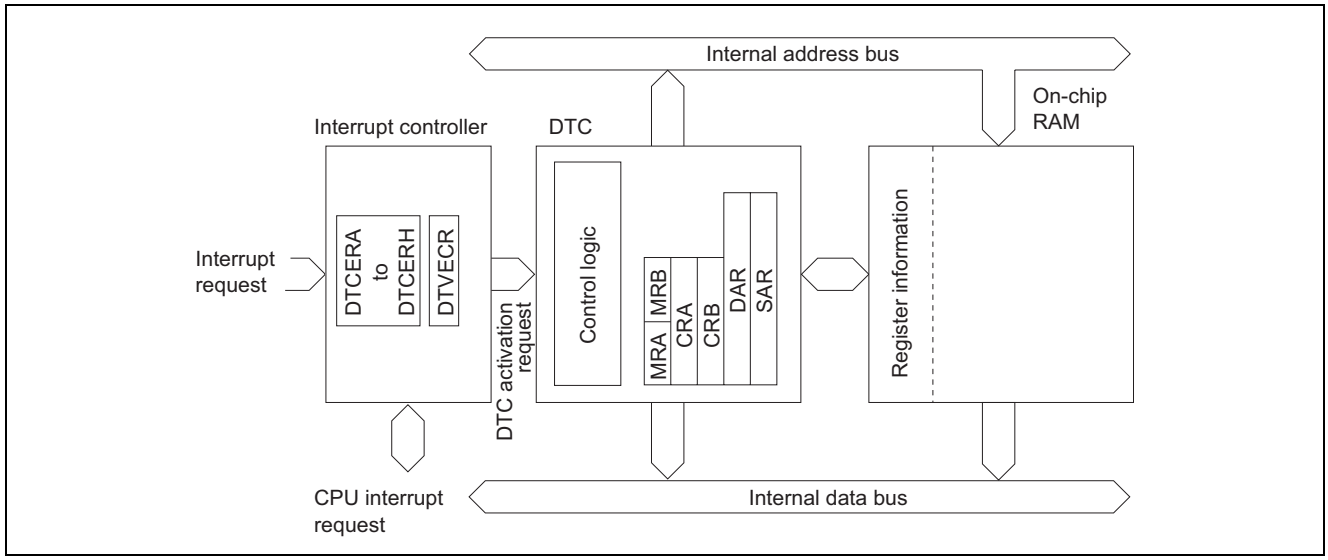


Figure 5 Block Diagram of DTC

2.3.1 Activation Sources

The DTC operates when activated by an interrupt request or by writing to DTVECR by software. An interrupt request can be designated by the DTCER bit. At the end of a data transfer (or the last consecutive transfer in the case of chained transfer), the activation source interrupt flag is the RDRF flag of SCI3_1.

When an interrupt has been designated a DTC activation source, existing CPU mask level and interrupt controller priorities have no effect. If there is more than one activation source at the same time, the DTC operates in accordance with the default priorities for the interrupt sources. Table 1 shows a relationship between activation sources and DTCER clear conditions. Figure 6 is a block diagram of DTC activation source control. For details, see the section on the interrupt controller of *H8S/20103, H8S/20203, H8S/20223 Group Hardware Manual* (REJ09B0465).

Table 1 Relationship between Activation Sources and DTCER Clearing

Activation Source	DISEL = 0 and Specified Number of Transfers Has Not Ended	DISEL = 1 or Specified Number of Transfers Has Ended
Activation by software	The SWDTE bit is cleared to 0.	• The SWDTE bit retains the value 1. • Interrupt request to the CPU
Activation by an interrupt	• The corresponding bit of DTCER retains the value 1. • Activation source flag is cleared to 0.	• The corresponding bit of the DTCER bit is cleared to 0. • Activation source flag retains the value 1. • The interrupt that had been the source for activation is issued as an interrupt request for the CPU.

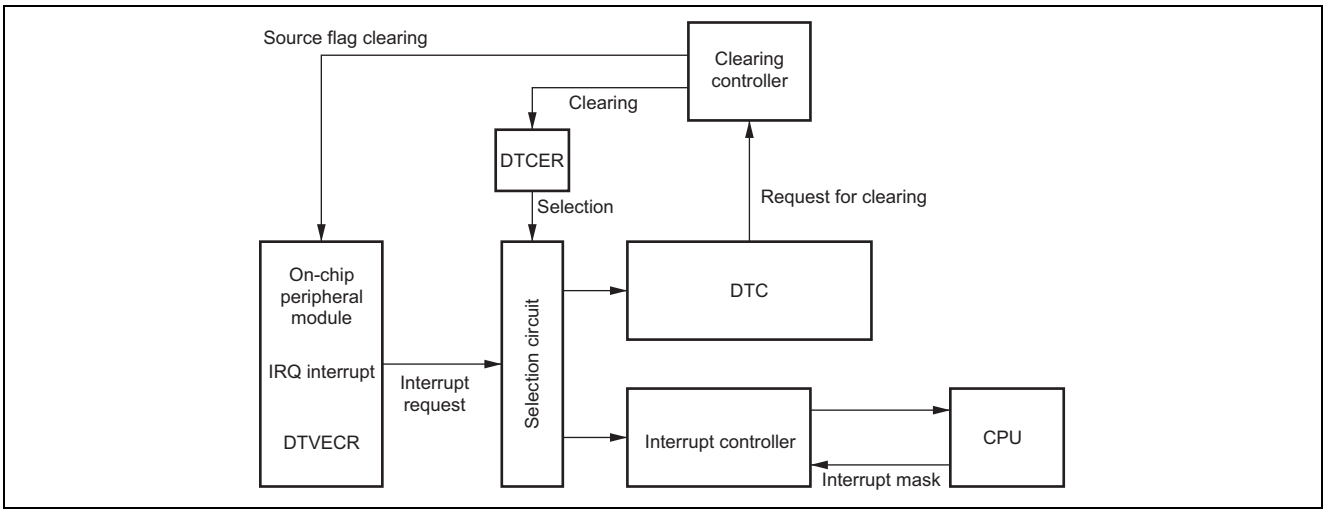


Figure 6 Block Diagram of DTC Activation Source Control

2.3.2 Location of Register Information and DTC Vector Table

Locate the register information in the on-chip RAM. Register information should be located at the address that is multiple of four. Locating the register information in address space is shown in figure 7. Locate the MRA, SAR, MRB, DAR, CRA, and CRB registers, in that order, from the start address of the register information. In the case of chained transfer, register information should be located in consecutive areas as shown in figure 7 and the register information start address should be located at the corresponding vector address to the activation source. Figure 8 shows correspondences between the DTC vector address and register information. The DTC reads the start address of the register information from the vector address set for each activation source, and then reads the register information from that start address.

Table 2 gives a list of interrupt sources capable of DTC activation, addresses in the vector table, and the corresponding DTCE bits.

When the DTC is activated by software, the vector address is obtained from: H'0400 + (DTVECR[6:0] × 2). For example, if VOFR and DTVECR are H'0000 and H'18 respectively, the vector address is H'0430.

The configuration of the vector address is a 2-byte unit. These two bytes specify the lower bits of the start address. Variable vector addresses can be used by setting VOFR. For details on VOFR settings, see the section on the interrupt controller of the *H8S/20103, H8S/20203, H8S/20223 Group Hardware Manual* (REJ09B0465).

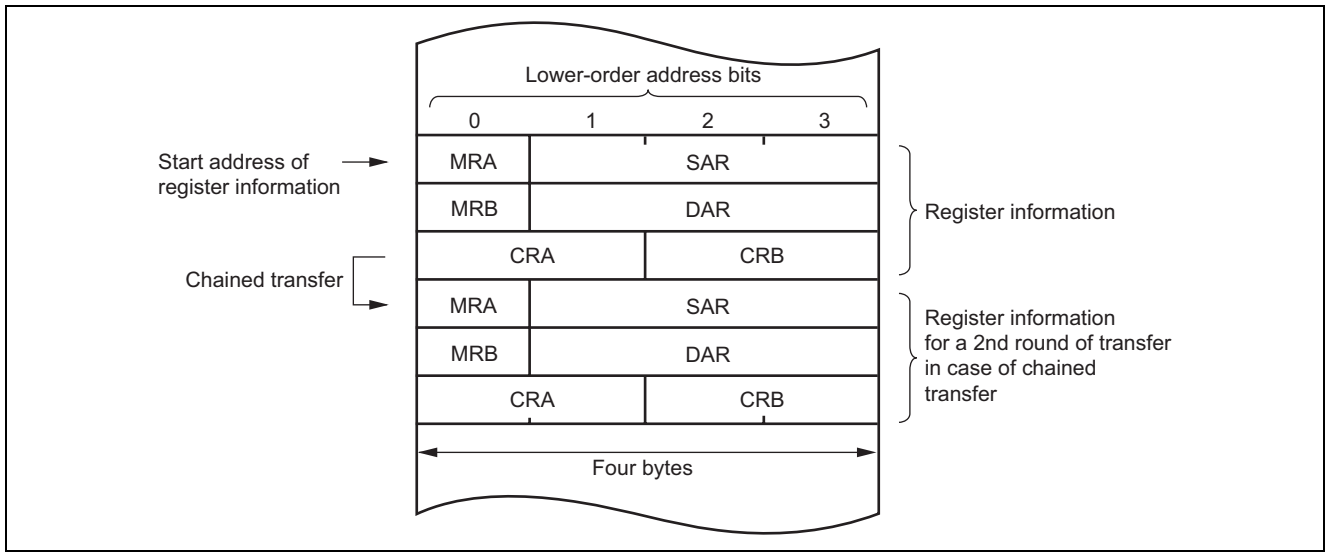


Figure 7 Locating DTC Register Information in Address Space

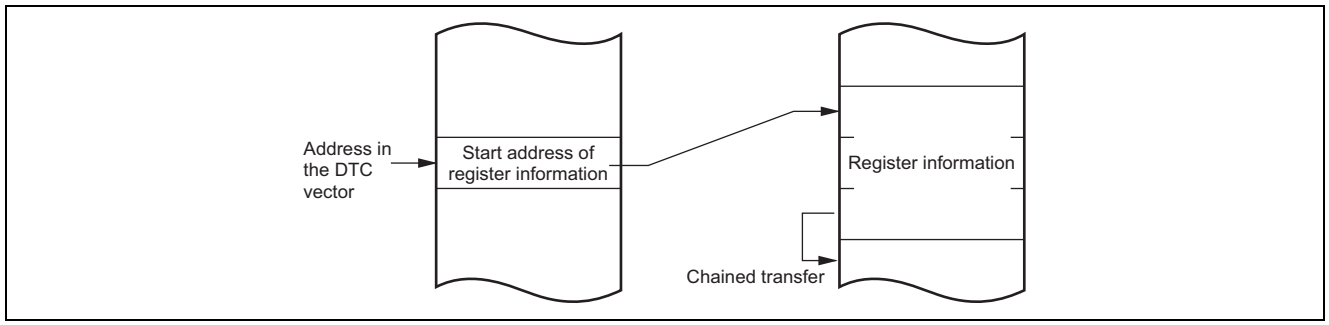


Figure 8 Correspondence between the Address in a DTC Vector and Register Information

Table 2 Interrupt Sources, Addresses of DTC Vectors, and Corresponding DTCE Bits

Origin of Activation Source	Activation Source	Vector Number	Address in Vector Table*[1]	DTCE*[5]	Priority
Software	Write to DTVECR	DTVECR	H'0400 + (DTVECR[6:0] × 2)	—	High
External pin	IRQ0	22	H'42C to H'42D	DTCEA7	
	IRQ1	23	H'42E to H'42F	DTCEA6	
	IRQ2	24	H'430 to H'431	DTCEA5	
	IRQ3	25	H'432 to H'433	DTCEA4	
	IRQ4	26	H'434 to H'435	DTCEA3	
	IRQ5	27	H'436 to H'437	DTCEA2	
	IRQ6	28	H'438 to H'439	DTCEA1	
	IRQ7	29	H'43A to H'43B	DTCEA0	
A/D converter unit 1	IADEND_1 (conversion completion)	30	H'43C to H'43D	DTCEB7	
	IADCMP_1 (compare condition match)	31	H'43E to H'43F	DTCEB6	
A/D converter unit 2	IADEND_2 (conversion completion)	32	H'442 to H'443	DTCEB5	
	IADCMP_2 (compare condition match)	33	H'444 to H'445	DTCEB4	
ELC	ELC1FP (ELSR12 event occurrence)	35	H'446 to H'447	DTCEB3	
	ELC2FP (ELSR30 event occurrence)	36	H'448 to H'449	DTCEB2	
SCI3 channel 1	SCI3_1 RXI	38	H'44C to H'44D	DTCEB1	
	SCI3_1 TXI	39	H'44E to H'44F	DTCEB0	
SCI3 channel 2	SCI3_2 RXI	42	H'454 to H'455	DTCEC7	
	SCI3_2 TXI	43	H'456 to H'457	DTCEC6	
SCI3 channel 3	SCI3_3 RXI	46	H'45C to H'45D	DTCEC5	
	SCI3_3 TXI	47	H'45E to H'45F	DTCEC4	
IIC2/SSU	IIC2/SSU_RXI	60	H'478 to H'479	DTCED7	
	IIC3/SSU_TXI	61	H'47A to H'47B	DTCED6	
Timer RC*[3]	ITCMA Input capture A/compare match A	71	H'48E to H'48F	DTCED3	
	ITCMB Input capture B/compare match B	72	H'490 to H'491	DTCED2	
	ITCMC Input capture C/compare match C	73	H'492 to H'493	DTCED1	
	ITCMD Input capture D/compare match D	74	H'494 to H'495	DTCED0	
Timer RD unit 0 channel 0	ITDMA0_0 Input capture A/compare match A	76	H'498 to H'499	DTCEE7	
	ITDMB0_0 Input capture B/compare match B	77	H'49A to H'49B	DTCEE6	
	ITDMC0_0 Input capture C/compare match C	78	H'49C to H'49D	DTCEE5	
	ITDMD0_0 Input capture D/compare match D	79	H'49E to H'49F	DTCEE4	Low

Origin of Activation Source	Activation Source	Vector Number	Address in Vector Table*[1]	DTCE*[5]	Priority
Timer RD unit 0 channel 1*[4]	ITDMA0_1 Input capture A/compare match A	82	H'4A4 to H'4A5	DTCEE3	High
	ITDMB0_1 Input capture B/compare match B	83	H'4A6 to H'4A7	DTCEE2	
	ITDMC0_1 Input capture C/compare match C	84	H'4A8 to H'4A9	DTCEE1	
	ITDMD0_1 Input capture D/compare match D	85	H'4AA to H'4AB	DTCEE0	
Timer RD unit 1 channel 2*[4]	ITDMA1_2 Input capture A/compare match A	87	H'4AE to H'4AF	DTCEF7	
	ITDMB1_2 Input capture B/compare match B	88	H'4B0 to H'4B1	DTCEF6	
	ITDMC1_2 Input capture C/compare match C	89	H'4B2 to H'4B3	DTCEF5	
	ITDMD1_2 Input capture D/compare match D	90	H'4B4 to H'4B5	DTCEF4	
Timer RD unit 1 channel 3*[4]	ITDMA1_3 Input capture A/compare match A	93	H'4BA to H'4BB	DTCEF3	
	ITDMB1_3 Input capture B/compare match B	94	H'4BC to H'4BD	DTCEF2	
	ITDMC1_3 Input capture C/compare match C	95	H'4BE to H'4BF	DTCEF1	
	ITDMD1_3 Input capture D/compare match D	96	H'4C0 to H'4C1	DTCEF0	
Timer RE	ITESC	100	H'4C8 to H'4C9	DTCEG4	
	ITEMI	101	H'4CA to H'4CB	DTCEG3	
	ITEHR	102	H'4CC to H'4CD	DTCEG2	
	ITEDY	103	H'4CE to H'4CF	DTCEG1	
	ITEWK	104	H'4D0 to H'4D1	DTCEG0	
Timer RG	ITGMA Input capture A/compare match A	109	H'4DA to H'4DB	DTCEH3	
	ITGMB Input capture B/compare match B	110	H'4DC to H'4DD	DTCEH2	Low

Notes: 1. "Address in vector table" indicates the 11 lower-order bits of the address in the vector table when VOFR = H'0000.
2. Supported only in the H8S/20223 Group and reserved in other products.
3. Supported only in the H8S/20103 Group and reserved in other products.
4. Not supported in the H8S/20103 Group and reserved in the H8S/20103 Group.
5. The DTCE bits with no corresponding interrupt are reserved. The write value should always be 0.

3. Principle of Operation

Figure 9 shows the principle of operation in this sample task. Operation as a timing pattern controller is realized without CPU intervention by timer RG and port group output by means of the hardware and software processing described in figure 9.

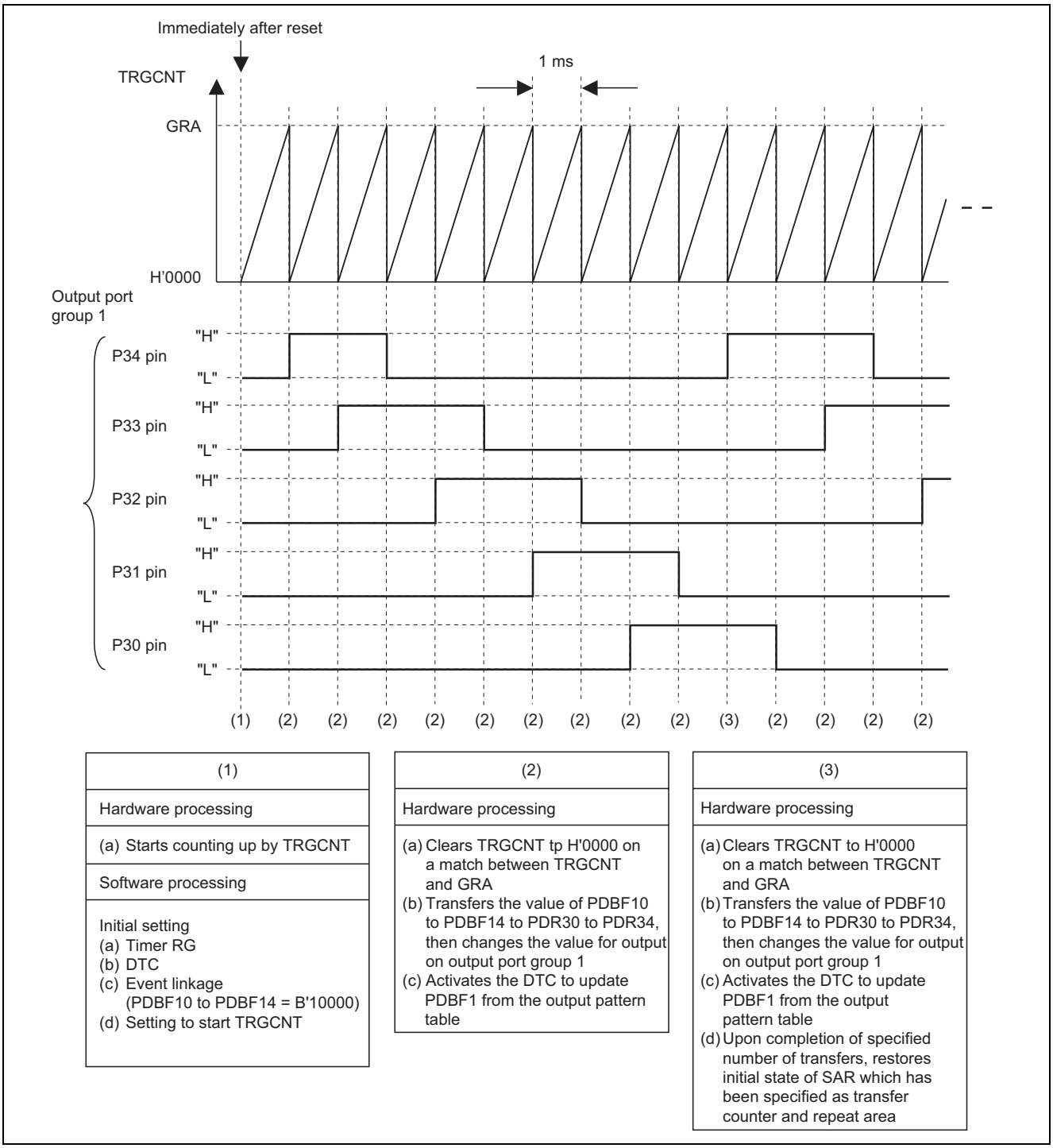


Figure 9 Principle of Operation in the Sample Task

4. Description of Software

4.1 Description of Functions

The functions in this sample task are listed and described in table 3.

Table 3 Description of Functions

Function Name	Label Name	Description
Main routine	main	Calls various other functions, enables compare match A interrupts of timer RG, and starts counting by timer RG.
System initialization routine	h8s_sysinit	Makes settings for module standby, system clock and bus-master operating clock, and halts the WDT.
Timer RG setting routine	init_tmrg	Makes settings for timer RG.
DTC setting routine	init_dtc	Makes DTC settings.
Event linkage setting routine	init_port_gr	Makes ELC settings.

4.2 Description of Argument

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 4 gives descriptions of how internal registers are used in this sample task.

Table 4 Description of Internal Registers

Register Name	Symbol	Description	Address	Setting
PMRJ	PMRJ[1:0]	The OSC1 and OSC2 functions are selected for pins PJ0/OSC1 and PJ1/OSC2.	H'FF000C	B'11
DTCERH	ITGMA	Compare match A interrupt from timer RG is selected as the source for DTC activation.	H'FF053B	1
DTVECR	DTVEC0 to DTVEC6	DTC activation vector numbers are specified.	H'FF053D	B'0000000
TRGCNT		TRGCNT is initialized.	H'FF0640	H'0000
GRA		The period of TRGCNT is specified.	H'FF0642	H'4E1F
TRGMDR	STR	Counting by TRGCNT	H'FF0646	1
	MDF	Counter incrementation is driven by the clock signal specified by TPSC0 to TPSC2 in TRGCR.		0
	PWM	In combination with the setting of the MDF bit, timer mode is selected.		0
TRGCR	CCLR[1:0]	TRGCNT is cleared on a match with GRA.	H'FF0648	B'01
	TPSC[2:0]	Internal clock: counting cycles of ϕ		B'000
TRGIOR	IOA2	GRA functions as a compare match register.	H'FF0649	0
	IOA[1:0]	Pin output in response to compare match is disabled.		B'00
TRGSR	IMFA	[Setting conditions] • GRA is functioning as a comparison register and TRGCNT = GRA. [Clearing condition] • Activation of the DTC by an IMFA interrupt while the DISEL bit in MRB of the DTC is 0. • After IMFA having been read when IMAF = 1, 0 was written to the bit.	H'FF064A	0
TRGIER	IMIEA	Interrupts corresponding to the IMFA flag are enabled.	H'FF064B	1
ELSR14		The operation of output port group 1 is linked with the compare match A signal from timer RG.	H'FF068E	H'23
PGR1	PGR14	P34 is specified as a member of the port group.	H'FF06A2	1
	PGR13	P33 is specified as a member of the port group.		1
	PGR12	P32 is specified as a member of the port group.		1
	PGR11	P31 is specified as a member of the port group.		1
	PGR10	P30 is specified as a member of the port group.		1
PGC1	PGCO1[2:0]	When the event signal corresponding to operation of port group 1 is input, the value from the buffer is output.	H'FF06A6	B'011

Register Name	Symbol	Description	Address	Setting
PDBF1	PDBF14	Buffer value to be transferred to PDR34	H'FF06AA	1*[1]
	PDBF13	Buffer value to be transferred to PDR33		0*[1]
	PDBF12	Buffer value to be transferred to PDR32		0*[1]
	PDBF11	Buffer value to be transferred to PDR31		0*[1]
	PDBF10	Buffer value to be transferred to PDR30		0*[1]
ELCR	ELCON	Linkage is enabled for all events.	H'FF06BC	1
SYSCCR	PHIHSEL	φosc is selected for clock source φhigh	H'FF06D0	1
LPCR1	PSCSTP	PSC divider is operating.	H'FF06D1	0
	PHIBSEL	φhigh is selected for clock source φbase.		1
LPCR2	PHI[2:0]	φbase is selected for system clock φ.	H'FF06D2	B'000
LPCR3	PHIS[2:0]	φ is selected for bus master operation clock φs.	H'FF06D3	B'000
OSCCSR		Setting is made for period of timer φosc oscillation settling time.	H'FF06D5	H'0E
TMWD		Clock input to WDT is prohibited.	H'FFFF99	H'F7
TCSRWD		Writing to TMWD is controlled.	H'FFFF9A	H'A3
MSTCR1	MSTWDT	The WDT is released from module standby.	H'FFFFDC	0
	MSTDTC	The DTC is released from module standby.		0
MSTCR3	MSTTMRG	Timer RG is released from module standby.	H'FFFFDE	0
PDR3	PDR34	0 is set as the initial value.	H'FFFFE2	0
	PDR33	0 is set as the initial value.		0
	PDR32	0 is set as the initial value.		0
	PDR31	0 is set as the initial value.		0
	PDR30	0 is set as the initial value.		0
PCR3	PCR34	P34 operates as an output pin.	H'FFFFF2	1
	PCR33	P33 operates as an output pin.		1
	PCR32	P32 operates as an output pin.		1
	PCR31	P31 operates as an output pin.		1
	PCR30	P30 operates as an output pin.		1
MRA*[2]	SM[1:0]	The SAR is incremented after transfer.	H'FFDF80	B'10
	DM[1:0]	The DAR is fixed after transfer.		B'00
	MD[1:0]	The DTC is placed in repeat mode.		B'01
	DTS	Source side is specified as a block area.		1
	Sz	Byte-size transfer		0
SAR*[2]		Transfer source address is specified.	H'FFDF81	H'000A00
MRB*[2]	CHNE	Setting is made so that transfer is not chained.	H'FFDF84	0
	DISEL	Setting is made so that an interrupt request for the CPU is only generated when the specified data transfer is completed.		0
DAR*[2]		Transfer destination address is specified.	H'FFDF85	H'FF06AA
CRAH*[2]		Number of unit transfers is specified.	H'FFDF88	10
CRAL*[2]		Transfer counter	H'FFDF89	10
CRB*[2]		—	H'FFDF8A	—

Notes: 1. Values are updated by DTC activation.
2. Information for the DTC registers is located in RAM.

4.4 RAM Usage

No RAM is used in this sample task.

4.5 Description of Definition in Use

Table 5 gives description of the definition used in this sample task.

Table 5 Description of Definition in Use

Label Name	Description	Constant
TPC_OUT_NUM	Number of pulse output patterns is specified.	10
SET_GRA	Period of counting by TRGCNT is set to 1 ms.	H'4E1F

4.6 Description of Constants

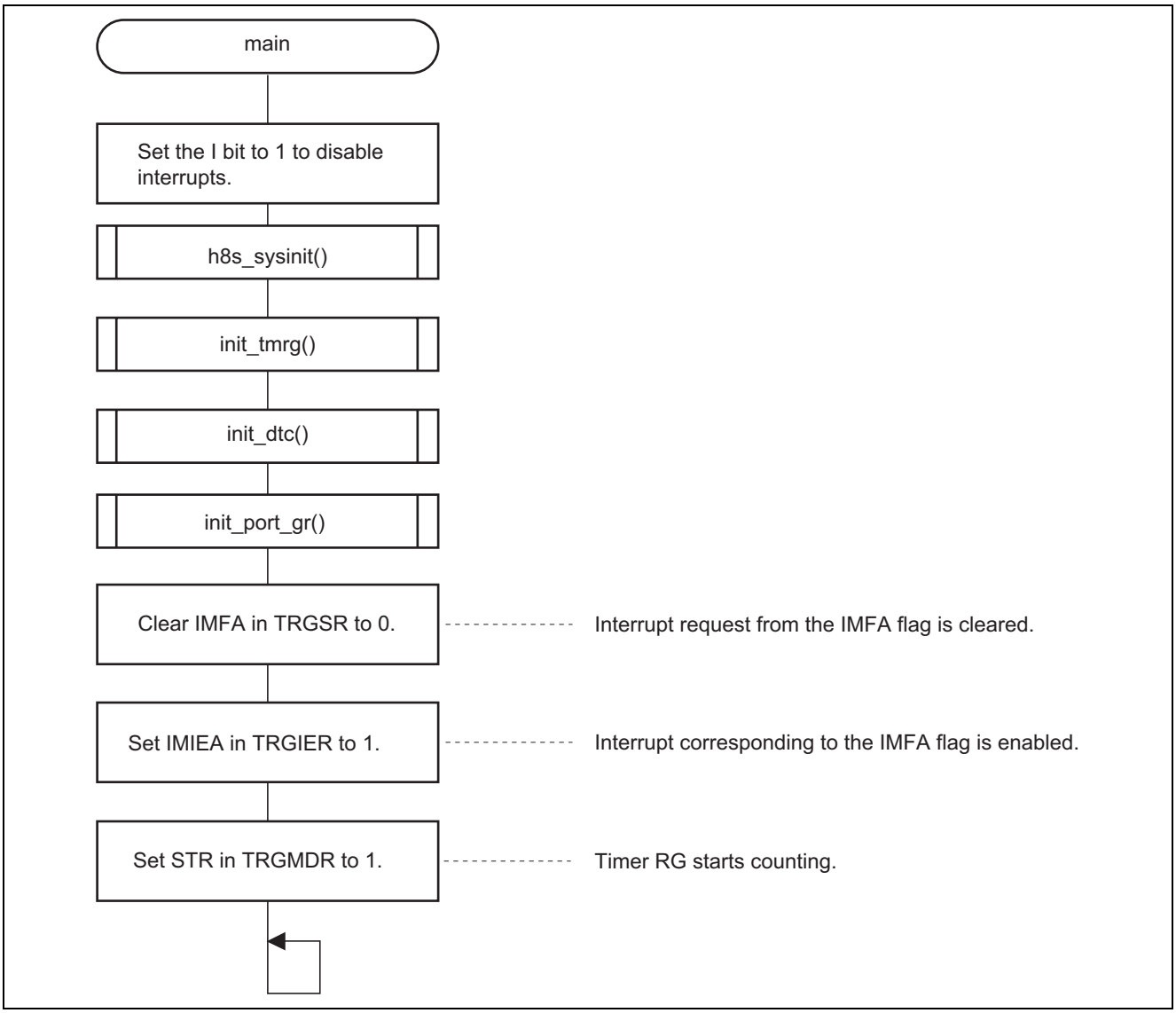
Table 6 gives description of the constants used in this sample task.

Table 6 Description of Constants

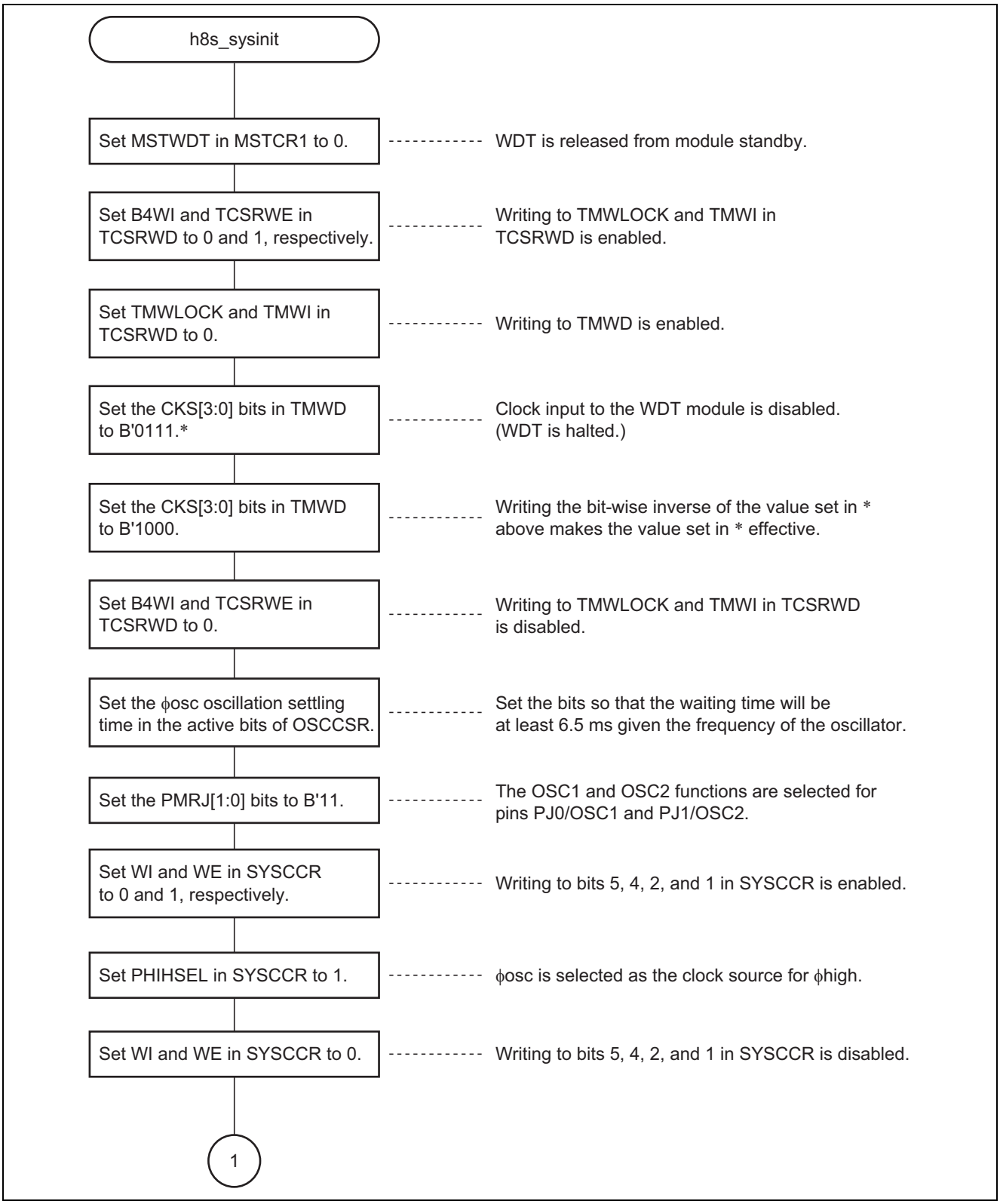
Label Name	Description	Address	Constant
tpc_out[10]	Pulse output pattern table	H'000A00	H'18, H'08, H'0C, H'04, H'06, H'02, H'03, H'01, H'11, H'10

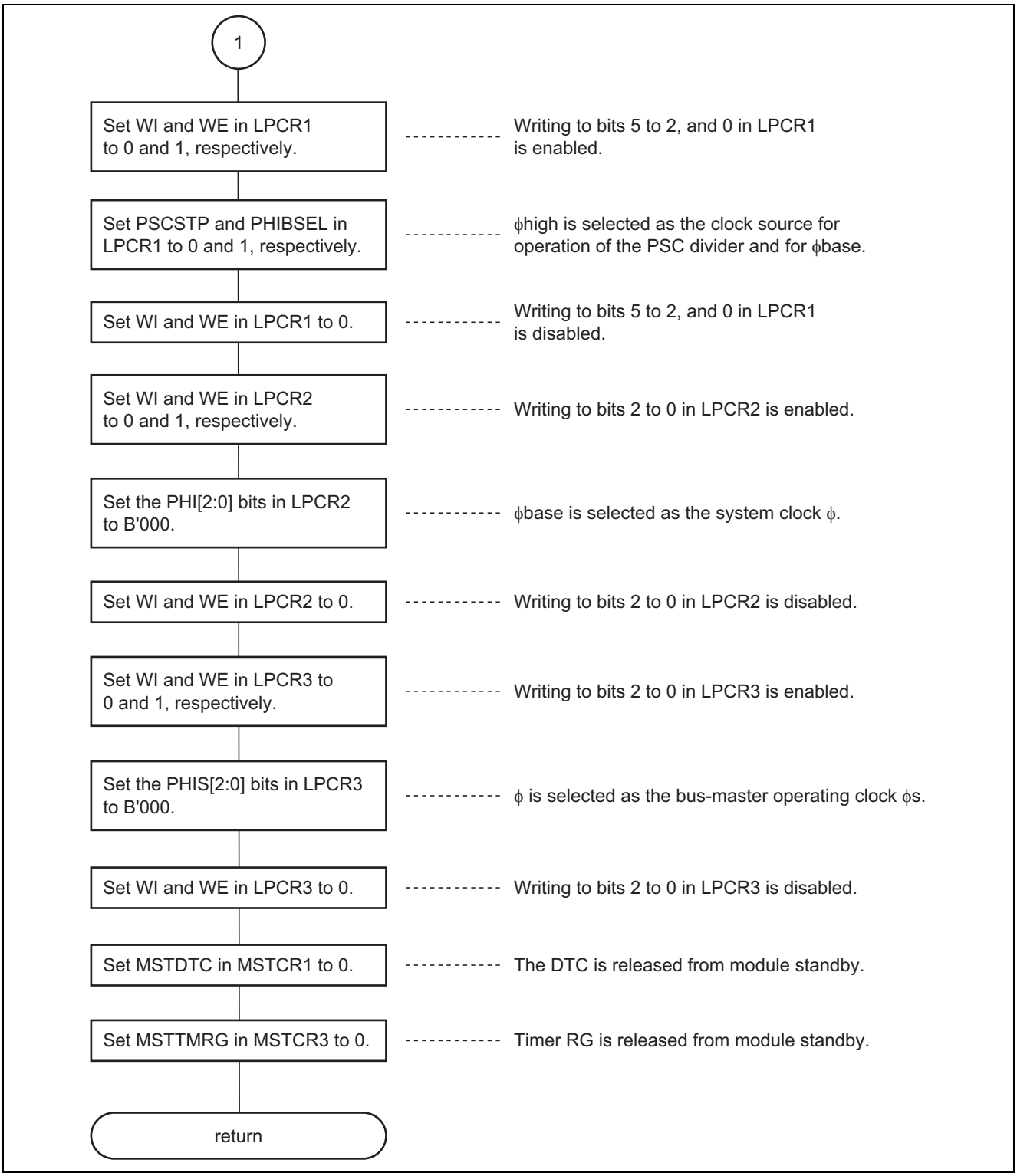
5. Flowcharts

5.1 Main Routine

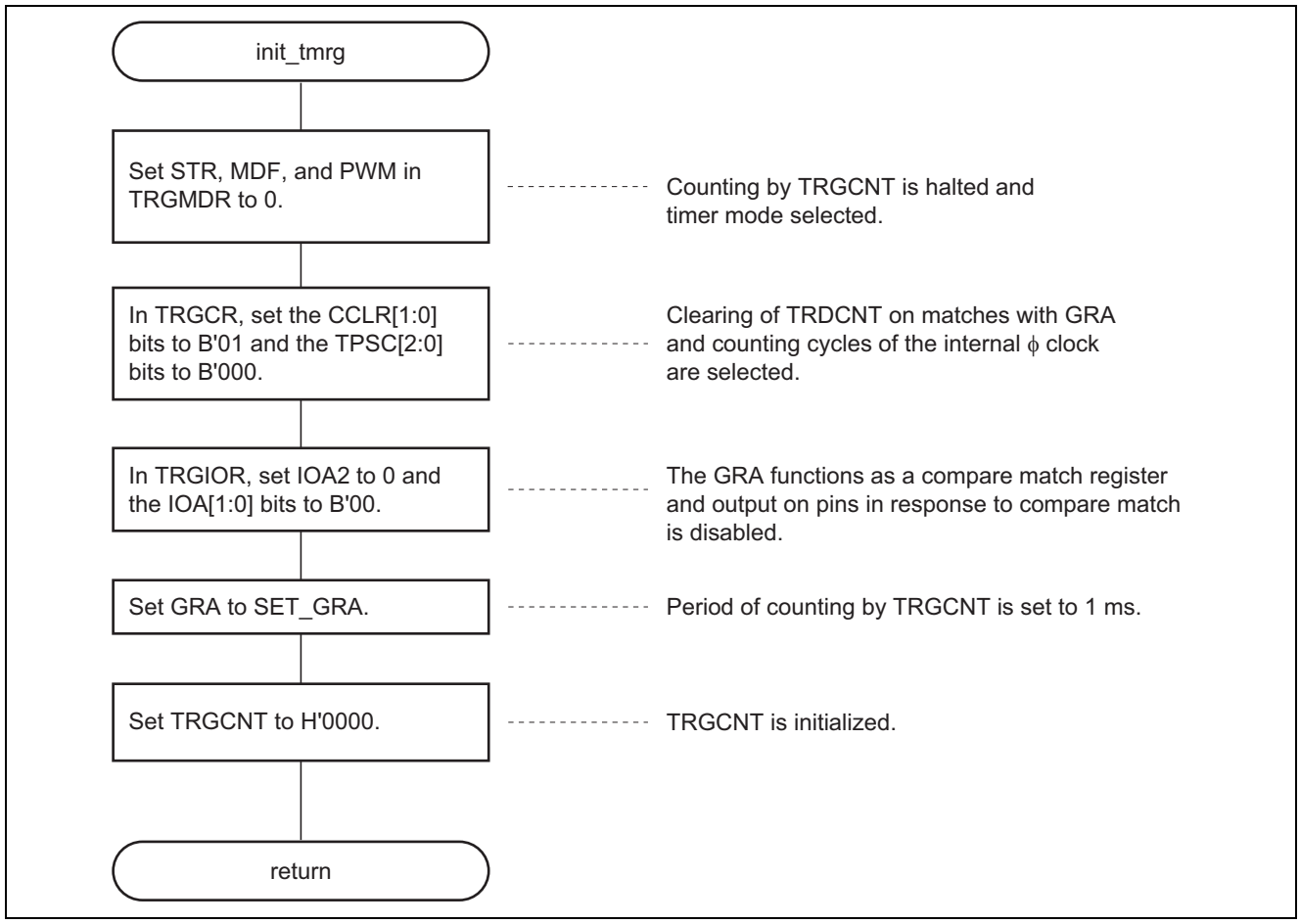


5.2 System Initialization Routine

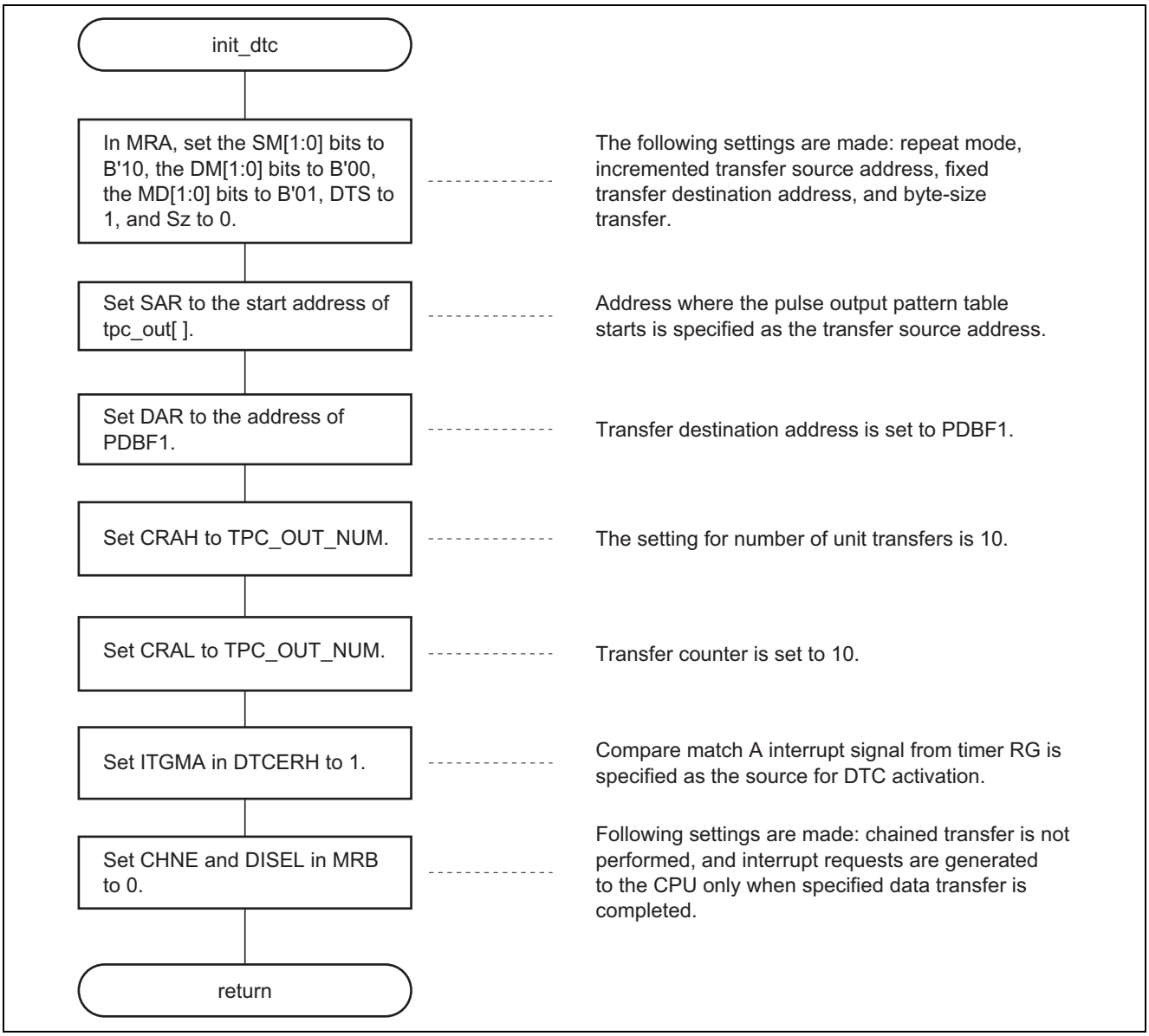



1
Set WI and WE in LPCR1 to 0 and 1, respectively.
Writing to bits 5 to 2, and 0 in LPCR1 is enabled.
Set PSCSTP and PHIBSEL in LPCR1 to 0 and 1, respectively.
ϕhigh is selected as the clock source for operation of the PSC divider and for ϕbase.
Set WI and WE in LPCR1 to 0.
Writing to bits 5 to 2, and 0 in LPCR1 is disabled.
Set WI and WE in LPCR2 to 0 and 1, respectively.
Writing to bits 2 to 0 in LPCR2 is enabled.
Set the PHI[2:0] bits in LPCR2 to B'000.
ϕbase is selected as the system clock ϕ.
Set WI and WE in LPCR2 to 0.
Writing to bits 2 to 0 in LPCR2 is disabled.
Set WI and WE in LPCR3 to 0 and 1, respectively.
Writing to bits 2 to 0 in LPCR3 is enabled.
Set the PHIS[2:0] bits in LPCR3 to B'000.
ϕ is selected as the bus-master operating clock ϕs.
Set WI and WE in LPCR3 to 0.
Writing to bits 2 to 0 in LPCR3 is disabled.
Set MSTDTC in MSTCR1 to 0.
The DTC is released from module standby.
Set MSTTMRG in MSTCR3 to 0.
Timer RG is released from module standby.
return

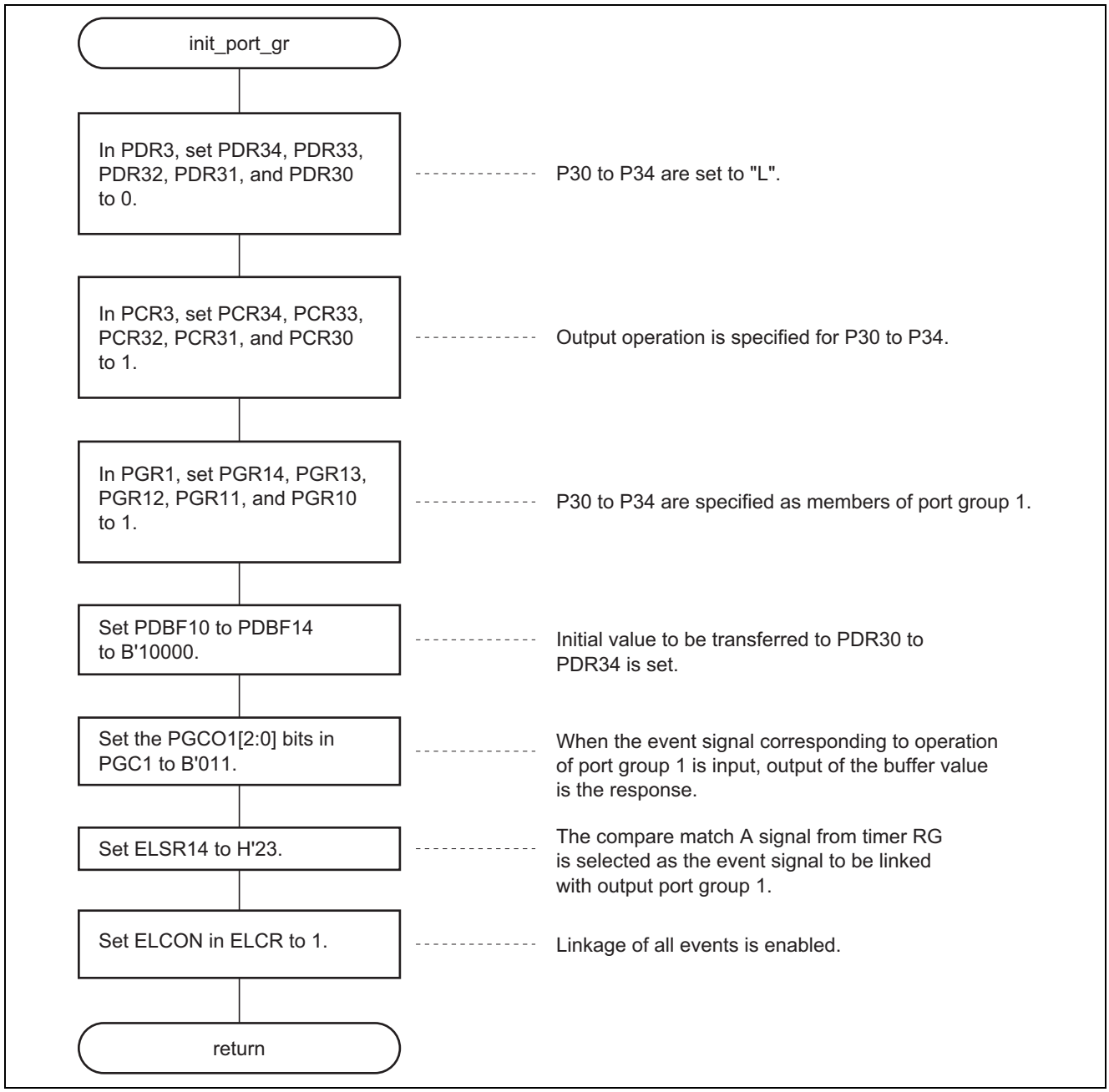
5.3 Timer RG Setting Routine



5.4 DTC Setting Routine



5.5 Event Linkage Setting Routine



6. Program Listing

```
/************************************************************************/
/*  H8S/2000 Tiny Series -H8S/20203-                                    */
/*  Application Note                                                    */
/*                                                                      */
/*  start TPC (output group port 1, DTC, Timer RG)                      */
/*                                                                      */
/*  Function                                                            */
/*  : start TPC (output group port 1 by Timer RG compare match A,       */
/*  and DTC by Timer RG compare match A interrupt                       */
/*  Event Link output group port 1 and Timer RG                         */
/*                                                                      */
/*  External Clock : 20 MHz                                             */
/*  Internal Clock : 20 MHz                                             */
/************************************************************************/
#include <machine.h>
#include "iodefine.h"

typedef struct
{
    union{
            unsigned char MRA;                          /* DTC mode register A */
            struct{
                    unsigned long      dummy1:8;        /* dummy1 data (MRA address) */
                    unsigned long      SAR:24;          /* DTC source address register */
            }SAR;
    }UN_MRA_SAR;
    union{
            unsigned char MRB;                          /* DTC mode register B */
            struct{
                    unsigned long      dummy2:8;        /* dummy2 data (DAR address) */
                    unsigned long      DAR:24;          /* DTC destination address register */
            }DAR;
    }UN_MRB_DAR;
    struct{
            unsigned char      CRAH;                    /* DTC transfer count register AH */
            unsigned char      CRAL;                    /* DTC transfer count register AL */
    }CRA; /* DTC transfer count register A */
    unsigned short     CRB;                             /* DTC transfer count register B */
} st_dtc_reg;
```

```
/*****************************************************/
/* Definition of const data                          */
/*****************************************************/
#define TPC_OUT_NUM           10             /* TPC output number */

/* Timer RG */
/* (Phi=20MHz, divide 1) */
#define SET_GRA               0x4E1F         /* Set GRA (1 ms) */

/* set PDBF1 table (TPC output) */
const unsigned char tpc_out[TPC_OUT_NUM] = {
    0x18, 0x08, 0x0C, 0x04, 0x06,
    0x02, 0x03, 0x01, 0x11, 0x10
};

/*****************************************************/
/* Declaration of function prototype                 */
/*****************************************************/
void main(void);
void init_tmrg(void);
void init_dtc(void);
void init_port_gr(void);
void h8s_sysinit(void);

/*****************************************************/
/* Definition of RAM area                            */
/*****************************************************/
#pragma section DTC
st_dtc_reg DTC_REG;                           /* DTC register */

#pragma section
```

```
/******************************************************/
/* Name:        main                                  */
/* Parameters:  None                                  */
/* Returns:     None                                  */
/* Description: User main                             */
/******************************************************/
void main(void)
{
    set_ccr(0x80);                  /* set CCR-Ibit */

    h8s_sysinit();                  /* initialize system */

    init_tmrg();                    /* initialize timer RG */

    init_dtc();                     /* initialize DTC */

    init_port_gr();                 /* initialize port group */

    TRG.TRGSR.BYTE &= 0xE0;         /* clear IMFA flag */
    TRG.TRGIER.BYTE = 0xF1;         /* interrupt enable by IMFA flag */
    TRG.TRGMDR.BIT.STR = 1;         /* TRGCNT start */

    while(1);
}

/******************************************************/
/* Name:        init_tmrg                             */
/* Parameters:  None                                  */
/* Returns:     None                                  */
/* Description: initialize timer RG                  */
/******************************************************/
void init_tmrg(void)
{
    TRG.TRGMDR.BYTE = 0x40;         /* select normal mode, TRGCNT stop */
    TRG.TRGCR.BYTE = 0xA0;          /* TRGCNT clear when compare match GRA */
                                    /* clock source Phi */
    TRG.TRGIOR.BYTE = 0x00;         /* select compare match register GRA */
    TRG.GRA = SET_GRA;              /* set GRA */
    TRG.TRGCNT = 0x0000;            /* clear TRGCNT */
}
```

```
/*****************************************************/
/* Name:        init_dtc                             */
/* Parameters:  None                                 */
/* Returns:     None                                 */
/* Description: initialize DTC (Timer RB one shot)   */
/*****************************************************/
void init_dtc(void)
{
    DTC_REG.UN_MRA_SAR.MRA = 0x86;              /* repeat mode, SAR increment, DAR hold */
                                                /* Set source to repeat area */
                                                /* transfer byte size */

    DTC_REG.UN_MRA_SAR.SAR.SAR = (unsigned long)&tpc_out;       /* Forwarding former address */
    DTC_REG.UN_MRB_DAR.DAR.DAR = (unsigned long)&ELC.PDBF1.BYTE;    /* Address at forwarding destination */
    DTC_REG.CRA.CRAH = TPC_OUT_NUM;             /* Set transfer counter keep */
    DTC_REG.CRA.CRAL = TPC_OUT_NUM;             /* Set transfer counter */

    DTC.DTCERH.BIT.ITGMA = 1;                   /* DTC start by Timer RG compare match A */
    DTC_REG.UN_MRB_DAR.MRB = 0x00;              /* disable chain, interrupt transfer end */
}

/*****************************************************/
/* Name:        init_port_gr                         */
/* Parameters:  None                                 */
/* Returns:     None                                 */
/* Description: initialize port group                */
/*****************************************************/
void init_port_gr(void)
{
    IO.PDR3.BYTE = 0x00;                        /* P34-P30 "L" */
    IO.PCR3.BYTE = 0x1F;                        /* output P34-P30 */

    /* Set event link, Timer RG compare match A */
    ELC.PGR1.BYTE = 0x1F;                       /* output port group P34-P30 */
    ELC.PDBF1.BYTE = 0x10;                      /* output port group P34:P30(B'10000) */
                                                /* TPC initialize output */
    ELC.PGC1.BYTE = 0xB9;                       /* output PDBF->PDR when event input */
    ELC.ELSR14.BYTE = 0x23;
    ELC.ELCR.BIT.ELCON = 1;                     /* event link enable */
}
```

```
/*****************************************************/
/* Name:        h8s_sysinit                          */
/* Parameters:  None                                 */
/* Returns:     None                                 */
/* Description: initialize H8S/20203                 */
/*****************************************************/
void h8s_sysinit(void)
{

    MSTCR1.BIT.MSTWDT = 0;                                  /* WDT module standby off */

    /* stop WDT */
    WDT.TCSRWD.BYTE = 0x97;                                 /* write enable TMWLOCK, TMWI */
    WDT.TCSRWD.BYTE = 0xA3;                                 /* write enable TMWD */
    WDT.TMWD.BYTE = 0xF7;                                   /* Not select clock source */
    WDT.TMWD.BYTE = 0xF8;                                   /* write bit inversion */
    WDT.TCSRWD.BYTE = 0x87;                                 /* write disable TMWLOCK, TMWI */

    CPG.OSCCSR.BYTE = 0x0E;                                 /* wait over 6.5 ms, Phi_osc = 20 MHz */
    PMRJ.BYTE = 0x03;                                       /* select OSC1, OSC2 */

    CPG.SYSCCR.BYTE = (CPG.SYSCCR.BYTE & 0x7F)| 0x40;       /* WI = 0, WE = 1 */
    CPG.SYSCCR.BYTE = 0x60;                                 /* high = Phi_osc, Phi_low = Phi_loco */
    CPG.SYSCCR.BYTE = CPG.SYSCCR.BYTE & 0x3F;               /* WI = 0, WE = 0 */

    CPG.LPCR1.BYTE = (CPG.LPCR1.BYTE & 0x7F) | 0x40;        /* WI = 0, WE = 1 */
    CPG.LPCR1.BYTE = 0x41;                                  /* PSC on, Phi_base = Phi_high */
    CPG.LPCR1.BYTE = CPG.LPCR1.BYTE & 0x3F;                 /* WI = 0, WE = 0 */

    CPG.LPCR2.BYTE = (CPG.LPCR2.BYTE & 0x7F) | 0x40;        /* WI = 0, WE = 1 */
    CPG.LPCR2.BYTE = 0x40;                                  /* select system clock */
    CPG.LPCR2.BYTE = CPG.LPCR2.BYTE & 0x3F;                 /* WI = 0, WE = 0 */

    CPG.LPCR3.BYTE = (CPG.LPCR3.BYTE & 0x7F) | 0x40;        /* WI = 0, WE = 1 */
    CPG.LPCR3.BYTE = 0x40;                                  /* select clock of bus master */
    CPG.LPCR3.BYTE = CPG.LPCR3.BYTE & 0x3F;                 /* WI = 0, WE = 0 */

    /* module standby off */
    MSTCR1.BIT.MSTDTC = 0;                                  /* DTC module standby off */
    MSTCR3.BIT.MSTTMRG = 0;                                 /* Timer RG module standby off */
}
```

6.1 Designation of Linkage Addresses

Section Name	Address
CDTC_VECT	H'000400
PResetPRG, PIntPRG	H'000500
P, C, C$DSEC, C$BSEC, D	H'000800
BDTC, B, R	H'FFDF80
S	H'FFFD80

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Rev.	**Date**	**Page**	**Summary**
1.00	Jan.19.09	—	First edition issued

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