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April 1st, 2010
Renesas Electronics Corporation

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H8S/20103, H8S/20203, and H8S/20223 Groups
Using Timer RG and Port Output for Timing Pattern Controller Operation

Introduction
The event link controller (ELC) is used to set up the compare match A signal from the timer RG module in products of the H8S/20103, H8S/20203, and H8S/20223 Groups such that operation as a programmable timing pattern controller (TPC) is realized through port event-input and port event-generation without CPU intervention.

Target Devices
H8S/20103 (R4F20103)
H8S/20203 (R4F20203)
H8S/20223 (R4F20223)

Frequency Used in Confirming Operation
System clock $\phi = \phi_{osc} = 20$ MHz

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2. Description of Modules Used .......................................................................................... 5
3. Principle of Operation ..................................................................................................... 15
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6. Program Listing .............................................................................................................. 26
1. Specifications

Specifications of this sample task are as given below. The compare match A signal from timer RG provides the time base for the output of pulses as desired without CPU intervention.

Figure 1 gives a schematic view of how the event controller sets up timer RG and output port pins for timing pattern controller operation and figure 2 shows the port output in timing pattern controller operation.

1. A table containing values for the timing of pulse output with respect to compare match A of timer RG as the time base is placed in ROM.
2. Settings are made so that timer RG is placed in timer mode, and TRGCNT counts clock source φ and is cleared on a compare match with GRA.
3. GRA is specified as a compare match register.
4. The period of timer RG is set in GRA (setting to control timing of pulse output).
5. TRGCNT is cleared to H'0000.
6. Settings are made to place the DTC in repeat mode with incrementation of transfer source addresses, a fixed transfer destination address, a repeated area on the source side, and “byte” as the unit of data transfer.
7. The source address for data transfer is specified as the first address of the pulse output pattern table that has been placed in ROM.
8. The destination address for data transfer is specified as the address of PDBF1.
9. The compare match A interrupt from timer RG is set as the activation source for the DTC.
10. PDR30 to PDR34 are set to “H” and the output direction is selected for pins P30 to P34.
11. Pins P30 to P34 are specified for use as output port group 1.
12. Initial value B’10000 to be transferred to PDR30 to PDR34 on event input is set in PDBF10 to PDBF14.
13. Settings are made so that the value from the buffer is output on port group 1 when the event signal is input.
14. For event operation of output port group 1, the compare match A signal from timer RG is specified as the event signal.
15. Event linkage is enabled.
16. The compare match A interrupt signal from timer RG is enabled.
17. Timer RG is activated.
18. Every time the compare match signal for a match between the counter of timer RG and GRA is generated, pulse output patterns are output from P30 to P34 without CPU intervention.
H8S/20103, H8S/20203, and H8S/20223 Groups
Using Timer RG and Port Output for Timing Pattern Controller Operation

Event control

ELCR

ELSR14

Settings are made to link a compare match A signal from timer RG with output port group 1.

PGR1

PGC1

PDBF1

Control of port event input and output

* When a compare match A signal from timer RG is generated, the output on output group 1 is updated.

Compare match A signal from timer RG

Input of event

Output port group 1 (port 3)

Source flag clearing

Clearing controller

DTVECR

Clearing

Selection circuit

DTCER

Selection

DTC

Interrupt controller

Interrupt mask

CPU

Updating value in buffer

Figure 1 Schematic View of How Timer RG and Port Group Output are Used to Set up TPC Operation
H8S/20103, H8S/20203, and H8S/20223 Groups
Using Timer RG and Port Output for Timing Pattern Controller Operation

Figure 2  Port Group Output in Timing Pattern Controller Operation
2. Description of Modules Used

2.1 Event Link Controller (ELC)

The features of the ELC are described below. Figure 3 is a block diagram of the ELC.

The ELC connects events generated by the various peripheral modules to other modules. This function allows direct cooperation between modules, without CPU intervention.

- Fifty-nine event signals can be directly connected to modules.
- The operation of timer modules can be selected when an event is input to the timer module.
- Events can be connected to ports 3 and 6.
- Settings for ports enable the generation of events in the form of signals on port pins.
- A single bit or any grouping of several bits can be set up for event connection on the ports used for connecting events.
- The event generation timer can be used to set up the generation of signals on four channels as events with the desired intervals.

![Figure 3 Block Diagram of Event Link Controller](image-url)
2.1.1 Operation of Peripheral Timer Modules at the Time of Event Input

Timer modules may perform any of three operations in response to the input of a signal indicating an event (event signal below). The operation depends on the ELOP settings.

1. Starting the timer counter
   When the event signal is input, the count start bit* in the given timer control register is set to 1 to make the timer start counting. Input of the event signal while the count start bit is 1 is ineffective.

2. Counting events
   The event signal is selected as the clock source for the timer so that the timer counts the events.

3. Input capture
   Input of the event signal makes the timer perform input-capture operation.

Note: * See the descriptions of the bits in the relevant sections on timers.
2.2 Timer RG

Timer RG is a 16-bit timer with output compare and input capture functions. Among other functions of this multifunctional timer for use in various applications, timer RG is capable of counting cycles of an external clock signal and producing output pulses with desired duty cycles by using compare-match signals produced by matches between the timer counter and the values in two general registers. Figure 4 is a block diagram of timer RG.

- Selection from among seven counter clock sources
  - Internal clocks: $\phi$, $\phi/2$, $\phi/4$, $\phi/8$, $\phi/32$ and $\phi/40$
  - External clocks: TCLKA, TCLKB

- Timer mode
  - Waveform output by compare match (Selection of 0 output, 1 output, or toggled output)
  - Input capture function (Rising edge, falling edge, or both edges)

- PWM mode
  - Generates pulses with a desired period and duty cycle.

- Phase counting mode
  - Detects phase difference between two external clock inputs and increments/decrements the TCNT.

- Fast access via internal 16-bit bus
  - Performs high-speed accesses to the timer counter and general registers using the 16-bit bus interface.

- Four interrupt sources
  - TRGCNT overflow, TRGCNT underflow, compare match, and input capture
2.2.1 Operation Controlled by Event Links

Using the event link controller (ELC), timer RG can be made to operate in the following ways in relation to events occurring in other modules.

1. Staring counter operation
   The start of counting operations by timer RG can be selected by ELOPC of the ELC. When the event specified by ELSR8 occurs, the STR bit in TRGMDR is set to 1, which starts counting by timer RG. However, if the specified event occurs when the STR bit has already been set to 1, the event is not effective.

2. Counting event
   The counting of events by timer RG can be selected by ELOPC of the ELC. When the event specified in ELSR8 occurs, event counter operation proceeds with that event as the source to drive counting, regardless of the setting of TPSC[2:0] bits in TRGCR. When the value of the counter is read, the value read out is the actual number of input events.

3. Input capture
   Input capture operation of timer RG can be selected by ELOPC of the ELC. When the event specified in ELSR8 occurs, GRB captures the value of TRGCNT. When input capture operation initiated by an event link is in use, set IOB[2:0] = B'101 in the TRGIOR register of timer RG, set the STR bit in TRGMDR to 1, and then start the counter. Since input on the TGIOB pin becomes valid at the same time, fix the input to the TGIOB pin or take other measures such as not allocating the TGIOB pin to the port in the PMC, etc.
2.3 Data Transfer Controller (DTC)

The features of the DTC are described below.

This LSI includes a data transfer controller (DTC). The DTC can be activated by an interrupt or software to transfer data.

Figure 5 is a block diagram of the DTC.

- Transfer possible over any number of channels
- Three transfer modes
  1. Normal mode
     - One operation transfers one byte or one word of data.
     - Memory address is incremented or decremented by 1 or 2.
     - From 1 to 65,536 transfers can be specified.
  2. Repeat mode
     - One operation transfers one byte or one word of data.
     - Memory address is incremented or decremented by 1 or 2.
     - Once the specified number of transfers (1 to 256) has ended, the initial state is restored, and transfer is repeated.
  3. Block transfer mode
     - One operation transfers specified one block of data.
     - The block size is 1 to 256 bytes or words.
     - From 1 to 65,536 transfers can be specified.
     - Either the transfer source or the transfer destination is designated as a block area.

- One activation source can trigger a number of data transfers (chained transfer)
- Direct specification of 16-Mbyte address space possible
- Activation by software is possible.
- Transfer can be set in byte or word units.
- A CPU interrupt can be requested for the interrupt that activated the DTC.
- Module standby mode can be set.
The DTC’s register information is stored in the on-chip RAM. A 32-bit bus connects the DTC to the on-chip RAM, enabling 32-bit/1-state reading and writing of the DTC register information.

Figure 5  Block Diagram of DTC
2.3.1 Activation Sources

The DTC operates when activated by an interrupt request or by writing to DTVECR by software. An interrupt request can be designated by the DTCER bit. At the end of a data transfer (or the last consecutive transfer in the case of chained transfer), the activation source interrupt flag is the RDRF flag of SCI3_1.

When an interrupt has been designated a DTC activation source, existing CPU mask level and interrupt controller priorities have no effect. If there is more than one activation source at the same time, the DTC operates in accordance with the default priorities for the interrupt sources. Table 1 shows a relationship between activation sources and DTCER clear conditions. Figure 6 is a block diagram of DTC activation source control. For details, see the section on the interrupt controller of H8S/20103, H8S/20203, H8S/20223 Group Hardware Manual (REJ09B0465).

Table 1 Relationship between Activation Sources and DTCER Clearing

<table>
<thead>
<tr>
<th>Activation Source</th>
<th>DISEL = 0 and Specified Number of Transfers Has Not Ended</th>
<th>DISEL = 1 or Specified Number of Transfers Has Ended</th>
</tr>
</thead>
<tbody>
<tr>
<td>Activation by software</td>
<td>The SWDTE bit is cleared to 0.</td>
<td>• The SWDTE bit retains the value 1.</td>
</tr>
<tr>
<td>Activation by an interrupt</td>
<td>• The corresponding bit of DTCER retains the value 1.</td>
<td>• The corresponding bit of the DTCER bit is cleared to 0.</td>
</tr>
<tr>
<td></td>
<td>• Activation source flag is cleared to 0.</td>
<td>• Activation source flag retains the value 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The interrupt that had been the source for activation is issued as an interrupt request for the CPU.</td>
</tr>
</tbody>
</table>

Figure 6 Block Diagram of DTC Activation Source Control
2.3.2 Location of Register Information and DTC Vector Table

Locate the register information in the on-chip RAM. Register information should be located at the address that is multiple of four. Locating the register information in address space is shown in figure 7. Locate the MRA, SAR, MRB, DAR, CRA, and CRB registers, in that order, from the start address of the register information. In the case of chained transfer, register information should be located in consecutive areas as shown in figure 7 and the register information start address should be located at the corresponding vector address to the activation source. Figure 8 shows correspondences between the DTC vector address and register information. The DTC reads the start address of the register information from the vector address set for each activation source, and then reads the register information from that start address.

Table 2 gives a list of interrupt sources capable of DTC activation, addresses in the vector table, and the corresponding DTCE bits.

When the DTC is activated by software, the vector address is obtained from: H'0400 + (DTVECR[6:0] × 2). For example, if VOFR and DTVECR are H'0000 and H'18 respectively, the vector address is H'0430.

The configuration of the vector address is a 2-byte unit. These two bytes specify the lower bits of the start address. Variable vector addresses can be used by setting VOFR. For details on VOFR settings, see the section on the interrupt controller of the *H8S/20103, H8S/20203, H8S/20223 Group Hardware Manual* (REJ09B0465).
### Table 2  Interrupt Sources, Addresses of DTC Vectors, and Corresponding DTCE Bits

<table>
<thead>
<tr>
<th>Origin of Activation Source</th>
<th>Activation Source</th>
<th>Vector Number</th>
<th>Address in Vector</th>
<th>DTCE Bits</th>
<th>Priority</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software</td>
<td>Write to DTVECR</td>
<td>DTVECR</td>
<td>$H'0400 + (\text{DTVECR}[6:0] \times 2)$</td>
<td>—</td>
<td>High</td>
</tr>
<tr>
<td>External pin</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>IRQ0</td>
<td>22</td>
<td>$H'42C$ to $H'42D$</td>
<td>DTCEA7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IRQ1</td>
<td>23</td>
<td>$H'42E$ to $H'42F$</td>
<td>DTCEA6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IRQ2</td>
<td>24</td>
<td>$H'430$ to $H'431$</td>
<td>DTCEA5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IRQ3</td>
<td>25</td>
<td>$H'432$ to $H'433$</td>
<td>DTCEA4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IRQ4</td>
<td>26</td>
<td>$H'434$ to $H'435$</td>
<td>DTCEA3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IRQ5</td>
<td>27</td>
<td>$H'436$ to $H'437$</td>
<td>DTCEA2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IRQ6</td>
<td>28</td>
<td>$H'438$ to $H'439$</td>
<td>DTCEA1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IRQ7</td>
<td>29</td>
<td>$H'43A$ to $H'43B$</td>
<td>DTCEA0</td>
<td></td>
</tr>
<tr>
<td>A/D converter unit 1</td>
<td>IADEND_1</td>
<td>30</td>
<td>$H'43C$ to $H'43D$</td>
<td>DTCEB7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(conversion completion)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>IADCMP_1</td>
<td>31</td>
<td>$H'43E$ to $H'43F$</td>
<td>DTCEB6</td>
<td></td>
</tr>
<tr>
<td>A/D converter unit 2</td>
<td>IADEND_2</td>
<td>32</td>
<td>$H'442$ to $H'443$</td>
<td>DTCEB5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(conversion completion)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>IADCMP_2</td>
<td>33</td>
<td>$H'444$ to $H'445$</td>
<td>DTCEB4</td>
<td></td>
</tr>
<tr>
<td>ELC</td>
<td>ELC1FP</td>
<td>35</td>
<td>$H'446$ to $H'447$</td>
<td>DTCEB3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(ELSR12 event occurrence)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ELC2FP</td>
<td>36</td>
<td>$H'448$ to $H'449$</td>
<td>DTCEB2</td>
<td></td>
</tr>
<tr>
<td>SCI3 channel 1</td>
<td>SCI3_1 RXI</td>
<td>38</td>
<td>$H'44C$ to $H'44D$</td>
<td>DTCEB1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SCI3_1 TXI</td>
<td>39</td>
<td>$H'44E$ to $H'44F$</td>
<td>DTCEB0</td>
<td></td>
</tr>
<tr>
<td>SCI3 channel 2</td>
<td>SCI3_2 RXI</td>
<td>42</td>
<td>$H'454$ to $H'455$</td>
<td>DTCEC7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SCI3_2 TXI</td>
<td>43</td>
<td>$H'456$ to $H'457$</td>
<td>DTCEC6</td>
<td></td>
</tr>
<tr>
<td>SCI3 channel 3</td>
<td>SCI3_3 RXI</td>
<td>46</td>
<td>$H'45C$ to $H'45D$</td>
<td>DTCEC5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SCI3_3 TXI</td>
<td>47</td>
<td>$H'45E$ to $H'45F$</td>
<td>DTCEC4</td>
<td></td>
</tr>
<tr>
<td>IIC2/SSU</td>
<td>IIC2/SSU_RXI</td>
<td>60</td>
<td>$H'478$ to $H'479$</td>
<td>DTCED7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IIC3/SSU_TXI</td>
<td>61</td>
<td>$H'47A$ to $H'47B$</td>
<td>DTCED6</td>
<td></td>
</tr>
<tr>
<td>Timer RC</td>
<td>ITCMA</td>
<td>71</td>
<td>$H'48E$ to $H'48F$</td>
<td>DTCED3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input capture A/compare match A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ITCMB</td>
<td>72</td>
<td>$H'490$ to $H'491$</td>
<td>DTCED2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input capture B/compare match B</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ITCMC</td>
<td>73</td>
<td>$H'492$ to $H'493$</td>
<td>DTCED1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input capture C/compare match C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ITCMD</td>
<td>74</td>
<td>$H'494$ to $H'495$</td>
<td>DTCED0</td>
<td></td>
</tr>
<tr>
<td>Timer RD unit 0 channel 0</td>
<td>ITDMA0_0</td>
<td>76</td>
<td>$H'498$ to $H'499$</td>
<td>DTCEE7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input capture A/compare match A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ITDMBO_0</td>
<td>77</td>
<td>$H'49A$ to $H'49B$</td>
<td>DTCEE6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input capture C/compare match C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ITDMCO_0</td>
<td>78</td>
<td>$H'49C$ to $H'49D$</td>
<td>DTCEE5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input capture D/compare match D</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ITDMDO_0</td>
<td>79</td>
<td>$H'49E$ to $H'49F$</td>
<td>DTCEE4</td>
<td></td>
</tr>
</tbody>
</table>
### Origin of Activation Source

<table>
<thead>
<tr>
<th>Activation Source</th>
<th>Vector Number</th>
<th>Address in Vector Table&lt;sup&gt;1&lt;/sup&gt;</th>
<th>DTCE&lt;sup&gt;4&lt;/sup&gt;</th>
<th>Priority</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer RD unit 0 channel 1&lt;sup&gt;44&lt;/sup&gt;</td>
<td>ITDMA0&lt;sub&gt;1&lt;/sub&gt;</td>
<td>82</td>
<td>H'4A4 to H'4A5</td>
<td>DTCEE3</td>
</tr>
<tr>
<td></td>
<td>ITDMB0&lt;sub&gt;1&lt;/sub&gt;</td>
<td>83</td>
<td>H'4A6 to H'4A7</td>
<td>DTCEE2</td>
</tr>
<tr>
<td></td>
<td>ITDMC0&lt;sub&gt;1&lt;/sub&gt;</td>
<td>84</td>
<td>H'4A8 to H'4A9</td>
<td>DTCEE1</td>
</tr>
<tr>
<td></td>
<td>ITDMO0&lt;sub&gt;1&lt;/sub&gt;</td>
<td>85</td>
<td>H'4AA to H'4AB</td>
<td>DTCEE0</td>
</tr>
<tr>
<td>Timer RD unit 1 channel 2&lt;sup&gt;44&lt;/sup&gt;</td>
<td>ITDMA1&lt;sub&gt;2&lt;/sub&gt;</td>
<td>87</td>
<td>H'4AE to H'4AF</td>
<td>DTCEF7</td>
</tr>
<tr>
<td></td>
<td>ITDMB1&lt;sub&gt;2&lt;/sub&gt;</td>
<td>88</td>
<td>H'4B0 to H'4B1</td>
<td>DTCEF6</td>
</tr>
<tr>
<td></td>
<td>ITDMC1&lt;sub&gt;2&lt;/sub&gt;</td>
<td>89</td>
<td>H'4B2 to H'4B3</td>
<td>DTCEF5</td>
</tr>
<tr>
<td></td>
<td>ITDMO1&lt;sub&gt;2&lt;/sub&gt;</td>
<td>90</td>
<td>H'4B4 to H'4B5</td>
<td>DTCEF4</td>
</tr>
<tr>
<td>Timer RD unit 1 channel 3&lt;sup&gt;44&lt;/sup&gt;</td>
<td>ITDMA1&lt;sub&gt;3&lt;/sub&gt;</td>
<td>93</td>
<td>H'4BA to H'4BB</td>
<td>DTCEF3</td>
</tr>
<tr>
<td></td>
<td>ITDMB1&lt;sub&gt;3&lt;/sub&gt;</td>
<td>94</td>
<td>H'4BC to H'4BD</td>
<td>DTCEF2</td>
</tr>
<tr>
<td></td>
<td>ITDMC1&lt;sub&gt;3&lt;/sub&gt;</td>
<td>95</td>
<td>H'4BE to H'4BF</td>
<td>DTCEF1</td>
</tr>
<tr>
<td></td>
<td>ITDMO1&lt;sub&gt;3&lt;/sub&gt;</td>
<td>96</td>
<td>H'4C0 to H'4C1</td>
<td>DTCEF0</td>
</tr>
<tr>
<td>Timer RE</td>
<td>ITESC</td>
<td>100</td>
<td>H'4C8 to H'4C9</td>
<td>DTCEG4</td>
</tr>
<tr>
<td></td>
<td>ITEMI</td>
<td>101</td>
<td>H'4CA to H'4CB</td>
<td>DTCEG3</td>
</tr>
<tr>
<td></td>
<td>ITEHRR</td>
<td>102</td>
<td>H'4CC to H'4CD</td>
<td>DTCEG2</td>
</tr>
<tr>
<td></td>
<td>ITEDY</td>
<td>103</td>
<td>H'4CE to H'4CF</td>
<td>DTCEG1</td>
</tr>
<tr>
<td></td>
<td>ITEWK</td>
<td>104</td>
<td>H'4D0 to H'4D1</td>
<td>DTCEG0</td>
</tr>
<tr>
<td>Timer RG</td>
<td>ITGMA</td>
<td>109</td>
<td>H'4DA to H'4DB</td>
<td>DTCEH3</td>
</tr>
<tr>
<td></td>
<td>ITGMB</td>
<td>110</td>
<td>H'4DC to H'4DD</td>
<td>DTCEH2</td>
</tr>
</tbody>
</table>

Notes:
1. "Address in vector table" indicates the 11 lower-order bits of the address in the vector table when VOFR = H'0000.
2. Supported only in the H8S/20223 Group and reserved in other products.
3. Supported only in the H8S/20103 Group and reserved in other products.
4. Not supported in the H8S/20103 Group and reserved in the H8S/20103 Group.
5. The DTCE bits with no corresponding interrupt are reserved. The write value should always be 0.
3. Principle of Operation

Figure 9 shows the principle of operation in this sample task. Operation as a timing pattern controller is realized without CPU intervention by timer RG and port group output by means of the hardware and software processing described in figure 9.

![Figure 9 Principle of Operation in the Sample Task](image-url)
4. Description of Software

4.1 Description of Functions

The functions in this sample task are listed and described in table 3.

Table 3 Description of Functions

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Label Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>main</td>
<td>Calls various other functions, enables compare match A interrupts of timer RG, and starts counting by timer RG.</td>
</tr>
<tr>
<td>System initialization routine</td>
<td>h8s_sysinit</td>
<td>Makes settings for module standby, system clock and bus-master operating clock, and halts the WDT.</td>
</tr>
<tr>
<td>Timer RG setting routine</td>
<td>init_tmrg</td>
<td>Makes settings for timer RG.</td>
</tr>
<tr>
<td>DTC setting routine</td>
<td>init_dtc</td>
<td>Makes DTC settings.</td>
</tr>
<tr>
<td>Event linkage setting routine</td>
<td>init_port_gr</td>
<td>Makes ELC settings.</td>
</tr>
</tbody>
</table>

4.2 Description of Argument

No arguments are used in this sample task.
### 4.3 Description of Internal Registers

Table 4 gives descriptions of how internal registers are used in this sample task.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Symbol</th>
<th>Description</th>
<th>Address</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMRJ</td>
<td>PMRJ[1:0]</td>
<td>The OSC1 and OSC2 functions are selected for pins PJ0/OSC1 and PJ1/OSC2.</td>
<td>H'FF000C</td>
<td>B'11</td>
</tr>
<tr>
<td>DTCERH</td>
<td>ITGMA</td>
<td>Compare match A interrupt from timer RG is selected as the source for DTC activation.</td>
<td>H'FF053B</td>
<td>1</td>
</tr>
<tr>
<td>DTVECR</td>
<td>DTVEC0 to DTVEC6</td>
<td>DTC activation vector numbers are specified.</td>
<td>H'FF053D</td>
<td>B'0000000</td>
</tr>
<tr>
<td>TRGCNT</td>
<td></td>
<td>TRGCNT is initialized.</td>
<td>H'FF0640</td>
<td>H'0000</td>
</tr>
<tr>
<td>GRA</td>
<td></td>
<td>The period of TRGCNT is specified.</td>
<td>H'FF0642</td>
<td>H'4E1F</td>
</tr>
<tr>
<td>TRGMDR</td>
<td>STR</td>
<td>Counting by TRGCNT</td>
<td>H'FF0646</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>MDF</td>
<td>Counter incrementation is driven by the clock signal specified by TPSC0 to TPSC2 in TRGCR.</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PWM</td>
<td>In combination with the setting of the MDF bit, timer mode is selected.</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>TRGCR</td>
<td>CCLR[1:0]</td>
<td>TRGCNT is cleared on a match with GRA.</td>
<td>H'FF0648</td>
<td>B'01</td>
</tr>
<tr>
<td></td>
<td>TPSC[2:0]</td>
<td>Internal clock: counting cycles of</td>
<td>B'0000</td>
<td></td>
</tr>
<tr>
<td>TRGIOR</td>
<td>IOA2</td>
<td>GRA functions as a compare match register.</td>
<td>H'FF0649</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>IOA[1:0]</td>
<td>Pin output in response to compare match is disabled.</td>
<td>B'00</td>
<td></td>
</tr>
<tr>
<td>TRGSR</td>
<td>IMFA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>[Setting conditions]</td>
<td>GRA is functioning as a comparison register and TRGCNT = GRA.</td>
<td>H'FF064A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>[Clearing condition]</td>
<td>Activation of the DTC by an IMFA interrupt while the DISEL bit in MRB of the DTC is 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>After IMFA having been read when IMAF = 1, 0 was written to the bit.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TRGIER</td>
<td>IMIEA</td>
<td>Interrupts corresponding to the IMFA flag are enabled.</td>
<td>H'FF064B</td>
<td>1</td>
</tr>
<tr>
<td>ELSR14</td>
<td></td>
<td>The operation of output port group 1 is linked with the compare match A signal from timer RG.</td>
<td>H'FF068E</td>
<td>H'23</td>
</tr>
<tr>
<td>PGR1</td>
<td>PGR14</td>
<td>P34 is specified as a member of the port group.</td>
<td>H'FF06A2</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>PGR13</td>
<td>P33 is specified as a member of the port group.</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PGR12</td>
<td>P32 is specified as a member of the port group.</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PGR11</td>
<td>P31 is specified as a member of the port group.</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PGR10</td>
<td>P30 is specified as a member of the port group.</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>PGC1</td>
<td>PGCO1[2:0]</td>
<td>When the event signal corresponding to operation of port group 1 is input, the value from the buffer is output.</td>
<td>H'FF06A6</td>
<td>B'011</td>
</tr>
</tbody>
</table>
### Register Table

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Symbol</th>
<th>Description</th>
<th>Address</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDBF1</td>
<td>PDBF14</td>
<td>Buffer value to be transferred to PDR34</td>
<td>H'FF06AA</td>
<td>1*1</td>
</tr>
<tr>
<td></td>
<td>PDBF13</td>
<td>Buffer value to be transferred to PDR33</td>
<td>H'FF06D0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>PDBF12</td>
<td>Buffer value to be transferred to PDR32</td>
<td>H'FF06BC</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>PDBF11</td>
<td>Buffer value to be transferred to PDR31</td>
<td>H'FF06D1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>PDBF10</td>
<td>Buffer value to be transferred to PDR30</td>
<td>H'FF06DA</td>
<td>0</td>
</tr>
<tr>
<td>ELCR</td>
<td>ELCON</td>
<td>Linkage is enabled for all events.</td>
<td>H'FF06BC</td>
<td>1</td>
</tr>
<tr>
<td>SYSCCR</td>
<td>PHIHSEL</td>
<td>φosc is selected for clock source φhigh</td>
<td>H'FF06D2</td>
<td>B’000</td>
</tr>
<tr>
<td>LPCR1</td>
<td>PSCSTP</td>
<td>PSC divider is operating.</td>
<td>H'FF06D0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>PHIBSEL</td>
<td>φhigh is selected for clock source φbase.</td>
<td>H'FF06D1</td>
<td>0</td>
</tr>
<tr>
<td>LPCR2</td>
<td>PHI[2:0]</td>
<td>φbase is selected for system clock φ.</td>
<td>H'FF06D2</td>
<td>B’000</td>
</tr>
<tr>
<td>LPCR3</td>
<td>PHIS[2:0]</td>
<td>φ is selected for bus master operation clock φs.</td>
<td>H'FF06D3</td>
<td>B’000</td>
</tr>
<tr>
<td>OSCCSR</td>
<td></td>
<td>Setting is made for period of timer φosc oscillation settling time.</td>
<td>H'FF06D5</td>
<td>H’0E</td>
</tr>
<tr>
<td>TMWD</td>
<td></td>
<td>Clock input to WDT is prohibited.</td>
<td>H'FFFF99</td>
<td>H’F7</td>
</tr>
<tr>
<td>TCSRWD</td>
<td></td>
<td>Writing to TMWD is controlled.</td>
<td>H'FFFF9A</td>
<td>H’A3</td>
</tr>
<tr>
<td>MSTCR1</td>
<td>MSTWDT</td>
<td>The WDT is released from module standby.</td>
<td>H'FFFFDC</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MSTDTC</td>
<td>The DTC is released from module standby.</td>
<td>H'FFFFDE</td>
<td>0</td>
</tr>
<tr>
<td>MSTCR3</td>
<td>MSTRMRG</td>
<td>Timer RG is released from module standby.</td>
<td>H'FFFFDE</td>
<td>0</td>
</tr>
<tr>
<td>PDR3</td>
<td>PDR34</td>
<td>0 is set as the initial value.</td>
<td>H'FFFFE2</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>PDR33</td>
<td>0 is set as the initial value.</td>
<td>H'FFFFE3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>PDR32</td>
<td>0 is set as the initial value.</td>
<td>H'FFFFE4</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>PDR31</td>
<td>0 is set as the initial value.</td>
<td>H'FFFFE5</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>PDR30</td>
<td>0 is set as the initial value.</td>
<td>H'FFFFE6</td>
<td>0</td>
</tr>
<tr>
<td>PCR3</td>
<td>PCR34</td>
<td>P34 operates as an output pin.</td>
<td>H'FFFFF2</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>PCR33</td>
<td>P33 operates as an output pin.</td>
<td>H'FFFFF3</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>PCR32</td>
<td>P32 operates as an output pin.</td>
<td>H'FFFFF4</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>PCR31</td>
<td>P31 operates as an output pin.</td>
<td>H'FFFFF5</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>PCR30</td>
<td>P30 operates as an output pin.</td>
<td>H'FFFFF6</td>
<td>1</td>
</tr>
<tr>
<td>MRA*2</td>
<td>SM[1:0]</td>
<td>The SAR is incremented after transfer.</td>
<td>H'FFDF80</td>
<td>B’10</td>
</tr>
<tr>
<td></td>
<td>DM[1:0]</td>
<td>The DAR is fixed after transfer.</td>
<td>H'FFDF81</td>
<td>B’00</td>
</tr>
<tr>
<td></td>
<td>MD[1:0]</td>
<td>The DTC is placed in repeat mode.</td>
<td>H'FFDF82</td>
<td>B’01</td>
</tr>
<tr>
<td></td>
<td>DTS</td>
<td>Source side is specified as a block area.</td>
<td>H'FFDF83</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Sz</td>
<td>Byte-size transfer</td>
<td>H'FFDF84</td>
<td>0</td>
</tr>
<tr>
<td>SAR*2</td>
<td>CHNE</td>
<td>Setting is made so that transfer is not chained.</td>
<td>H'FFDF85</td>
<td>0</td>
</tr>
<tr>
<td>MRB*2</td>
<td></td>
<td>Setting is made so that an interrupt request for the CPU is only generated when the specified data transfer is completed.</td>
<td>H'FFDF86</td>
<td>0</td>
</tr>
<tr>
<td>DAR*2</td>
<td></td>
<td>Transfer destination address is specified.</td>
<td>H'FFDF87</td>
<td>0</td>
</tr>
<tr>
<td>CRAH*2</td>
<td></td>
<td>Number of unit transfers is specified.</td>
<td>H'FFDF88</td>
<td>10</td>
</tr>
<tr>
<td>CRAL*2</td>
<td></td>
<td>Transfer counter</td>
<td>H'FFDF89</td>
<td>10</td>
</tr>
<tr>
<td>CRB*2</td>
<td></td>
<td></td>
<td>H'FFDF8A</td>
<td>—</td>
</tr>
</tbody>
</table>

Notes:
1. Values are updated by DTC activation.
2. Information for the DTC registers is located in RAM.
4.4 RAM Usage

No RAM is used in this sample task.

4.5 Description of Definition in Use

Table 5 gives description of the definition used in this sample task.

<table>
<thead>
<tr>
<th>Label Name</th>
<th>Description</th>
<th>Constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPC_OUT_NUM</td>
<td>Number of pulse output patterns is specified.</td>
<td>10</td>
</tr>
<tr>
<td>SET_GRA</td>
<td>Period of counting by TRGCNT is set to 1 ms.</td>
<td>H'4E1F</td>
</tr>
</tbody>
</table>

4.6 Description of Constants

Table 6 gives description of the constants used in this sample task.

<table>
<thead>
<tr>
<th>Label Name</th>
<th>Description</th>
<th>Address</th>
<th>Constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>tpc_out[10]</td>
<td>Pulse output pattern table</td>
<td>H'000A00</td>
<td>H'18, H'08, H'0C, H'04, H'06, H'02, H'03, H'01, H'11, H'10</td>
</tr>
</tbody>
</table>
5. Flowcharts

5.1 Main Routine

```
main

Set the I bit to 1 to disable interrupts.

h8s_sysinit()

init_tmrg()

init_dtc()

init_port_gr()

Clear IMFA in TRGSR to 0. Interrupt request from the IMFA flag is cleared.

Set IMIEA in TRGIER to 1. Interrupt corresponding to the IMFA flag is enabled.

Set STR in TRGMDR to 1. Timer RG starts counting.
```
5.2 System Initialization Routine

Set MSTWDT in MSTR1 to 0. WDT is released from module standby.

Set B4WI and TCSRWE in TCSRWD to 0 and 1, respectively. Writing to TMWLOCK and TMWI in TCSRWD is enabled.

Set TMWLOCK and TMWI in TCSRWD to 0. Writing to TMWD is enabled.

Set the CKS[3:0] bits in TMWD to B'0111.* Clock input to the WDT module is disabled. (WDT is halted.)

Writing the bit-wise inverse of the value set in * above makes the value set in * effective.

Set the CKS[3:0] bits in TMWD to B'1000. Writing to TMWLOCK and TMWI in TCSRWD is disabled.

Set B4WI and TCSRWE in TCSRWD to 0. Writing to TMWLOCK and TMWI in TCSRWD is disabled.

Set the φosc oscillation settling time in the active bits of OSCCSR. Set the bits so that the waiting time will be at least 6.5 ms given the frequency of the oscillator.

Set the PMRJ[1:0] bits to B'11. The OSC1 and OSC2 functions are selected for pins PJ0/OSC1 and PJ1/OSC2.

Set WI and WE in SYSCCR to 0 and 1, respectively. Writing to bits 5, 4, 2, and 1 in SYSCCR is enabled.

Set PHIHSEL in SYSCCR to 1. φosc is selected as the clock source for φhigh.

Set WI and WE in SYSCCR to 0. Writing to bits 5, 4, 2, and 1 in SYSCCR is disabled.
Set WI and WE in LPCR1 to 0 and 1, respectively.

Set PSCSTP and PHIBSEL in LPCR1 to 0 and 1, respectively.

Set WI and WE in LPCR1 to 0.

Set WI and WE in LPCR2 to 0 and 1, respectively.

Set the PHI[2:0] bits in LPCR2 to B'000.

Set WI and WE in LPCR2 to 0.

Set the PHIS[2:0] bits in LPCR3 to B'000.

Set WI and WE in LPCR3 to 0.

Set MSTDTC in MSTCR1 to 0.

Set MSTTMRG in MSTCR3 to 0.

return
5.3 Timer RG Setting Routine

```
init_tmrg

Set STR, MDF, and PWM in TRGMDR to 0.

In TRGCR, set the CCLR[1:0] bits to B'01 and the TPSC[2:0] bits to B'000.

In TRGIOR, set IOA2 to 0 and the IOA[1:0] bits to B'00.

Set GRA to SET_GRA.

Set TRGCNT to H'0000.

return
```

Counting by TRGCNT is halted and timer mode selected.

Clearing of TRDCNT on matches with GRA and counting cycles of the internal φ clock are selected.

The GRA functions as a compare match register and output on pins in response to compare match is disabled.

Period of counting by TRGCNT is set to 1 ms.

TRGCNT is initialized.
5.4 DTC Setting Routine

- **init_dtc**

- In MRA, set the SM[1:0] bits to B'10, the DM[1:0] bits to B'00, the MD[1:0] bits to B'01, DTS to 1, and Sz to 0.

- The following settings are made: repeat mode, incremented transfer source address, fixed transfer destination address, and byte-size transfer.

- Address where the pulse output pattern table starts is specified as the transfer source address.

- Transfer destination address is set to PDBF1.

- The setting for number of unit transfers is 10.

- Transfer counter is set to 10.

- Compare match A interrupt signal from timer RG is specified as the source for DTC activation.

- Following settings are made: chained transfer is not performed, and interrupt requests are generated to the CPU only when specified data transfer is completed.

- Set ITGMA in DTCERH to 1.

- Set SAR to the start address of tpc_out[ ].

- Set DAR to the address of PDBF1.

- Set CRAH to TPC_OUT_NUM.

- Set CRAL to TPC_OUT_NUM.

- Set CHNE and DISEL in MRB to 0.

- **return**
5.5 Event Linkage Setting Routine

```
init_port_gr

In PDR3, set PDR34, PDR33, PDR32, PDR31, and PDR30 to 0.

----------
P30 to P34 are set to "L".

In PCR3, set PCR34, PCR33, PCR32, PCR31, and PCR30 to 1.

----------
Output operation is specified for P30 to P34.

In PGR1, set PGR14, PGR13, PGR12, PGR11, and PGR10 to 1.

----------
P30 to P34 are specified as members of port group 1.

Set PDBF10 to PDBF14 to B'10000.

----------
Initial value to be transferred to PDR30 to PDR34 is set.

Set the PGCO[2:0] bits in PGC1 to B'011.

----------
When the event signal corresponding to operation of port group 1 is input, output of the buffer value is the response.

Set ELSR14 to H'23.

----------
The compare match A signal from timer RG is selected as the event signal to be linked with output port group 1.

Set ELCON in ELCR to 1.

----------
Linkage of all events is enabled.

return
```
6. Program Listing

/*************************************************************************
/*  H8S/2000 Tiny Series -H8S/20203-                                     */
/*  Application Note                                                     */
/*  */
/*  start TPC (output group port 1, DTC, Timer RG)                       */
/*  */
/*  Function                                                           */
/*  : start TPC (output group port 1 by Timer RG compare match A,       */
/*  and DTC by Timer RG compare match A interrupt                      */
/*  Event Link output group port 1 and Timer RG                        */
/*  */
/*  External Clock : 20 MHz                                            */
/*  Internal Clock : 20 MHz                                            */
/*************************************************************************/
#include <machine.h>
#include "iodefine.h"

typedef struct
{
    union{
        unsigned char MRA;        /* DTC mode register A */
        struct{
            unsigned long dummy1:8;    /* dummy1 data (MRA address) */
            unsigned long SAR:24;    /* DTC source address register */
        }SAR;
    }UN_MRA_SAR;

    union{
        unsigned char MRB;        /* DTC mode register B */
        struct{
            unsigned long dummy2:8;    /* dummy2 data (DAR address) */
            unsigned long DAR:24;    /* DTC destination address register */
        }DAR;
    }UN_MRB_DAR;

    struct{
        unsigned char CRAH;       /* DTC transfer count register AH */
        unsigned char CRAL;       /* DTC transfer count register AL */
    }CRA;

    unsigned short CRB;         /* DTC transfer count register B */
} st_dtc_reg;
/*****************************************************************************/
/* Definition of const data */
/* *****************************************************************************/
#define TPC_OUT_NUM 10   /* TPC output number */

/* Timer RG */
/* (Phi=20MHz, divide 1) */
#define SET_GRA 0x4E1F   /* Set GRA (1 ms) */

/* set PDBF1 table (TPC output) */
const unsigned char tpc_out[TPC_OUT_NUM] = {
    0x18, 0x08, 0x0C, 0x04, 0x06,
    0x02, 0x03, 0x01, 0x11, 0x10
};

/*****************************************************************************/
/* Declaration of function prototype */
/*****************************************************************************/
void main(void);
void init_tmrg(void);
void init_dtc(void);
void init_port_gr(void);
void h8s_sysinit(void);

/*****************************************************************************/
/* Definition of RAM area */
/*****************************************************************************/
#pragma section DTC
st_dtc_reg DTC_REG;             /* DTC register */

#pragma section
void main(void)
{
    set_ccr(0x80); /* set CCR-Ibit */
    h8s_sysinit(); /* initialize system */
    init_tmrg(); /* initialize timer RG */
    init_dtc(); /* initialize DTC */
    init_port_gr(); /* initialize port group */
    TRG.TRGSR.BYTE &= 0xE0; /* clear IMFA flag */
    TRG.TRGIER.BYTE = 0xF1; /* interrupt enable by IMFA flag */
    TRG.TRGMDR.BIT.STR = 1; /* TRGCNT start */
    while(1);
}

void init_tmrg(void)
{
    TRG.TRGMDR.BYTE = 0x40; /* select normal mode, TRGCNT stop */
    TRG.TRGCR.BYTE = 0xA0; /* TRGCNT clear when compare match GRA */
    /* clock source Phi */
    TRG.TRGIOR.BYTE = 0x00; /* select compare match register GRA */
    TRG.GRA = SET_GRA; /* set GRA */
    TRG.TRGCNT = 0x0000; /* clear TRGCNT */
}
void init_dtc(void)
{
    DTC_REG.UN_MRA_SAR.MRA = 0x86;     /* repeat mode, SAR increment, DAR hold */
    /* Set source to repeat area */
    /* transfer byte size */

    DTC_REG.UN_MRA_SAR.SAR.SAR = (unsigned long)&tpc_out;   /* Forwarding former address */
    DTC_REG.UN_MRB_DAR.DAR.DAR = (unsigned long)&ELC.PDBF1.BYTE;  /* Address at forwarding destination */
    DTC_REG.CRA.CRAH = TPC_OUT_NUM;     /* Set transfer counter keep */
    DTC_REG.CRAL = TPC_OUT_NUM;         /* Set transfer counter */

    DTC.DTCERH.BIT.ITGMA = 1;           /* DTC start by Timer RG compare match A */
    DTC_REG.UN_MRB_DAR.MRB = 0x00;     /* disable chain, interrupt transfer end */
}

void init_port_gr(void)
{
    IO.PDR3.BYTE = 0x00;        /* P34-P30 "L" */
    IO.PCR3.BYTE = 0x1F;        /* output P34-P30 */

    /* Set event link, Timer RG compare match A */
    ELC.PGR1.BYTE = 0x1F;       /* output port group P34-P30 */
    ELC.PDBF1.BYTE = 0x10;      /* output port group P34:P30(B'10000) */
    /* TPC initialize output */
    ELC.PGC1.BYTE = 0xB9;       /* output PDBF->PDR when event input */
    ELC.ELSR14.BYTE = 0x23;
    ELC.ELCR.BIT.ELCON = 1;     /* event link enable */
}
void h8s_sysinit(void)
{
    MSTCR1.BIT.MSTWDT = 0;          /* WDT module standby off */

    /* stop WDT */
    WDT.TCSRWD.BYTE = 0x97;          /* write enable TMWLOCK, TMWI */
    WDT.TCSRWD.BYTE = 0xA3;          /* write enable TMWD */
    WDT.TMWD.BYTE = 0xF7;           /* Not select clock source */
    WDT.TMWD.BYTE = 0xF8;           /* write bit inversion */
    WDT.TCSRWD.BYTE = 0x87;          /* write disable TMWLOCK, TMWI */

    CPG.OSCCSR.BYTE = 0x0E;          /* wait over 6.5 ms, Phi_osc = 20 MHz */
    PMRJ.BYTE = 0x03;            /* select OSC1, OSC2 */

    CPG.SYSCCR.BYTE = (CPG.SYSCCR.BYTE & 0x7F)| 0x40;   /* WI = 0, WE = 1 */
    CPG.SYSCCR.BYTE = 0x60;          /* high = Phi_osc, Phi_low = Phi_loco */
    CPG.SYSCCR.BYTE = CPG.SYSCCR.BYTE & 0x3F;     /* WI = 0, WE = 0 */

    CPG.LPCR1.BYTE = (CPG.LPCR1.BYTE & 0x7F) | 0x40;     /* WI = 0, WE = 1 */
    CPG.LPCR1.BYTE = CPG.LPCR1.BYTE & 0x3F;      /* WI = 0, WE = 0 */

    CPG.LPCR2.BYTE = (CPG.LPCR2.BYTE & 0x7F) | 0x40;     /* WI = 0, WE = 1 */
    CPG.LPCR2.BYTE = CPG.LPCR2.BYTE & 0x3F;      /* WI = 0, WE = 0 */

    CPG.LPCR3.BYTE = (CPG.LPCR3.BYTE & 0x7F) | 0x40;     /* WI = 0, WE = 1 */
    CPG.LPCR3.BYTE = CPG.LPCR3.BYTE & 0x3F;      /* WI = 0, WE = 0 */

    /* module standby off */
    MSTCR1.BIT.MSTDTC = 0;          /* DTC module standby off */
    MSTCR3.BIT.MSTMRG = 0;          /* Timer RG module standby off */
}

### 6.1 Designation of Linkage Addresses

<table>
<thead>
<tr>
<th>Section Name</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>CDT_C_VECT</td>
<td>H'000400</td>
</tr>
<tr>
<td>PRsetPRG, PIntPRG</td>
<td>H'000500</td>
</tr>
<tr>
<td>P, C, CS$DSEC, CS$BSEC, D</td>
<td>H'000800</td>
</tr>
<tr>
<td>BDTC, B, R</td>
<td>H'FFFF80</td>
</tr>
<tr>
<td>S</td>
<td>H'FFFF80</td>
</tr>
</tbody>
</table>
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