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April 1st, 2010
Renesas Electronics Corporation

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H8/300L Super Low Power Series

Using an Output-Compare Function to Produce PWM Output

Introduction

PWM is output through TMOFH output pin using the output compare function. PWM waveform with the period of 1.64 ms, and with the duty cycle changing by 6.25% between 6.25% and 93.75% is output.

Target Device

H8/38024

Contents

1. Specifications

1. As shown in Figure 1, PWM is output through TMOFH output pin using the Timer F output compare function.
2. The period of PWM waveform to be output is set by the overflow period of the 8-bit timer counter FH (TCFH).
3. The "High" width of PWM waveform to be output is set by the 8-bit output compare register FH (OCRFH).
4. In this sample task, PWM waveform with the period of 1.64 ms, and with the duty cycle changing by 6.25 % between 6.25 % and 93.75 % per every 1 period is output.

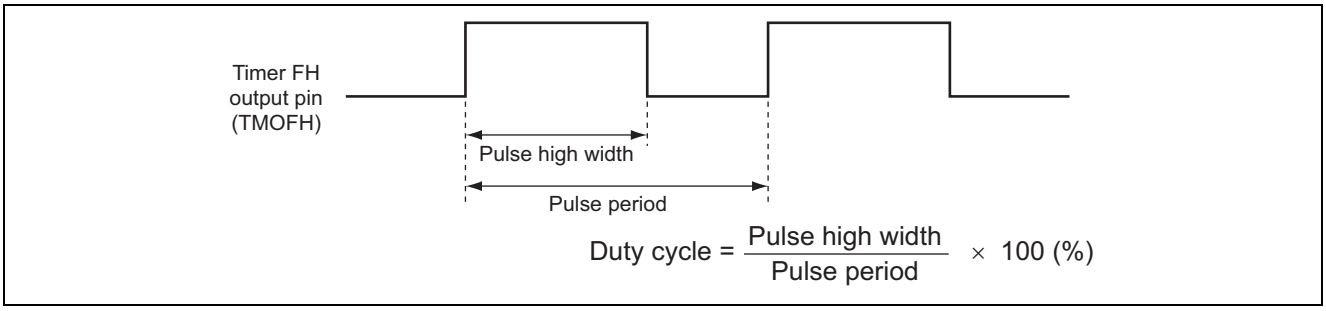


Figure 1 PWM Output

2. Description of Functions Used

1. In this sample task, PWM waveform is output through TMOFH output pin using the Timer F output compare function.
   a. Figure 2 shows the block diagram of the output compare function of Timer F which is described below.
      - The system clock (ϕ) is a 5-MHz clock and is a reference clock to operate the CPU and its peripheral functions.
      - The Prescaler S (PSS) is a 13-bit counter using ϕ as its input clock and is counted up every cycle.
      - The Timer Counter FH (TCFH) is an 8-bit read/write up-counter and is counted up by an internal or external clock which is input. The input clock can be selected from one external clock and three clocks obtained by dividing ϕ.
      - The Timer Control Register F (TCRF) is an 8-bit write-only register. It selects an input clock to TCFH and sets the output level of TMOFH pin. In this sample task, a clock obtained by dividing ϕ by 32 is selected as the TCFH input clock and the output level of TMOFH pin is set to high level.
      - The Timer Control/Status Register F (TCSRF) is an 8-bit register which selects counter clear, sets compare match flag, sets timer overflow flag, and controls enable/disable of overflow interrupt request. In this sample task, clearing TCFH by compare match FH is disabled, and FH overflow interrupts are enabled.
      - The Output Compare Register FH (OCRFH) is an 8-bit read/write register, and the data of OCRFH is always compared with that of TCFH. When the values of both registers match, the compare match FH is generated and the toggle signal is output from TMOFH pin.
      - The data of TCFH is constantly compared with that of OCRFH, and when they match the compare match flag H (CMFH) is set to 1 and an interrupt is requested to CPU at this time.
      - PWM waveform is output through Timer FH output pin (TMOFH).

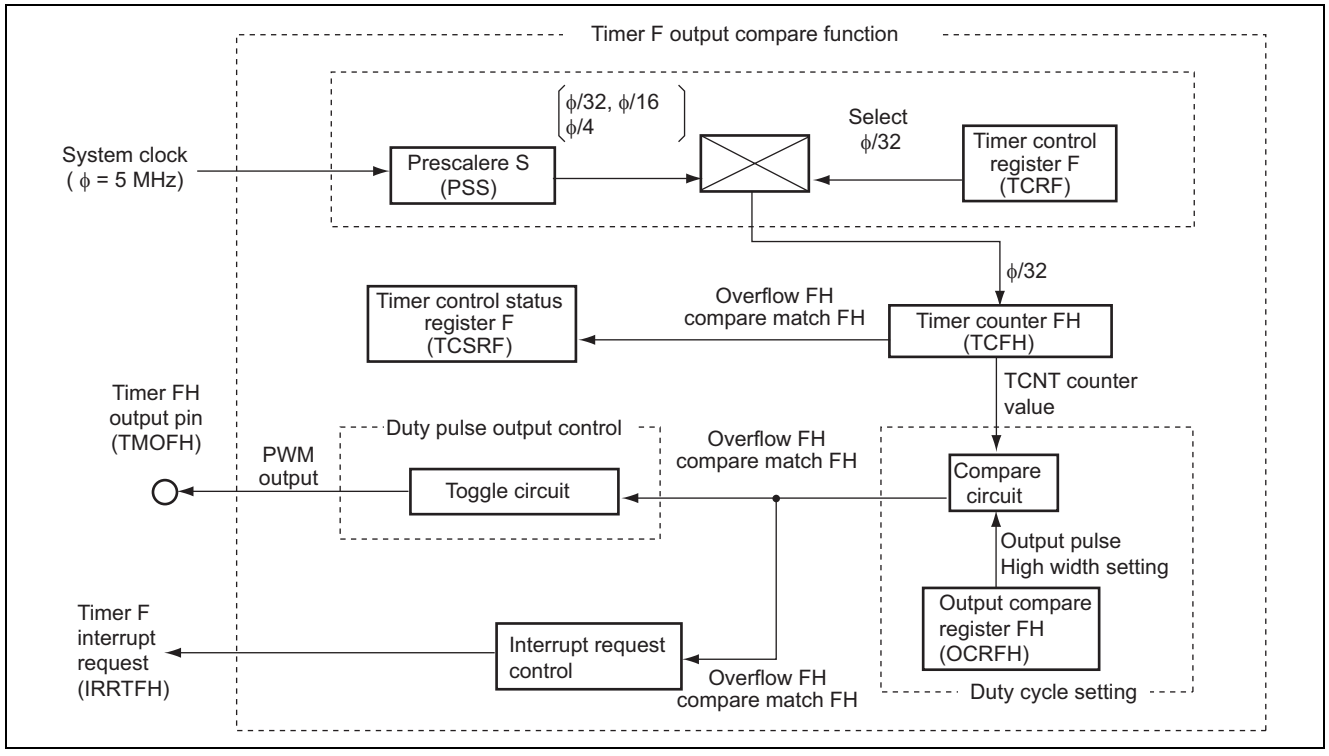


Figure 2 Block Diagram of Timer F output compare function

b. Figure 3 shows the method to set a period and duty cycle of PWM waveform output in this sample task.

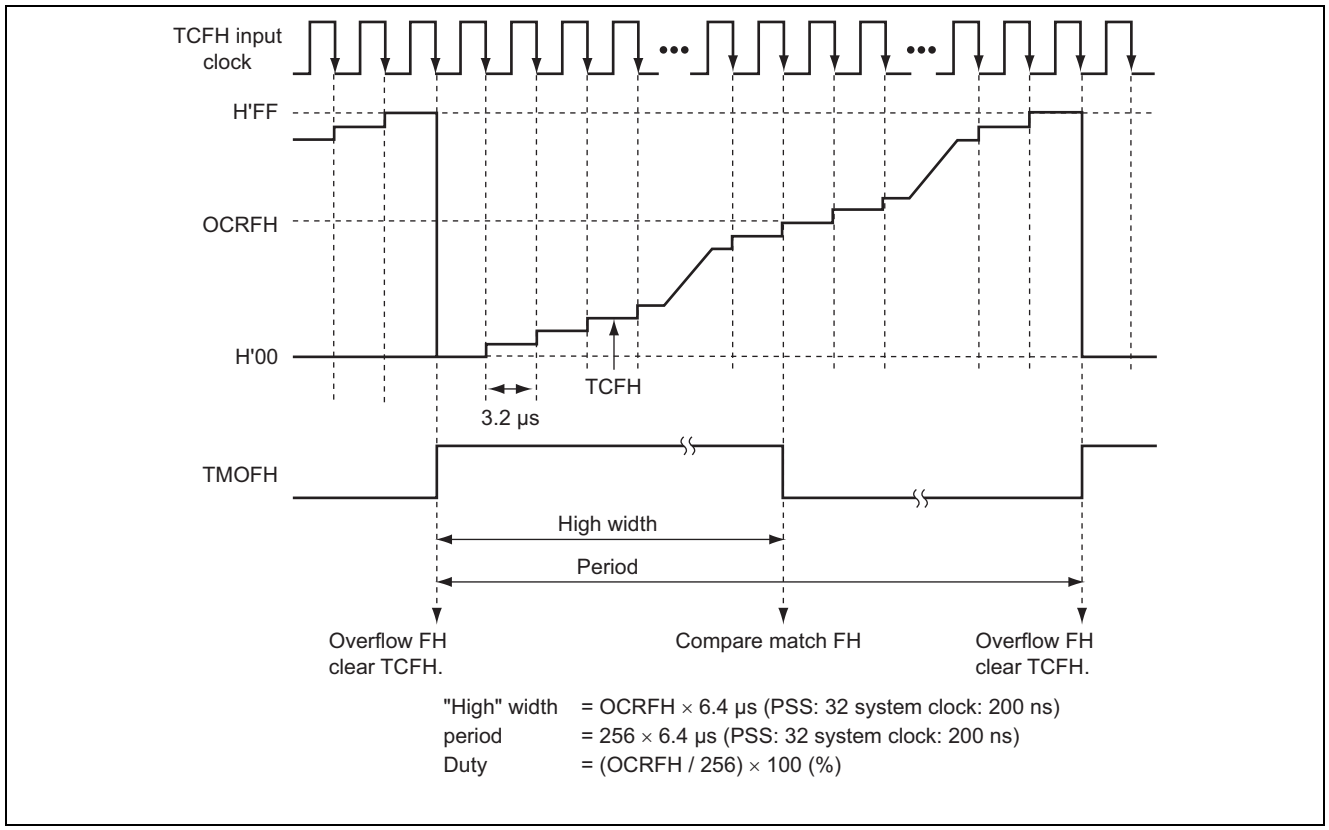


Figure 3 Method to Set Period and Duty of PWM Waveform Output

c. Figure 4 shows the timing for rewriting OCRFH to increase the duty cycle.

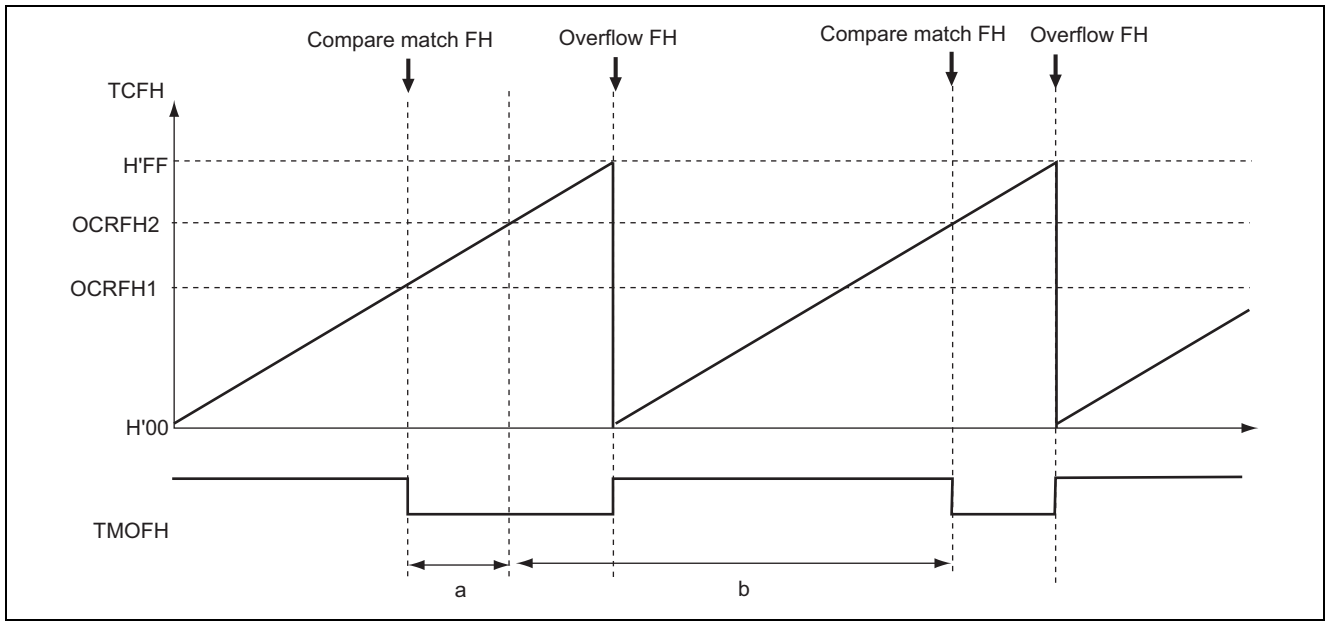


Figure 4 Timing for Rewriting OCRFH to Increase the Duty Cycle

- The contents of OCRFH are updated simultaneously when it is written to OCRFH. In the case of increasing the duty cycle, if OCRFH is rewritten during the period a in figure 4, compare match FH occurs consecutively before an overflow interrupt occurs, and PWM waveform is not output correctly. Therefore the timing for rewriting OCRFH must be during the period b in figure 4.
- In this sample task, OCRFH is rewritten during the overflow FH interrupt handling.

d. Figure 5 shows the timing for rewriting OCRFH to decrease the duty cycle.

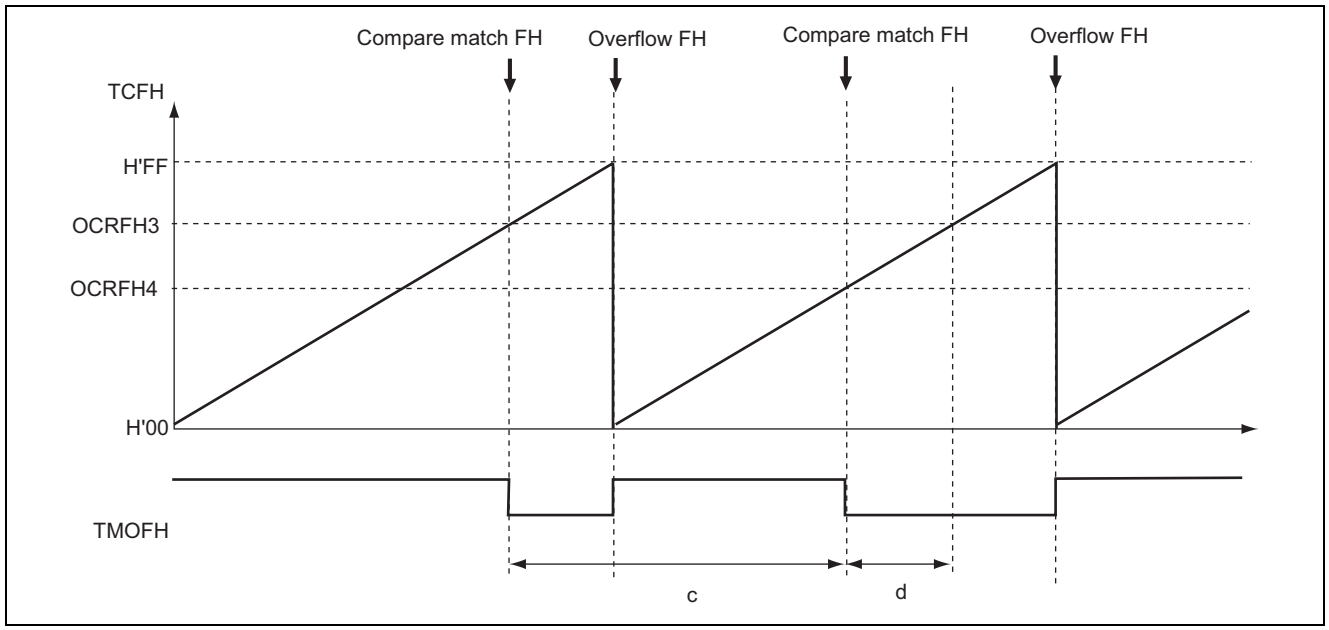


Figure 5 Timing for Rewriting OCRFH to Decrease the Duty Cycle

- The contents of OCRFH are updated simultaneously when it is written to OCRFH. In the case of decreasing the duty cycle, if OCRFH is rewritten during the period d in figure 5, the next compare match FH does not occur consecutively, and PWM waveform is not output correctly. Therefore the timing for rewriting OCRFH must be during the period c in figure 5.
- In this sample task, OCRFH is rewritten during the overflow FH interrupt handling.

2. Table 1 shows function assignment in this sample task. The functions are assigned as shown in Table 1 and PWM is output by the Timer F output compare function.

Table 1 Assignment of Functions

Function	Assignment
PSS	A 13-bit up-counter using the system clock as input
IENTFH	Selects enable/disable of Timer FH interrupt request
IRRTFH	Timer FH interrupt request flag
TCRF	Selects output level of TCFH and selects input clock.
TCSRF	Enables TCFH overflow interrupts and selects clearing TCFH by compare match FH
TCFH	An 8-bit counter using the system clock/32 as input
OCRFH	Sets the high width of PWM output
TMOFH	PWM output pin

3. Principle of Operation

1. Figure 6 illustrates the principle of operation of this sample task. As shown in figure 6, PWM is output by the Timer F output compare function by means of hardware processing and software processing.

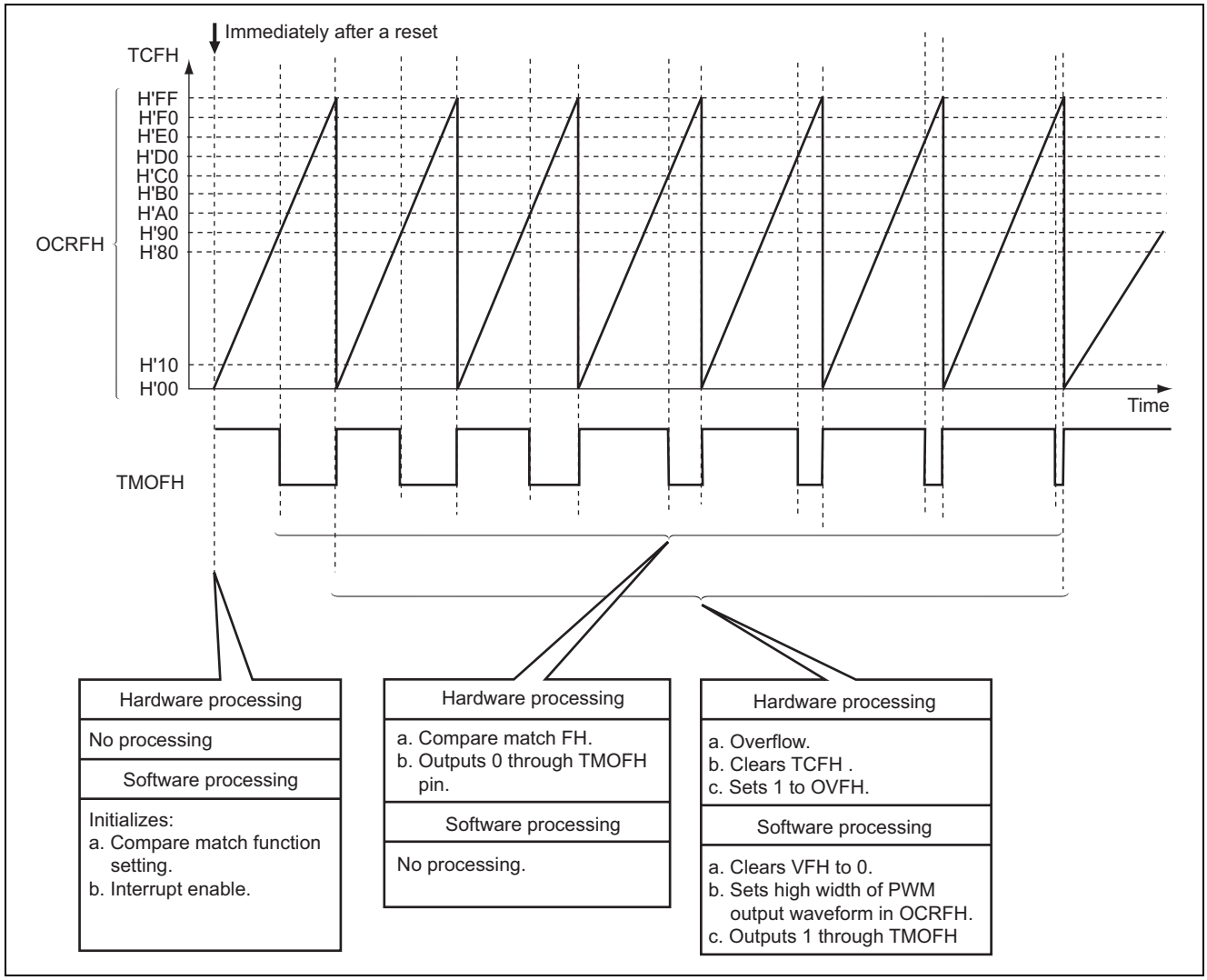


Figure 6 Operation Principle of PWM Output by Timer F Output Compare Function

4. Description of Software

4.1 Modules

Table 2 describes the modules in this sample task.

Table 2 Description of Modules

Module	Label	Function
Main Routine	main	Sets the output compare match function, and enables interrupts.
Change of PWM waveform	tfint	During Timer F interrupt handling routine, rewrites OCRFH in the case of overflow interrupt (CNTF0 = 1), or sets CNTF0 to 1 in the case of compare match interrupt (CNTF0 = 0), and stops the interrupt handling operation.

4.2 Arguments

Arguments are not used in this sample task.

4.3 Internal registers

Table 3 describes the internal registers in this sample task.

Table 3 Description of Internal Registers

Register		Function	Address	Setting
IENR2	IENTFH	Interrupt Enable Register 2 (Timer FH Interrupt Enable) When IENTFH = 0, Timer FH interrupt requests are disabled. When IENTFH = 1, Timer FH interrupt requests are enabled.	H'FFF4 Bit 3	1
IRR2	IRRTFH	Interrupt Request Register 2 (Timer FH Interrupt Request Flag) When IRRTFH = 0, a Timer FH interrupt is not requested. When IRRTFH = 1, a Timer FH interrupt is requested.	H'FFF7 Bit 3	0
TCRF	TOLH	Timer Control Register F (Toggle output level H) When TOLH = 0, the output level of TMOFH pin is set to High. When TOLH = 1, the output level of TMOFH pin is set to Low.	H'FFB6 Bit 7	1
	CKSH2 CKSH1 CKSH0	Timer Control Register F (Clock Select H) When CKSH2 = 1, CKSH1 = 0 and CKSH0 = 0, TCFH is counted by system clock/32.	H'FFB6 Bit 6 Bit 5 Bit 4	CKSH2 = 1 CKSH1 = 0 CKSH0 = 0

Register		Function	Address	Setting
TCSRF	OVFH	Timer Control/Status Register F (Timer Overflow Flag H) When OVFH = 0, TCFH has not overflowed. When OVFH = 1, TCFH has overflowed.	H'FFB7 Bit 7	0
	CMFH	Timer Control/Status Register F (Compare Match Flag H) When CMFH = 0, compare match FH has not occurred. When CMFH = 1, compare match FH has occurred.	H'FFB7 Bit 6	0
	OVIEH	Timer Control/Status Register F (Timer Overflow Interrupt Enable H) When OVIEH = 0, overflow FH interrupt requests are disabled. When OVIEH = 1, overflow FH interrupt requests are enabled	H'FFB7 Bit 5	1
	CCLRH	Timer Control/Status Register F (Counter Clear H) When CCLRH = 0, clearing TCFH by compare match FH is disabled. When CCLRH = 1, clearing TCFH by compare match FH is enabled	H'FFB7 Bit 4	0
TCFH		Timer Counter FH An 8-bit up-counter using system clock/32 as input clock.	H'FFB8	H'00
OCRFH		Output Compare Register FH When OCRFH = H'80, counter value of TCFH counts to H'80, and compare match FH is generated.	H'FFBA	H'80
PMR3	TMOFH	Port Mode Register 3 (P32/TMOFH pin function switch) When TMOFH = 1, P32/TMOFH pin function is set to TMOFH output pin.	H'FFCA Bit 2	1

4.4 RAM

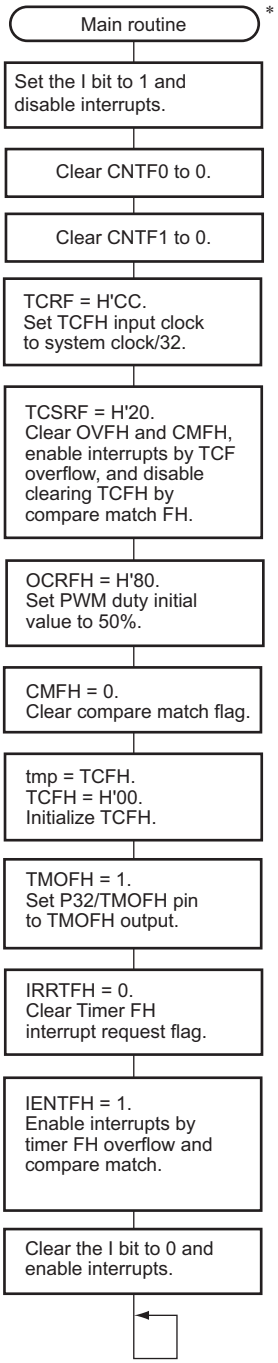
Table 4 describes the RAMs used in this sample task.

Table 4 Description of RAM Used

Label		Function	Address	Used in
USRF	CNTF0	A flag to indicate whether an interrupt is requested by overflow or compare match.	H'FB80 Bit 0	Main Routine PWM waveform change
	CNTF1	A flag to indicate whether to increment or decrement the value of OCRFH.	H'FB80 Bit 1	Main Routine PWM waveform change

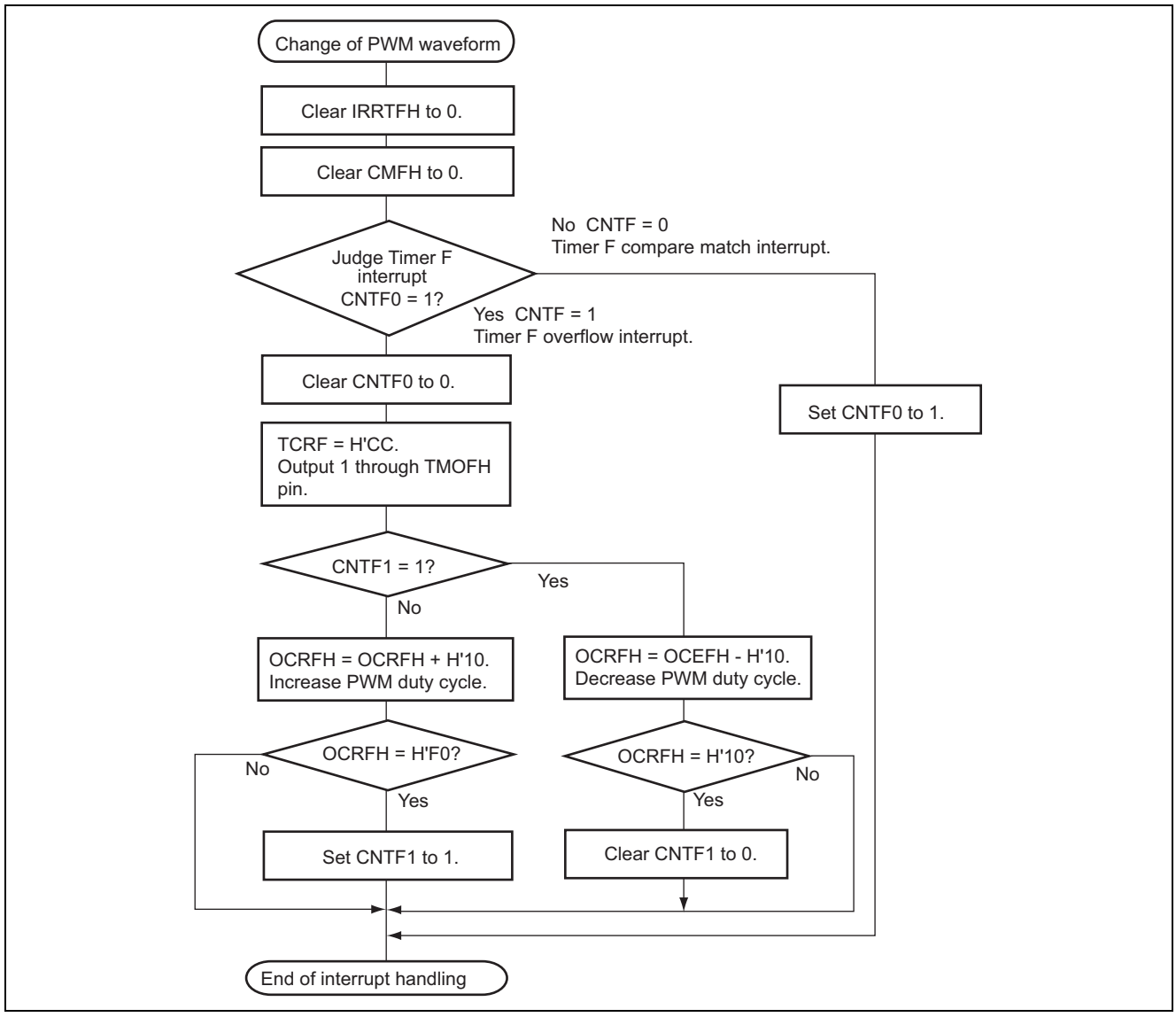
5. Flowchart

1. Main routine



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

2. Timer F Overflow Interrupt routine



6. Program Listing

INIT.SRC (Program listing)

```
    .EXPORT     _INIT
    .IMPORT     _main
;
    .SECTION    P,CODE
_INIT:
    MOV.W       #H'FF80,R7
    LDC.B       #B'10000000,CCR
    JMP         @_main
;
    .END
```

```
/************************************************************************************************/
/*                                                                                              */
/*  H8/300L Super Low Power Series                                                              */
/*      -H8/38024 Series-                                                                       */
/*  Application Note                                                                            */
/*                                                                                              */
/*  'PWM Output by Compare Match Function'                                                      */
/*                                                                                              */
/*  Function                                                                                    */
/*  :Timer F Compare Match                                                                      */
/*                                                                                              */
/*  External Clock :     10MHz                                                                  */
/*  Internal Clock :     5MHz                                                                   */
/*  Sub Clock :          32.768kHz                                                              */
/*                                                                                              */
/************************************************************************************************/

#include     <machine.h>

/************************************************************************************************/
/*  Symbol Definition                                                                           */
/************************************************************************************************/
struct BIT {
    unsigned char    b7:1;       /* bit7 */
    unsigned char    b6:1;       /* bit6 */
    unsigned char    b5:1;       /* bit5 */
    unsigned char    b4:1;       /* bit4 */
    unsigned char    b3:1;       /* bit3 */
    unsigned char    b2:1;       /* bit2 */
    unsigned char    b1:1;       /* bit1 */
    unsigned char    b0:1;       /* bit0 */
};
```

```
#define      TCRF      *(volatile unsigned char *)0xFFB6   /* Timer Control Register F          */
#define      TCRF_BIT  (*(struct BIT *)0xFFB6)             /* Timer Control Register F          */
#define      TOLH      TCRF_BIT.b7                         /* Toggle Output Level F             */
#define      CKSH2     TCRF_BIT.b6                         /* Clock Select H2                   */
#define      CKSH1     TCRF_BIT.b5                         /* Clock Select H1                   */
#define      CKSH0     TCRF_BIT.b4                         /* Clock Select H0                   */
#define      TCSRF     *(volatile unsigned char *)0xFFB7   /* Timer Control Status Register F   */
#define      TCSRF_BIT (*(struct BIT *)0xFFB7)             /* Timer Control Status Register F   */
#define      OVFH      TCSRF_BIT.b7                        /* Timer Overflow Flag H             */
#define      CMFH      TCSRF_BIT.b6                        /* Compare Match Flag H              */
#define      OVIEH     TCSRF_BIT.b5                        /* Timer Overflow Interrupt Enable   */
#define      CCLRH     TCSRF_BIT.b4                        /* Output Select 3                   */
#define      OCRFH     *(volatile unsigned char *)0Xffba   /* Output Compare Register FH        */
#define      TCFH      *(volatile unsigned char *)0xFFB8   /* Timer Counter FH                  */
#define      IENR2_BIT (*(struct BIT *)0xFFF4)             /* Interrupt Enable Register 2       */
#define      IENTFH    IENR2_BIT.b3                        /* Timer F Interrupt Enable          */
#define      IRR2_BIT  (*(struct BIT *)0xFFF7)             /* Interrupt Request Register 2      */
#define      IRRTFH    IRR2_BIT.b3                         /* Timer F Interrupt Request Flag    */
#define      PMR3_BIT  (*(struct BIT *)0xFFCA)             /* Port Mode Register 3              */
#define      TMOFH     PMR3_BIT.b2                         /* P32/TMOFH Input Select            */

#pragma interrupt(     tfint)
/************************************************************************************************/
/*Function Define                                                                               */
/************************************************************************************************/
extern void  INIT ( void );                                /* SP Set                            */
void         main ( void );
void         tfint ( void );

/************************************************************************************************/
/*  RAM Define                                                                                  */
/************************************************************************************************/
unsigned char    USRF;                                     /* User Flag Erea                    */
#define      USRF_BIT  (*(struct BIT *)&USRF)
#define      CNTF0     USRF_BIT.b0                         /* Counter Flag                      */
#define      CNTF1     USRF_BIT.b1                         /* Counter Flag                      */

/************************************************************************************************/
/*  Vector Address                                                                              */
/************************************************************************************************/
#pragma section  V1                                        /* Vector Section Set                */
void (*const VEC_TBL1[])(void) = {                         /* 0x0000 - 0x000F                   */
    INIT                                                   /* 0x0000 Reset Vector               */
};
#pragma section  V2                                        /* Vector Section Set                */
void (*const VEC_TBL2[])(void) = {
    taint                                                  /* 0x001E Timer F Interrupt Vector   */
};

#pragma section                                            /* P                                 */
```

```
/*****************************************************************************************/
/*  Main Program                                                                         */
/*****************************************************************************************/
void      main ( void )
{
    int tmp;
    set_imask_ccr(1);                                   /* Interrupt Disable            */

    CNTF0  = 0;
    CNTF1  = 0;

    TCRF   = 0xCC;                                      /* Initialize Clock Select      */
    TCSRF  = 0x20;                                      /* Initialize Overflow Interrupt*/

  OCRFH   = 0x80;                                       /* Initialize Compare Match FH Value*/

    CMFH   = 0;                                         /* Clear Compare Match Flag FH  */
    Tmp    = TCFH;                                      /* Dummy Read for Flag Clear    */
    TCFH   = 0;                                         /* Compare Match FH Interrupt Enable*/

    TMOFH = 1;                                          /* P32/TMOFH input select       */

    IRRTFH= 0;                                          /* Clear IRRTFH                 */
    IENTFH = 1;                                         /* Timer FH Interrupt Enable    */

    set_imask_ccr(0);                                   /* Interrupt Enable             */

    while(1);

}

/*****************************************************************************************/
/*  Timer F Overflow Interrupt                                                           */
/*****************************************************************************************/
void      tfint ( void )
{
    int tmp;

    IRRTFH = 0;
    tmp = CMFH;                                         /* Dummy Read for Flag Clear    */
    CMFH = 0;                                           /* Clear CMFH to 0              */

    if ( CNTF0 == 1){                                   /* CNTF0 = 1 ?                  */
          CNTF0 = 0;                                    /* Clear CNTF1 to 0             */
          TCRF  = 0xCC;                                 /* TMOFH High level Output      */

          if ( CNTF1 == 1){                             /* CNTF1 = 1 ?                  */
                OCRFH - = 0x10;                         /* Decrement High Width         */
                if ( OCRFH == 0x10 ){                   /* High Width = H'10 ?          */
                      CNTF1 = 0;                        /* Clear CNTF1 to 0             */
          }
    }
```

```
    else{
          OCRFH + = 0x10;                          /* Increment High Width          */
          if ( OCRFH == 0xF0 ){                    /* High Width = H'F0 ?           */
                CNTF1 = 1;                         /* Set CNTF1 at 1                */
                }
          }
    }
    else{
          CNTF0 = 1;                               /* Set CNTF0 at 1                */
    }
}
```

Link address specifications

Section Name	Address
CV1	H'0000
CV2	H'001E
P	H'0100
B	H'FB80

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
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2.00	Nov.30.06	All pages	Content correction

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