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SH7262/SH7264 Group

Using the Motor Control PWM Timer

Summary

This application note describes an example of using the SH7262/SH7264 motor control PWM timer (PWM timer).

Target Device

SH7264 MCU

As the SH7262 PWM timer output pin is multiplexed with the data bus, the PWM timer can be used in the system not using the data bus.

Contents

1. Introduction

1.1 Specifications

Uses the motor control PWM timer (PWM timer) to output the PWM pulses.

1.2 Modules Used

- Motor control PWM timer (PWM timer)
- Interrupt controller

1.3 Applicable Conditions

MCU	SH7262/SH7264
Operating Frequency	Internal clock: 144 MHz Bus clock: 72 MHz Peripheral clock: 36 MHz
Integrated Development Environment	Renesas Technology Corp. High-performance Embedded Workshop Ver.4.04.01
C compiler	Renesas Technology SuperH RISC engine Family C/C++ compiler package Ver.9.02 Release 00
Compiler options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo)

1.4 Related Application Note

Refer to the related application notes as follows:

- SH7262/SH7264 Group Example of Initialization

2. Applications

The SH7264 PWM timer outputs 4 PWM pulses.

2.1 PWM Timer Operation

PWM timer has following features:

- Up to 16 pulses can be output
  Two channels of 10-bit PWM to output 8 pulses is included
  10-bit counter (PWCNT) and the cycle register (PWCYR) are included
  Duty and output polarity can be set for each pulse
- Data can be automatically transferred every cycle
  Four duty registers (PWDTR) include the buffer registers (PWBFR) to transfer data automatically at every cycle
- Duty cycle can be set
  0% to 100% can be selected for the duty register
- Selectable from five count clocks
  Count clocks can be selected from Pφ, Pφ/2, Pφ/4, Pφ/8, Pφ/16
- High-speed access by the internal 16-bit bus
- Interrupt factors: 2
  Interrupts can be requested to two channels respectively, by the compare match in the cycle register
- Data can be automatically transferred
  Transferring data in blocks or one-word data are enabled by activating the Direct memory access controller (DMAC).
- Module stop mode can be set

Figure 1 shows the block diagram of the PWM timer. Table 1 lists the PWM timer pin configurations.

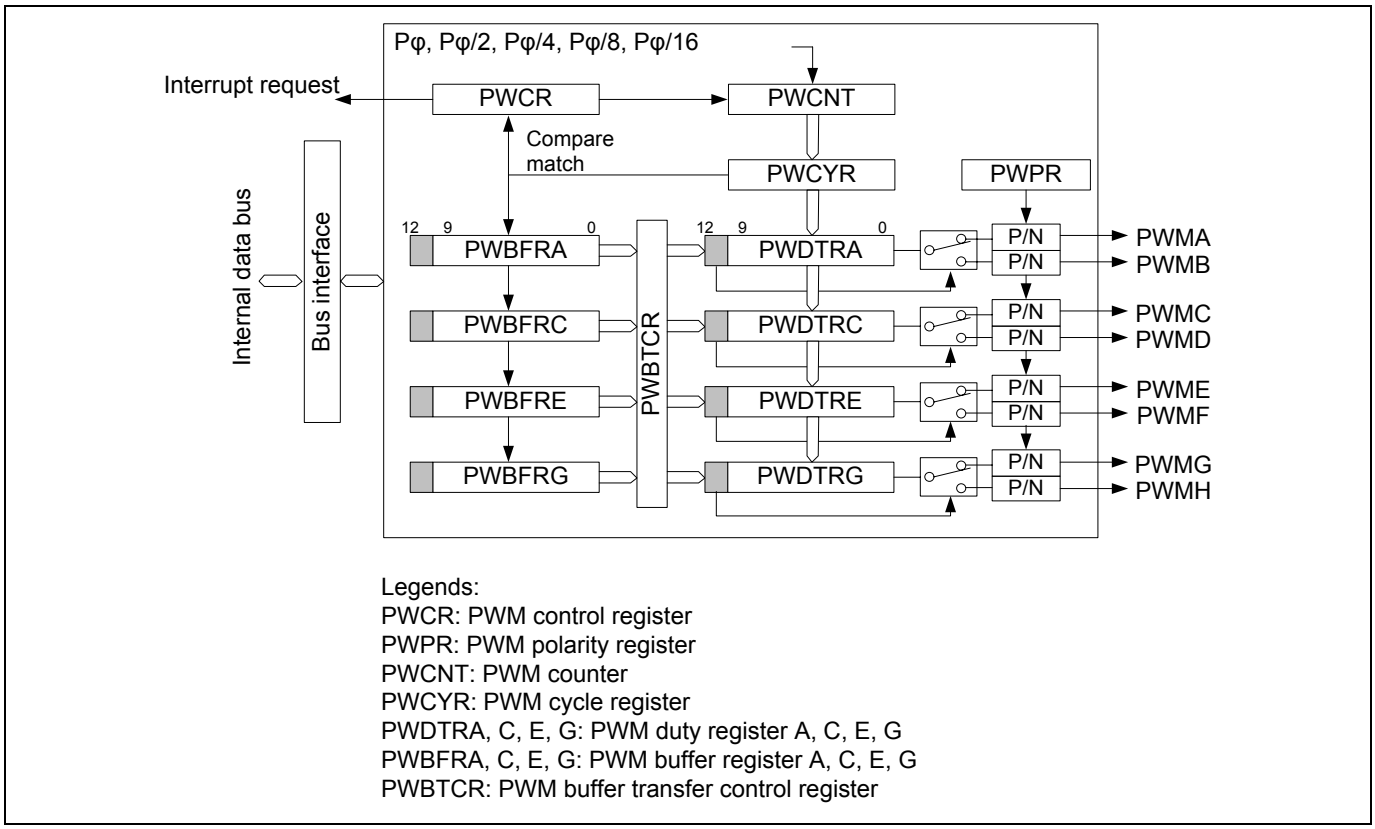

Figure 1 PWM Timer Block Diagram

Table 1 PWM Timer Pin Configurations

Channel	Pin Name	Symbol	I/O	Description
1	PWM output pin 1A	PWM1A	Output	PWM output from channel 1A
	PWM output pin 1B	PWM1B	Output	PWM output from channel 1B
	PWM output pin 1C	PWM1C	Output	PWM output from channel 1C
	PWM output pin1D	PWM1D	Output	PWM output from channel 1D
	PWM output pin 1E	PWM1E	Output	PWM output from channel 1E
	PWM output pin 1F	PWM1F	Output	PWM output from channel 1F
	PWM output pin 1G	PWM1G	Output	PWM output from channel 1G
	PWM output pin 1H	PWM1A	Output	PWM output from channel 1H
2	PWM output pin 2A	PWM2A	Output	PWM output from channel 2A
	PWM output pin 2B	PWM2B	Output	PWM output from channel 2B
	PWM output pin 2C	PWM2C	Output	PWM output from channel 2C
	PWM output pin 2D	PWM2D	Output	PWM output from channel 2D
	PWM output pin 2E	PWM2E	Output	PWM output from channel 2E
	PWM output pin 2F	PWM2F	Output	PWM output from channel 2F
	PWM output pin 2G	PWM2G	Output	PWM output from channel 2G
	PWM output pin 2H	PWM2A	Output	PWM output from channel 2H

Figure 2 shows the PWM timer operation.

The PWM counter (PWCNT), a 10-bit up-counter, counts the PWM timer. Set the count clock by the PWM control register (PWCR).

The PWM cycle register (PWCYR) setting decides the cycle to convert PWM. Lower 10 bits of the PWCYR register is valid. When the compare match occurs between the PWCNT and PWCYR registers, the setting in the PWM buffer register n [n = A,C, E, G] (PWBFRn [n = A, C, E, G]) is transferred to the PWM duty register n [n = A, C, E, G] (PWDTRn [n = A, C, E, G]), and starts outputting the PWM waveform according to the value in the PWDTRn [n = A, C, E, G]. The compare match interrupt occurs at this timing.

The PWBFRn [n = A, C, E, G] register and the PWM polarity register (PWPR) setting decide the PWM duty cycle.

The PWBFRn [n = A, C, E, G] register has the OTS and DTn [n = 1 to 9] bits. OTS bit selects the pin to output high-level signals. When the OTS bit in the PWBFRA register is 0, the OTS bit selects the PWMA pin. When the OTS bit is 1, it selects the PWMB pin. The OTS bit in the PWBFRC register selects either PWMC pin or PWMD pin.

DTn [n = 1 to 9] bits specify the period to output high-level signals. The period to output high level signals is from the compare match between the PWCNT and PWCYR register to the compare match between the PWCNT register and DTn [n = 1 to 9]. The pins not selected by the OTS bit output low-level signals.

When setting the OPSn [n = A to H] bit as 1, the corresponding pin is inverted to output signals.

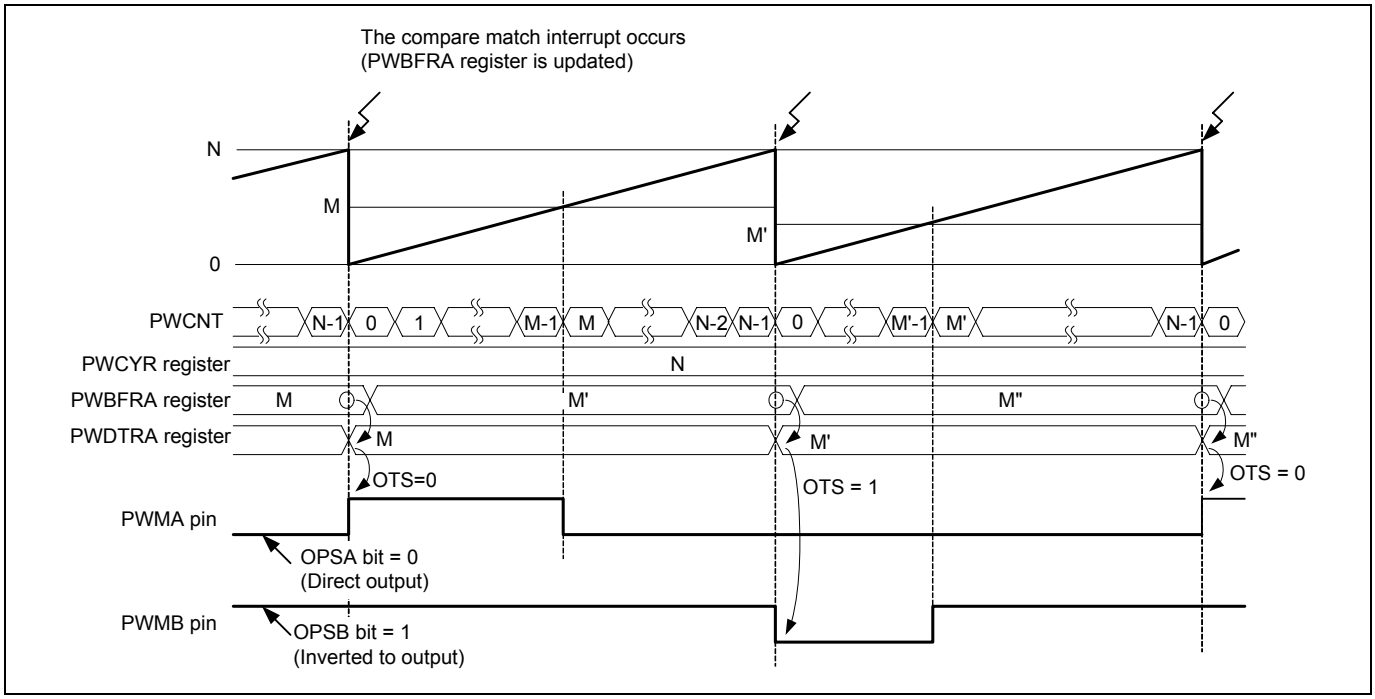

Figure 2 PWM Timer Operation

2.2 PWM Timer Setting Procedure

Figure 3 shows the flow chart of setting the PWM timer. This example enables the compare match interrupt by channel 1 of the PWM timer. For details on the registers, refer to the "SH7262, SH7264 Group, Hardware manual".

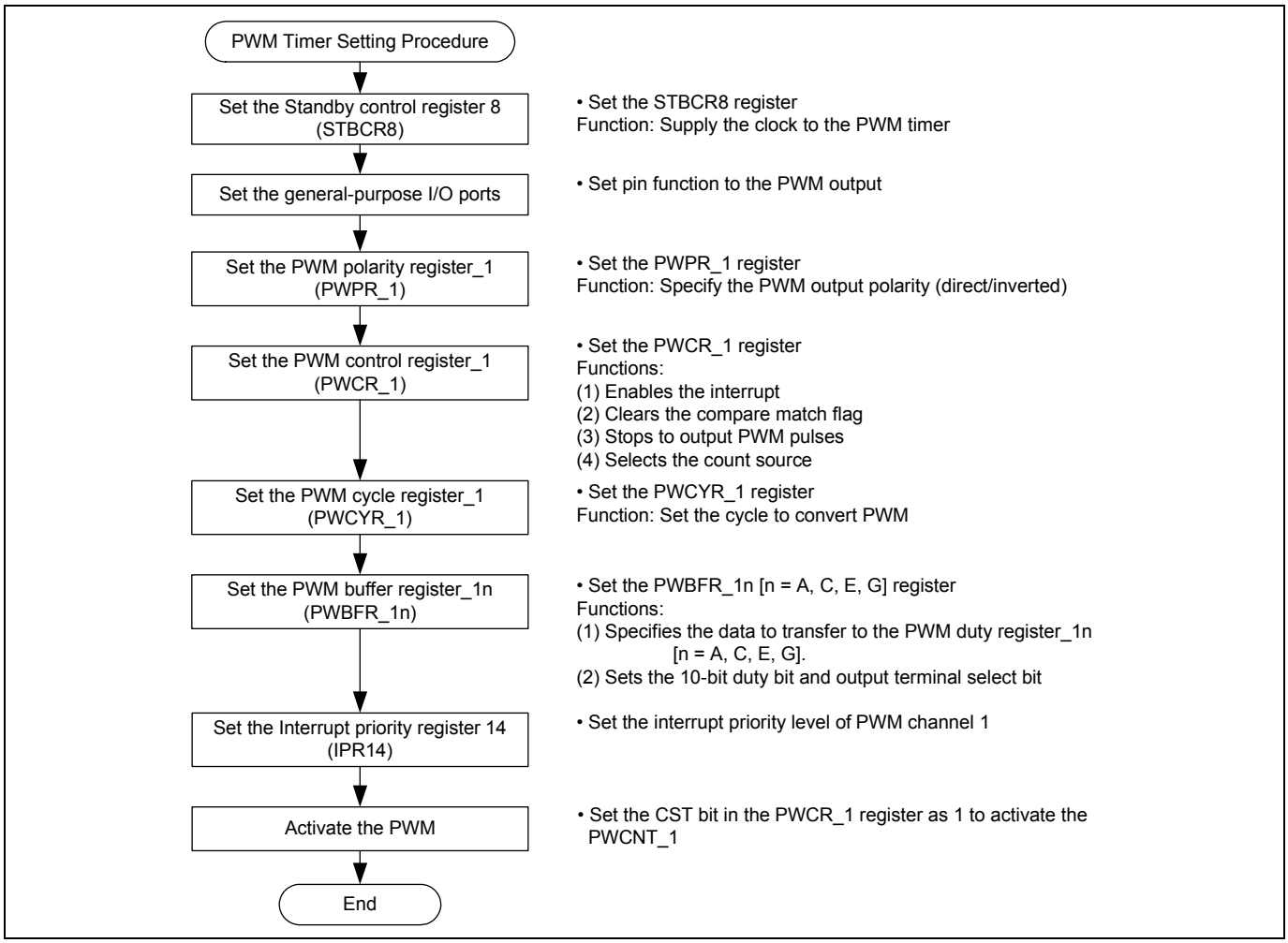

Figure 3 PWM Timer Setting Flow Chart

2.3 Sample Program Operation

The PWM timer outputs the PWM pulse from PWM1A to PWM1D pins (four pins) in the sample program. The compare match interrupt updates the PWM buffer register, however, duty bit setting in the PWM buffer register is set in main function.

PWM timer setting in the sample program is as follows:

- Channel to use: channel 1
- Output pins: PWM1A, PWM1B, PWM1C, PWM1D
- Update procedure of the PWM buffer register: CPU transfer by the compare match interrupt
- Cycle to convert PWM: 200 µs (Actual PWM cycle to output signals from two pins alternately is 400 µs)
- Duty cycle: 0%, 10%, 20%, 30%, 40% (Duty cycles for inverted output pin are 100%, 90%, 80%, 70%, 60%)
- Polarity: Direct (PWM1A and PWM1C pins), inverted (PWM1B and PWM1D pins)

Figure 4 shows the PWM output waveform in the sample program.

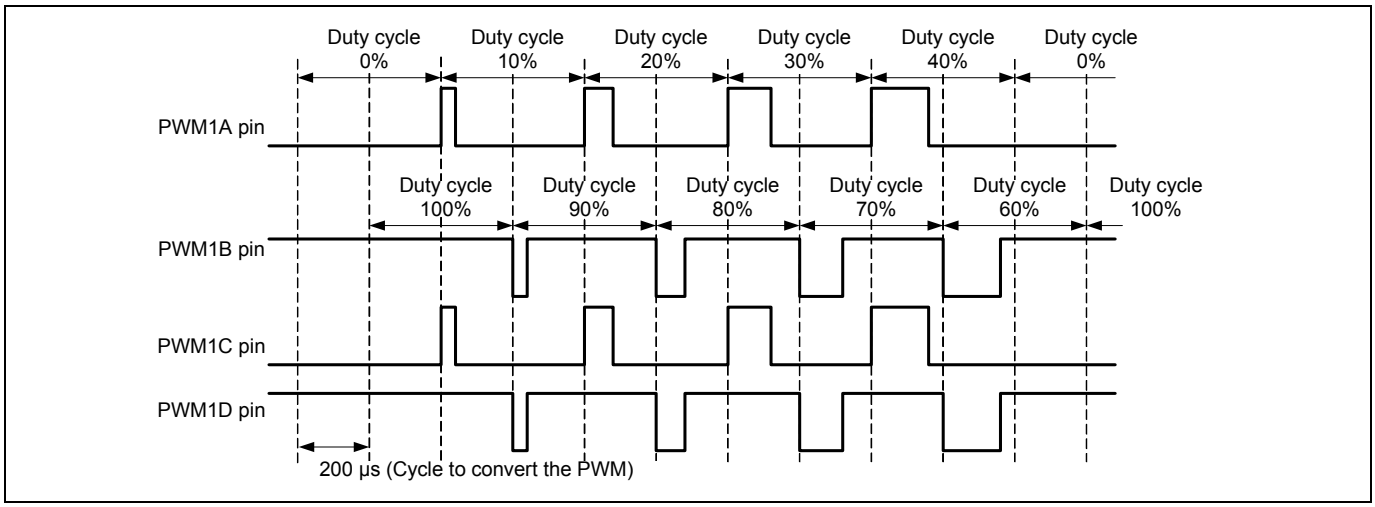

Figure 4 PWM Output Waveform in the Sample Program

2.4 Sample Program Procedure

Table 2 lists the registers setting in the sample program.

Table 2 Register Setting

Register Name	Address	Setting	Description
Standby control register 8 (STBCR8)	H'FFFE 041C	MSTP87 bit = 0	• Supplies the clock to the PWM timer
Port K control register 0 (PKCR0)	H'FFFE 392E	PK0MD bit = 1 PK1MD bit = 1 PK2MD bit =1 PK3MD bit =1	• Sets the functions of the PWM1A, PWM1B, PWM1C, and PWM1D pins (Port K can be used with the SH7264 only)
PWM polarity register_1 (PWPR_1)	H'FFFE F4E4	OPS1A bit = 0 OPS1B bit = 1 OPS1C bit = 0 OPS1D bit = 1	• PWM1A and PWM1C pins output direct • PWM1B and PWM1D pins output inverted
PWM control register_1 (PWCR_1)	H'FFFE F4E0	H'E4	• Stops counting thePWCNT_1 register • Enables the compare match interrupt • Clears the compare match flag (Read the status of 1, then write 0) • Specifies the counter clock as Pφ/16
		H'EC	• Starts counting the PWCNT_1 register
PWM cycle register_1 (PWCYR_1)	H'FFFE F4E6	450	• Specifies the cycle to convert the PWM as 200 µs 200 µs = 27.8 ns × 16 × 450 (Pφ = 36 MHz)
PWM buffer register_1A (PWBFR_1A)	H'FFFE F4E8	H'0000	• OTS bit = 0: Selects the PWM1A pin • DTn [n = 0 to 9] bits = 0: High-level output period 0
PWM buffer register_1C (PWBFR_1C)	H'FFFE F4EA	H'0000	• OTS bit = 0: Selects the PWM1C pin • DTn [n = 0 to 9] bits = 0: High-level output period 0
Interrupt priority register 14 (IPR14)	H'FFFE 0C10	PWM1 bit = 5	• Sets the interrupt priority level of the PWM timer channel 1 as 5

Figure 5 shows the flow chart of the main function. Figure 6 shows the flow chart of the compare match interrupt.

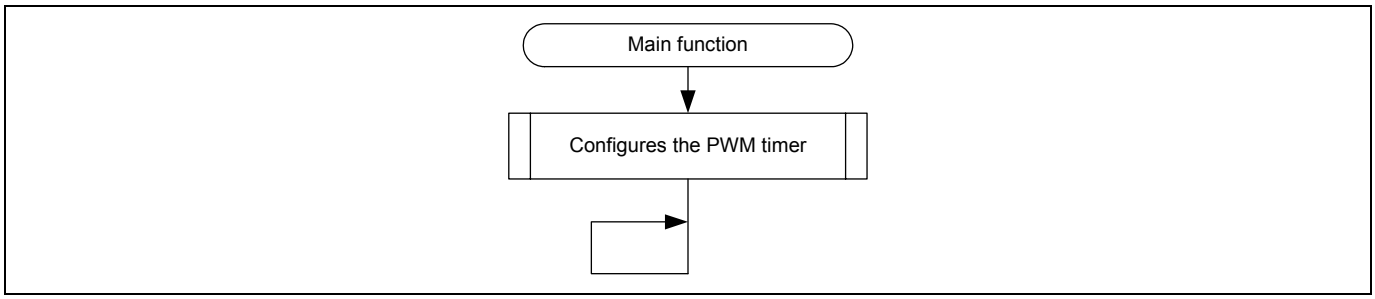

Figure 5 Main Function Flow Chart

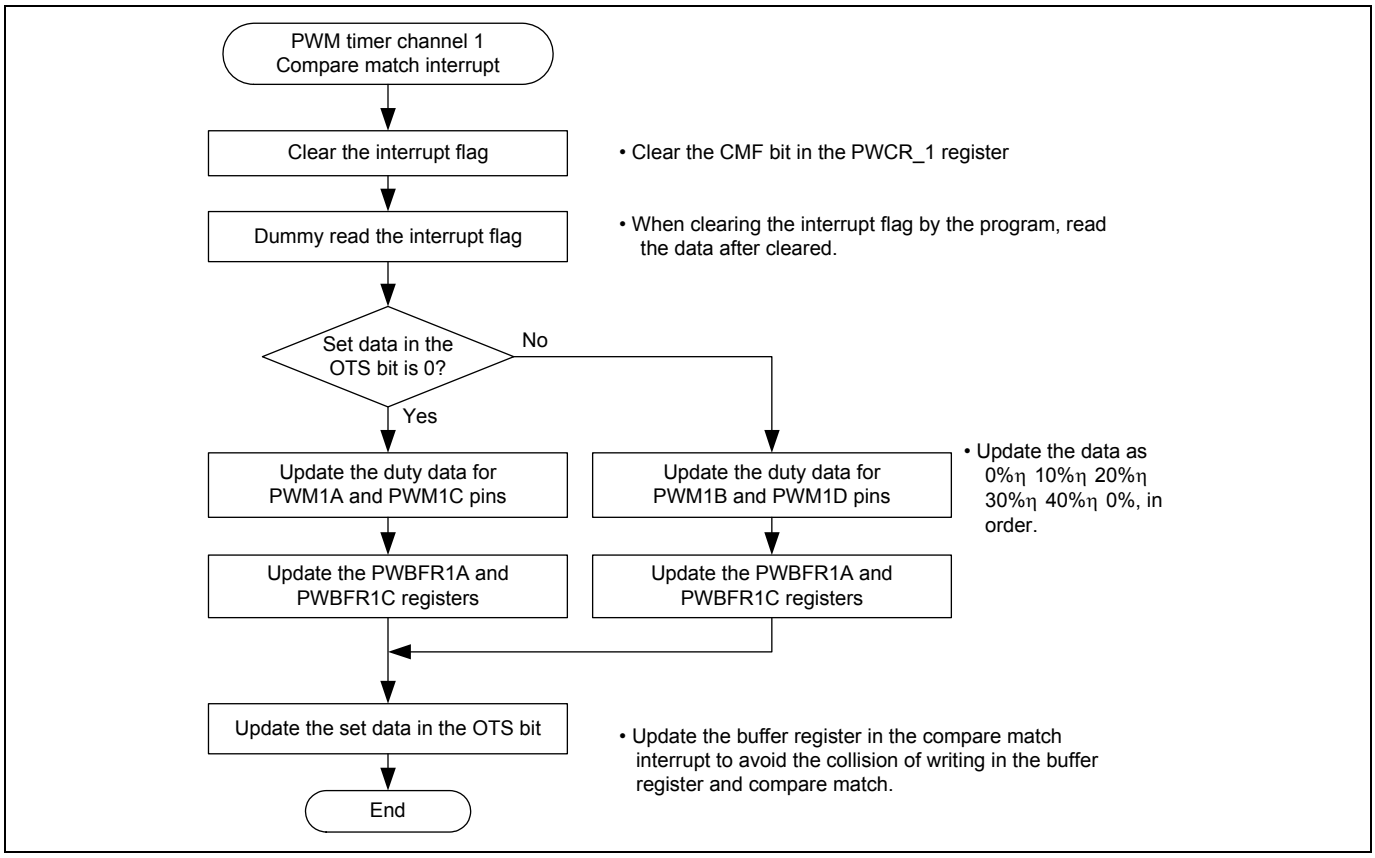

Figure 6 Compare Match Timer Flow Chart

3. Sample Program Listing

3.1 Sample Program Listing "main.c" (1/5)

```
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***********************************************************************
*   Copyright (C) 2009. Renesas Technology Corp., All Rights Reserved.
*""FILE COMMENT""*********** Technical reference data *************************
*   System Name : SH7264 Sample Program
*   File Name   : main.c
*   Abstract    : Sample Program Main
*   Version     : 1.00.00
*   Device      : SH7264
*   Tool-Chain  : High-performance Embedded Workshop (Ver.4.04.01).
*               : C/C++ compiler package for the SuperH RISC engine family
*               :                             (Ver.9.02 Release00).
*   OS          : None
*   H/W Platform: M3A-HS64G50 (CPU board)
*   Description :
***********************************************************************
*   History     : Aug.21,2009 Ver.1.00.00
*""FILE COMMENT END""*****************************************************/
#include <machine.h>
#include "iodefine.h"
```

3.2 Sample Program Listing "main.c" (2/5)

```
46
47    /* ==== Macro definition ==== */
48    #define OTS0       0x0000u        /* PWMnA, PWMnC, PWMnE, PWMnG */
49    #define OTS1       0x1000u        /* PWMnB, PWMnD, PWMnF, PWMnH */
50    #define DT_10per   (450 * 2 / 10) /* Specifies 10% of double of the conversion cycle
51                                         to output from 2 pins alternately) */
52    #define DT_20per   (DT_10per * 2)
53    #define DT_30per   (DT_10per * 3)
54    #define DT_40per   (DT_10per * 4)
55    #define DT_0per    (0)
56
57    /* ==== Prototype declaration ==== */
58    void main(void);
59    void io_init_pwm( void );
60    void io_int_pwm_ch1( void );
61
62    /* ==== Variable definition ==== */
63    static unsigned short pwm_duty_table[] = {
64      DT_0per, DT_10per, DT_20per, DT_30per, DT_40per,
65    };
66
67    /*""FUNC COMMENT""*****************************************************************
68     * ID           :
69     * Outline      : Main function
70     *-----------------------------------------------------------------------------
71     * Include      :
72     *-----------------------------------------------------------------------------
73     * Declaration  : void main(void);
74     *-----------------------------------------------------------------------------
75     * Description  : Uses the PWM timer to output PWM pulses.
76     *-----------------------------------------------------------------------------
77     * Argument     : void
78     *-----------------------------------------------------------------------------
79     * Return Value : void
80     *-----------------------------------------------------------------------------
81     * Note         : None
82     *""FUNC COMMENT END""*************************************************************/
83    void main(void)
84    {
85      /* ==== Configures the motor control PWM timer (PWM timer) ==== */
86      io_init_pwm();
87
88        while(1){
89        /* wait */
90        }
91    }
92
```

3.3 Sample Program Listing "main.c" (3/5)

```
93    /*""FUNC COMMENT""*****************************************************************
94     * ID           :
95     * Outline      : Initializes the motor controller PWM timer
96     *-------------------------------------------------------------------------------
97     * Include      :
98     *-------------------------------------------------------------------------------
99     * Declaration  : void io_init_pwm( void );
100    *-------------------------------------------------------------------------------
101    * Description  : Outputs the PWM pulses from four PWM output pins 1A to 1D.
102    *              : PWM output pin 1B and 1D output inverted signals of 1A and 1C pins.
103    *-------------------------------------------------------------------------------
104    * Argument     : void
105    *-------------------------------------------------------------------------------
106    * Return Value : void
107    *-------------------------------------------------------------------------------
108    * Note         : Port K can be used with the SH7264 only.
109    *""FUNC COMMENT END""*************************************************************/
110   void io_init_pwm( void )
111   {
112     unsigned long dummy;
113
114     /* ==== Sets the Standby control register 8 (STBCR8) ==== */
115     CPG.STBCR8.BIT.MSTP87 = 0;      /* Supplies the clock to the PWM timer */
116
117     /* ==== Sets the general-purpose I/O port (Port K) ==== */
118     PORT.PKCR0.BIT.PK0MD = 1;       /* PWM1A */
119     PORT.PKCR0.BIT.PK1MD = 1;       /* PWM1B */
120     PORT.PKCR0.BIT.PK2MD = 1;       /* PWM1C */
121     PORT.PKCR0.BIT.PK3MD = 1;       /* PWM1D */
122
123     /* ==== Sets the PWM polarity register_1 (PWPR_1) ==== */
124     PWM.PWPR1.BIT.OPS1A = 0;    /* PWM output pin 1A: direct */
125     PWM.PWPR1.BIT.OPS1B = 1;    /* PWM output pin 1B: inverted */
126     PWM.PWPR1.BIT.OPS1C = 0;    /* PWM output pin 1C: direct */
127     PWM.PWPR1.BIT.OPS1D = 1;    /* PWM output pin 1D: inverted */
128
129     /* ==== Sets the PWM control register_1 (PWCR_1) ==== */
130     dummy = PWM.PWCR1.BYTE;
131     PWM.PWCR1.BYTE = 0xE4;          /* Enables the interrupt, clears the CMF, and
132                                     stops the PWM */
133                                    /* Specifies the counter clock as internal clock
134                                     (P clock)/16 */
135     /* ==== Sets the PWM cycle register_1 (PWCYR_1) ==== */
136     PWM.PWCYR1.WORD = 450;          /* 200us = 16/P clock( = 36 MHz) * 450 */
137
138     /* ==== Sets the PWM buffer register_1n (PWBFR_1n) ==== */
139     PWM.PWBFR1A.WORD = 0x0000u;     /* OTS = 0, duty = 0 */
140     PWM.PWBFR1C.WORD = 0x0000u;     /* OTS = 0, duty = 0 */
```

3.4 Sample Program Listing "main.c" (4/5)

```
141
142     /* ==== Sets the Interrupt priority register 14 (IPR14) ==== */
143     INTC.IPR14.BIT._PWM1 = 5;       /* Enables the interrupt by the PWM timer channel 1 */
144
145     /* ==== Activates the PWM ==== */
146     PWM.PWCR1.BIT.CST = 1;          /* Starts counting channel 1 */
147   }
148   /*""FUNC COMMENT""*****************************************************************
149    * ID           :
150    * Outline      : Compare match interrupt on the motor controller PWM timer channel 1
151    *-------------------------------------------------------------------------------
152    * Include      :
153    *-------------------------------------------------------------------------------
154    * Declaration  : void io_int_pwm_ch1( void );
155    *-------------------------------------------------------------------------------
156    * Description  : Compare match interrupt on the PWM timer channel 1.
157    *              : Updates the buffer registers on the PWM output 1A, 1B, 1C, 1D pins.
158    *              : Writing in the buffer register is executed by this interrupt to
159    *              : avoid the collision of writing in the buffer register
160    *              : and compare match.
161    *-------------------------------------------------------------------------------
162    * Argument     : void
163    *-------------------------------------------------------------------------------
164    * Return Value : void
165    *-------------------------------------------------------------------------------
166    * Note         :
167    *""FUNC COMMENT END""*************************************************************/
168   void io_int_pwm_ch1( void )
169   {
170     volatile int dummy;
171     static int ots = 0;             /* 0: OTS bit = 0, 1: OTS bit = 1 */
172     static int idx1 = 0, idx2 = 0;
173
174     /* ==== Clears the interrupt flag ==== */
175     PWM.PWCR1.BIT.CMF = 0;
176     dummy = PWM.PWCR1.BIT.CMF;      /* Dummy read is required */
177
```

3.5 Sample Program Listing "main.c" (5/5)

```
178     /* ==== Updates the buffer register when OTS bit = 0 (PWM1A/PWM1C) ==== */
179     if( ots == 0 ){
180       /* ---- Updates the PWM1A/PWM1C index ---- */
181       if( ++idx1 >= 5 ){        /* idx1 = 0 to 4 -> duty cycle 0% to 40% */
182           idx1 = 0;
183       }
184       /* ---- Updates the buffer register ---- */
185       PWM.PWBFR1A.WORD = OTS0 | pwm_duty_table[idx1];
186       PWM.PWBFR1C.WORD = OTS0 | pwm_duty_table[idx1];
187     }
188     else{
189       /* ---- Updates the PWM1B/PWM1D index ---- */
190       if( ++idx2 >= 5 ){        /* idx1 = 0 to 4 -> duty cycle 0% to 40% */
191           idx2 = 0;
192       }
193       /* ---- Updates the buffer register ---- */
194       PWM.PWBFR1A.WORD = OTS1 | pwm_duty_table[idx2];
195       PWM.PWBFR1C.WORD = OTS1 | pwm_duty_table[idx2];
196     }
197     /* ==== Updates the set data in the OTS bit ==== */
198     ots ^= 1;
199   }
200
201   /* End of File */
```

4. References

- Software Manual
  SH-2A/SH-2A-FPU Software Manual Rev. 3.00
  (Download the latest version from the Renesas website.)

- Hardware Manual
  SH7262 Group, SH7264 Group Hardware Manual Rev. 2.00
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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep. 30, 2009	—	First edition issued

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