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Renesas Electronics Corporation

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April 1, 2003

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APPLICATION NOTE

Using Interval Timing Function to Increment 8-Bit Counter

Introduction

Timer A, an 8-bit timer with an interval timing function is used to increment an 8-bit counter in RAM.

Target Device

H8/300H Tiny Series H8/3664

Contents

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1. Specifications

1. Timer A, an 8-bit timer with an interval timing function is used to increment an 8-bit counter in RAM.
2. A timer A interrupt is generated when timer counter A (TCA) overflows, and the counter in RAM is incremented or initialized during the timer A interrupt handling.
3. The 8-bit counter in RAM starts from the initial value of H'00. When the counter's value becomes H'FF, it is initialized to H'00 and incrementing resumes.
4. A timer A interrupt is set to be generated every 65.536 ms.

2. Description of Functions Used

In this sample task, the 8-bit counter is incremented by the interval timing function of timer A. Figure 2.1 is a block diagram of the interval timing function of timer A. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz OSC clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ. PSS is incremented every cycle.
- Timer mode register A (TMA) is an 8-bit readable/writable register that selects the prescaler and input clock. In this sample task, PSS is selected as the prescaler and division by 4096 is selected as the prescaler division ratio.
- Timer counter A (TCA) is an 8-bit read-only up-counter that is incremented by internal clock input. When TCA overflows, the timer A interrupt request flag (IRRTA) in interrupt request register 1 (IRR1) is set to 1.
- IRRTA in IRR1 is set to 1 when TCA overflows. A timer A interrupt is accepted and timer A interrupt handling starts when the IRRTA flag is set to 1, timer A interrupt enable (IENTA) in interrupt enable register 1 (IENR1) is set to 1, and the I bit in the condition code register (CCR) is cleared to 0.
- The TCA overflow cycle in this sample task is calculated by the following equation:

$$\text{TCA overflow cycle} = \frac{1}{\text{System clock}/4096} \times 256$$

$$= 65.536 \text{ ms}$$

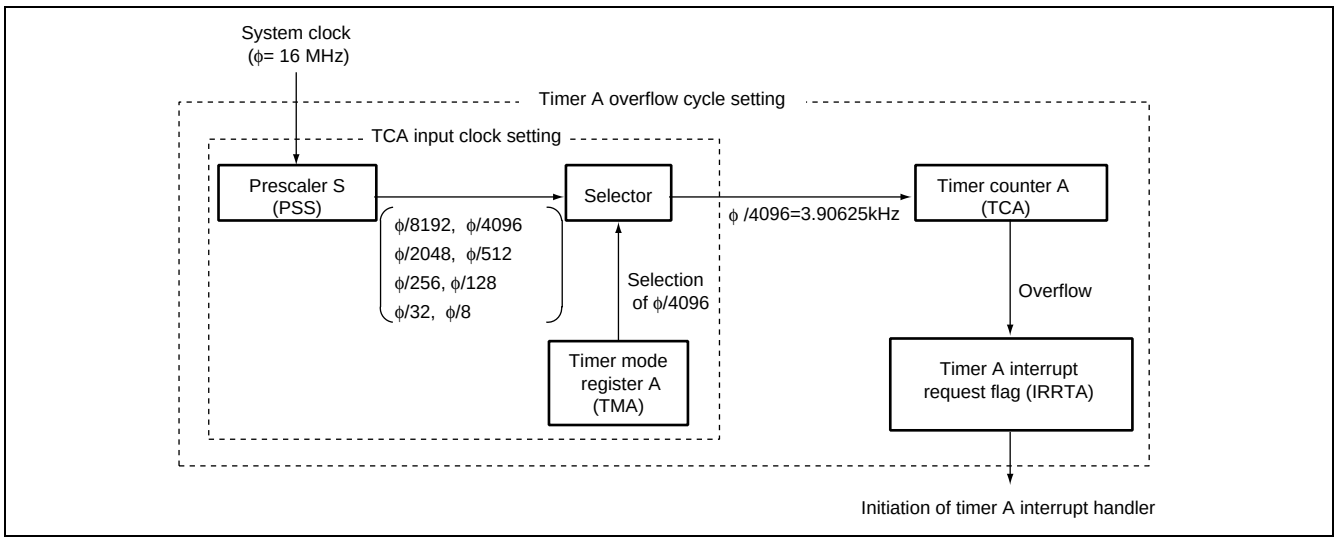

Figure 2.1 Timer A's Interval Timing Function

Table 2.1 lists the function allocation for this sample task. The functions listed in table 2.1 are allocated so that the 8-bit counter is incremented by the interval timing function of timer A.

Table 2.1 Function Allocation

Function	Description
PSS	13-bit counter with system clock input
TCA	8-bit counter with clock input of system clock/4096
TMA	Selects prescaler and sets the prescaler division ratio
IRRTA	Indicates whether or not a timer A interrupt request is issued

3. Description of Operations

Figure 3.1 shows this sample task's principle of operation. The hardware and software processing shown in figure 3.1 applies the interval timing function of timer A to increment the 8-bit counter.

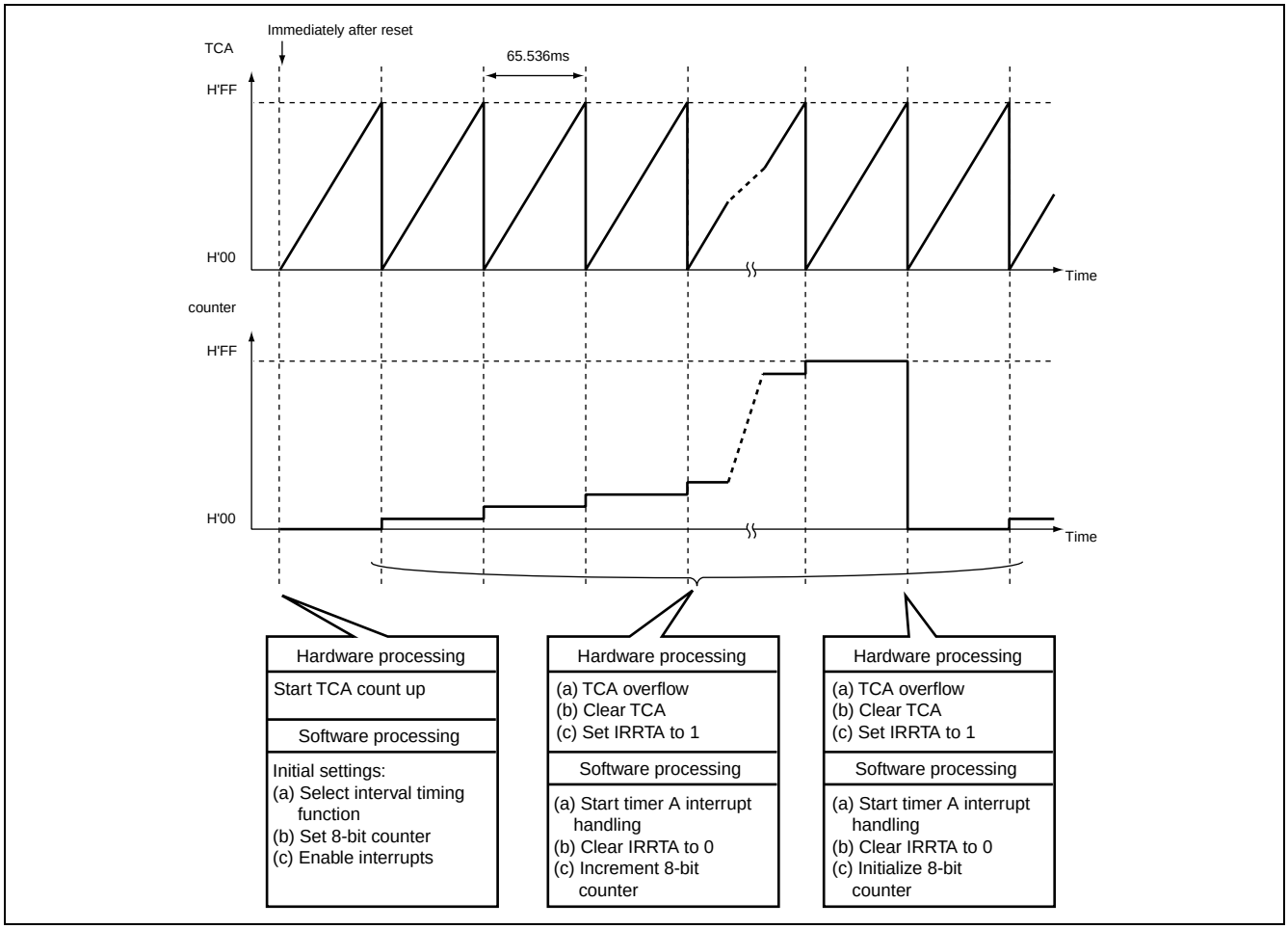

Figure 3.1 Operation Principle: Using Interval Timing Function of Timer A to Increment 8-Bit Counter

4. Description of Software

4.1 Description of Modules

Table 4.1 describes the software used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Selects the interval timing function, sets the 8-bit counter, and enables interrupts.
Count up	taint	During the timer A interrupt handling routine, increments or initializes the 8-bit counter that is set to R1L.

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 4.2 describes the internal registers used in this sample task.

Table 4.2 Description of Internal Registers

Register Name		Function	Address	Setting
IRR1	IRRTA	Interrupt request register 1 (timer A interrupt request flag):	H'FFF6	
		When IRRTA is cleared to 0, no timer A interrupt is requested.	Bit 6	0
		When IRRTA is set to 1, a timer A interrupt is requested.		
IENR1	IENTA	Interrupt enable register 1 (timer A interrupt enable):	H'FFF4	
		When IENTA is set to 1, timer A interrupt requests are enabled.	Bit 6	1
TMA		Timer mode register A:	H'FFA6	H'11
		When TMA is set to H'11, timer A is set to the interval timing function, the TCA input clock source to PSS, and the prescaler division ratio to division by 4096.		
TCA		Timer counter A:	H'FFA7	H'00
		8-bit up-counter incremented by clock input of system clock/4096.		

4.4 Description of RAM

Table 4.3 describes the RAM used in this sample task.

Table 4.3 Description of RAM

Label Name	Function	Address	Used in
counter	8-bit counter to count timer A interrupts	H'FB80	Main routine Count up

5. Flowcharts

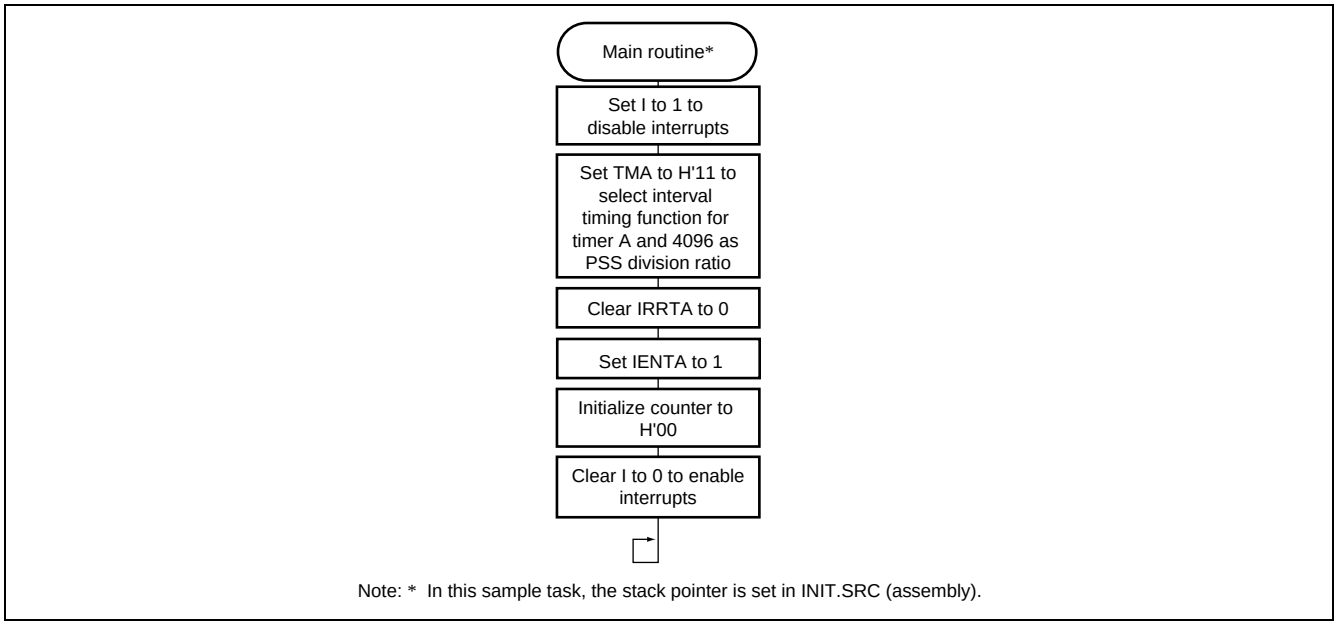

Figure 5.1 Flowchart for Main Routine

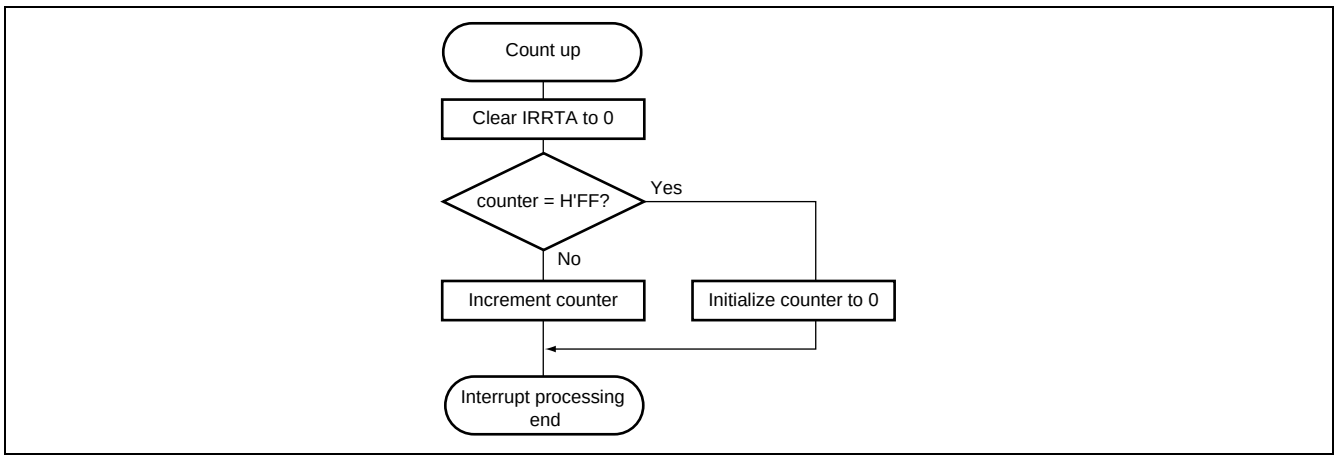

Figure 5.2 Flowchart for Timer A Interrupt Handling Routine

6. Program Listing

INIT.SRC (Program listing)

```
.EXPORT_INIT
       .IMPORT_main
;
       .SECTION    P,CODE
_INIT:
       MOV.W#H'FF80,R7
       LDC.B#B'10000000,CCR
       JMP@_main
;
       .END
```

```
/*;*********************************************************/
/*;                                                       */
/*;    H8/300H Tiny Series -H8/3664-                      */
/*;    Application Note                                   */
/*;                                                       */
/*;    '8-bit Counter Count-Up by Interval Function'      */
/*;                                                       */
/*;    Function                                           */
/*;    : Timer A Interval Timer                           */
/*;                                                       */
/*;    External Clock : 16MHz                             */
/*;    Internal Clock : 16MHz                             */
/*;    Sub Clock      : 32.768kHz                         */
/*;                                                       */
/*;*********************************************************/

    #include    <machine.h>
```

```
/*;*********************************************************/
/*;    Symbol Definition                                    */
/*;*********************************************************/
struct BIT {
    unsigned char    b7:1;      /* bit7 */
    unsigned char    b6:1;      /* bit6 */
    unsigned char    b5:1;      /* bit5 */
    unsigned char    b4:1;      /* bit4 */
    unsigned char    b3:1;      /* bit3 */
    unsigned char    b2:1;      /* bit2 */
    unsigned char    b1:1;      /* bit1 */
    unsigned char    b0:1;      /* bit0 */
};

#define    TMA          *(volatile unsigned char *)0xFFA6    /* Timer Mode Register A            */
#define    TCA          *(volatile unsigned char *)0xFFA7    /* Timer Counter A                  */
#define    IENR1_BIT    (*(struct BIT *)0xFFF4)              /* Interrupt Enable Register 1      */
#define    IENTA        IENR1_BIT.b6                         /* Timer A Interrupt Enable         */
#define    IRR1_BIT     (*(struct BIT *)0xFFF6)              /* Interrupt Request Register 1     */
#define    IRRTA        IRR1_BIT.b6                          /* Timer A Interrupt Request Flag   */

#pragma        interrupt    (taint)
/*;*********************************************************/
/*;    Function Definition                                  */
/*;*********************************************************/
extern    void    INIT ( void );                             /* SP Set                          */
void      main ( void );
void      taint ( void );
/*;*********************************************************/
/*;     RAM define                                          */
/*;*********************************************************/

unsigned char         counter;                               /* 8bit Counter                    */
```

```
/*;*********************************************************/
/*;    Vector Address                                      */
/*;*********************************************************/
#pragma    section        V1                                /* VECTOR SECTOIN SET         */
void (*const VEC_TBL1[])(void) = {
/* 0x00 - 0x0f */

INIT                                                        /* 00 Reset                   */
};
#pragma    section        V2                                /* VECTOR SECTOIN SET         */
void (*const VEC_TBL2[])(void) = {
    taint                                                   /* 26 Timer A Interrupt       */
};
#pragma        section                                      /* P                          */
/*;*********************************************************/
/*;    Main Program                                        */
/*;*********************************************************/
void main ( void )
{

    set_imask_ccr(1);                                       /* Interrupt Disable          */

    TMA = 0x11;                   /* Initialize Timer A Function & TCA input clock period */

    IRRTA = 0;                                              /* Clear IRRTA                */
    IENTA = 1;                                              /* Timer A Interrupt Enable   */

    counter = 0;                                            /* Initialize 8bit  Counter   */

    set_imask_ccr(0);                                       /* Interrupt Enable           */

    while(1)    {
        ;
    }
}
```

```
/*;*********************************************************/
/*;    Timer A Interrupt                                    */
/*;*********************************************************/
void taint ( void )
{
    IRRTA = 0;                                          /* Clear IRRTA              */

    if ( counter == 0xff )    {                         /* 8bit Counter = 0xff?     */
        counter = 0;                                    /* Clear 8bit Counter       */
    }
    else    {
        counter++;                                      /* Increment 8bit Counter   */
    }
}
```

Link Address Setting:

Section Name	Address
CV1	H'0000
CV2	H'0026
P	H'0100
B	H'FB80