To our customers,

---

### Old Company Name in Catalogs and Other Documents

On April 1\textsuperscript{st}, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: [http://www.renesas.com](http://www.renesas.com)

April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

---

Issued by: Renesas Electronics Corporation ([http://www.renesas.com](http://www.renesas.com))

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.

2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.

4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.

5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.

6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.

7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depend on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.

8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.

9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention. Appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.

10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.
H8/300H Super Low Power Series
Using Input-Capture Function of Timer G to Measure Pulse Period

Introduction
The period of a pulse input to Input Capture Input Pin (TMIG) is measured by using the Timer G input capture function. The maximum pulse period that can be measured is 1.638 ms and the measurement is accurate to within 6.4 µs.

Target Device
H8/38099

Contents

1. Specifications.................................................................................................................. 2
2. Description of Functions Used........................................................................................ 2
3. Principle of Operation ..................................................................................................... 5
4. Description of Software.................................................................................................. 6
5. Flowcharts..................................................................................................................... 10
6. Link Address Specifications.......................................................................................... 12
1. Specifications

1. The period of a pulse input to Input Capture Input Pin (TMIG) is measured using the Timer G input capture function.
2. The counter value of Timer Counter G (TCG) between rising edges of an input pulse is counted and the period of an input pulse is measured based on this counter value.
3. The maximum pulse period that can be measured is 1.638 ms and the measurement accuracy is 6.4 µs.

![Figure 1 Measurement of Input Pulse Period](image1)

2. Description of Functions Used

2.1 Block Diagram of Timer G

Figure 2 shows the block diagram of the Timer G input capture function.

![Figure 2 Block Diagram of Timer G Input Capture Function](image2)

[Legend]
- TMG: Timer mode register G
- TCG: Timer counter G
- ICRGF: Input capture register GF
- ICRGR: Input capture register GR
- IRRTG: Timer G interrupt request flag
- NCS: Noise canceler select
- PSS: Prescaler S
2.2 Functions Used

2.2.1 Description of Functions

In this sample task, the period of pulses input to Input Capture Input Pin (TMIG) is measured using the Timer G input capture function. Details of the bits of the individual registers will be explained in 4.3, “Internal Registers”.

- The system clock (\(\phi\))
  The system clock (\(\phi\)) is a 10-MHz system clock and is a reference clock to operate the CPU and its peripheral functions.

- The prescaler S (PSS)
  The prescaler S (PSS) is a 17-bit counter using \(\phi\) as input and is counted up every cycle.

- The Port Mode Register F (PMRF)
  The Port Mode Register F (PMRF) controls the selection of the pin function on port F. Setting the TMIG bit in PMRF to 1 selects operation of pin PF0 as the TMIG input pin and operation of Timer G as an input capture timer.

- The Timer Counter G (TCG)
  The Timer Counter G (TCG) is an 8-bit up-counter which is incremented by clock input. The input clock is selected by bits CKS1 and CKS0 in TMG. TMIG in PMRF is set to 1 to operate TCG as an input capture timer. In input capture timer operation, the TCG value can be cleared by the rising edge, falling edge, or both edges of the input capture input signal, according to the setting made in TMG. When TCG overflows from H'FF to H'00, when OVIE in TMG is 1, IRRTG in IRR2 is set to 1, and when IENTG in IENR2 is 1, an interrupt request is sent to the CPU. TCG cannot be read or written by the CPU. It is initialized to H'00 upon reset.

- The Input Capture Register GR (ICRGR)
  The Input Capture Register GR (ICRGR) is an 8-bit read-only register. When a rising edge of the input signal is detected, the current TCG value is transferred to ICRGR. When IIEGS in TMG is 0 at this time, IRRTG in IRR2 is set to 1, and when IENTG in IENR2 is 1, an interrupt request is sent to the CPU. To ensure dependable input capture operation, the pulse width of the input capture input signal must be at least 2\(\phi\) or 2\(\phi_{sub}\) (when the noise canceller is not used). ICRGF is initialized to H'00 upon reset.

- Timer Mode Register G (TMG)
  Timer Mode Register G (TMG) is an 8-bit read/write register. It selects 4 types of TCG internal clocks, counter clearing, and the interrupt request edge of input capture input signal, and controls enable/disable of overflow interrupt request, and indicates the overflow flag. TMG is initialized to H'00 upon reset.

- A pulse, whose frequency is subject to measurement, is input through Input Capture Input Pin (TMIG).
2.2.2 Calculation of Input Pulse Periods

The method to calculate input pulse periods in this sample task is shown below. Pulse periods cannot be measured accurately when the TCG overflows. Input pulse period must be therefore shorter than the TCG overflow period (1.638 ms).

- The following are defined in the user RAM area: PRDHL, for storage of the TCG value that is transferred to the Input Capture Register GR (ICRGR) on detection of a rising edge of the input pulse; the SRTF flag, which indicates whether or not an interrupt is the second to be generated by rising edges of the input pulse, and the ENDF flag, which indicates whether or not the measurement is complete.
- Capture of the rising edge of the first input pulse drives clearing of the TCG counter value.
- Capture of the rising edge of the second input pulse drives transfer of the ICRGR value, which has been transferred from TCG, to PRDHL.
- The following formula (1) provides the input pulse period.

Input pulse period
\[ \text{Input pulse period} = \text{(TCG counter value stored in PRDHL)} \times \text{(TCG input clock period)} \]
\[ = \text{(TCG counter value stored in PRDHL)} \times 6.4 \mu\text{s} \left(1/\phi: 10 \text{MHz}/\text{PSS: 64}\right) \] ............. (1)

- When the TCG overflows after the first rising edge of the input pulse is captured, the value of H'FF is stored in PDRHL.

2.2.3 Watchdog Timer Function

H8/38099 incorporates a watchdog timer (WDT) that is turned on by default after a reset. The WDT is an 8-bit timer that can generate an internal reset signal when the timer counter overflows because a system crash has prevented the CPU from writing to it. In this sample task, the WDT function is not used, so it is turned off.

- Timer Control/Status Register WD1 (TCSRWD1)
  Timer Control/Status Register WD1 (TCSRWD1) performs TCSRWD1 and TCWD write control. TCSRWD1 also controls the watchdog timer operation and indicates the operating state. TCSRWD1 must be rewritten by using the MOV instruction. Bit-manipulation instructions cannot be used to change the setting.

2.3 Assignment of Functions

Table 1 lists the assignment of functions applicable to this sample task. The functions are assigned as indicated in table 1, and frequencies are measured by the Timer G input capture function.

Table 1 Assignment of Functions

<table>
<thead>
<tr>
<th>Function</th>
<th>Assignment of Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSS</td>
<td>A 17-bit up-counter using the system clock as input</td>
</tr>
<tr>
<td>TMG</td>
<td>This selects the event-counter function, whether counting is up or down, and the input clock.</td>
</tr>
<tr>
<td>TCG</td>
<td>An 8-bit up-counter driven by the detection of rising edges on the TMIC input pin.</td>
</tr>
<tr>
<td>ICRGR</td>
<td>When a rising edge of the TMIG input pulse is detected, the TCG counter value is stored.</td>
</tr>
<tr>
<td>NCS</td>
<td>This controls the noise-cancellation function and is not used in this task.</td>
</tr>
<tr>
<td>IENTG</td>
<td>This enables interrupt requests of rising edges of TMIG pin input.</td>
</tr>
<tr>
<td>IRRTG</td>
<td>An interrupt flag of rising edge of TMIG pin input.</td>
</tr>
<tr>
<td>TMIG</td>
<td>Pulses to be measured are input.</td>
</tr>
<tr>
<td>TCSRWD1</td>
<td>This stops the watchdog timer.</td>
</tr>
</tbody>
</table>
3. Principle of Operation

Figure 3 illustrates the principle of operation of this sample task. As shown in figure 3, pulse periods are measured by the Timer G input capture function by means of hardware processing and software processing.

![Diagram of principle of operation]

**Figure 3  Principle of Operation of Pulse Period Measurement by Timer G Input Capture Function**
4. Description of Software

4.1 Modules

The modules applicable to this sample task are listed in table 2.

Table 2 Description of Modules

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Label Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Routine</td>
<td>main</td>
<td>Sets the Timer G input capture function, sets the TMIG input pin function, and enables interrupts.</td>
</tr>
<tr>
<td>Period Measurement</td>
<td>tgint</td>
<td>During the Timer G interrupt handling, initializes TCG to H'00 when the first IRRTG interrupt occurs, stores ICRGR data in the RAM when the second IRRTG interrupt occurs, and disables Timer G interrupt requests.</td>
</tr>
</tbody>
</table>

4.2 Arguments

No arguments are used in this sample task.
### 4.3 Internal Registers

The following tables list the internal registers used in this sample task.

- **Timer Mode Register G (TMG)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Setting Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
  | 7   | OVFH      | 0             | R/(W)* | Timer Overflow Flag H  
Indicates that TCG has overflowed from H'FF to H'00 when the input capture input signal is high. This flag is set by hardware and cleared by software. It cannot be set by software.  
[Setting condition]  
  • Set when input capture input signal is high level and TCG overflows from H'FF to H'00.  
[Clearing condition]  
  • Writing 0 to OVFH after reading OVFH = 1 |
  | 6   | OVFL      | 0             | R/(W)* | Timer Overflow Flag L  
Indicates that TCG has overflowed from H'FF to H'00 when the input capture input signal is low, or in interval operation. This flag is set by hardware and cleared by software. It cannot be set by software.  
[Setting condition]  
  • Set when TCG overflows from H'FF to H'00 while input capture input signal is low level or during interval operation  
[Clearing condition]  
  • Writing 0 to OVFL after reading OVFL = 1 |
  | 5   | OVIE      | 1             | R/W   | Timer Overflow Interrupt Enable  
Selects enabling or disabling of interrupt generation when TCG overflows.  
0: TCG overflow interrupt request is disabled  
1: TCG overflow interrupt request is enabled |
  | 4   | IIEGS     | 0             | R/W   | Input Capture Interrupt Edge Select  
Selects the input capture input signal edge that generates an interrupt request.  
0: Interrupt generated on rising edge of input capture input signal  
1: Interrupt generated on falling edge of input capture input signal |
  | 3   | CCLR1     | 1             | R/W   | Counter Clear 1 and 0  
Specify whether or not TCG is cleared by the rising edge, falling edge, or both edges of the input capture input signal.  
00: TCG clearing is disabled  
01: TCG cleared by falling edge of input capture input signal  
10: TCG cleared by rising edge of input capture input signal  
11: TCG cleared by both edges of input capture input signal |
  | 2   | CCLR0     | 0             | R/W   | Clock Select  
Select the clock input to TCG from four internal clock sources.  
00: Internal clock: counting on φ/64  
01: Internal clock: counting on φ/32  
10: Internal clock: counting on φ/2  
11: Internal clock: counting on φ/4 |

Note: * Only 0 can be written to clear the flag.
Using Input-Capture Function of Timer G to Measure Pulse Period

- **Input Capture Register GR (ICRGR)**
  - **Address:** H'FF86

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Setting</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ICRGR7</td>
<td>—</td>
<td>R</td>
<td>ICRGR is an 8-bit read-only register. When a rising edge of the input capture input signal is detected, the current TCG value is transferred to ICRGR. When IIEGS in TMG is 0 at this time, IRRTG in IRR2 is set to 1, and when IENTG in IENR2 is 1, an interrupt request is sent to the CPU. To ensure dependable input capture operation, the pulse width of the input capture input signal must be at least 2φ or 2φ\text{SUB} (when the noise canceller is not used).</td>
</tr>
<tr>
<td>6</td>
<td>ICRGR6</td>
<td>—</td>
<td>R</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>ICRGR5</td>
<td>—</td>
<td>R</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>ICRGR4</td>
<td>—</td>
<td>R</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>ICRGR3</td>
<td>—</td>
<td>R</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>ICRGR2</td>
<td>—</td>
<td>R</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>ICRGR1</td>
<td>—</td>
<td>R</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>ICRGR0</td>
<td>—</td>
<td>R</td>
<td>ICRGR is initialized to H'00 upon reset.</td>
</tr>
</tbody>
</table>

- **Interrupt Enable Register 2 (IENR2)**
  - **Address:** H'FFF4

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Setting</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>IENTG</td>
<td>1</td>
<td>R/W</td>
<td>Timer G Interrupt Request Enable</td>
</tr>
</tbody>
</table>

  The timer G interrupt request is enabled when this bit is set to 1.

- **Interrupt Request Register 2 (IRR2)**
  - **Address:** H'FFF7

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Setting</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>IRRTG</td>
<td>1</td>
<td>R/W</td>
<td>Timer G Interrupt Request Flag</td>
</tr>
</tbody>
</table>

  [Setting condition]
  - The timer G input capture or overflow occurs.

  [Clearing condition]
  - Writing of 0 to this bit.

- **Port Mode Register F (PMRF)**
  - **Address:** HF03C

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Setting</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>TMIG</td>
<td>1</td>
<td>R/W</td>
<td>PF0/TMIG Pin Function Switch</td>
</tr>
</tbody>
</table>

  0: PF0 I/O pin
  1: TMIG input pin
### 4.4 RAM Usage

Table 3 lists and describes the RAM usage in this sample task.

<table>
<thead>
<tr>
<th>Type</th>
<th>Label Name</th>
<th>Description</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char</td>
<td>PRDHL</td>
<td>Stores the TCG count value between rising edges of the TMIG input capture input signal</td>
<td>tgint</td>
</tr>
<tr>
<td>unsigned char</td>
<td>USRF</td>
<td>Flag to indicate whether or not the interrupt is the second Timer G interrupt</td>
<td>tgint</td>
</tr>
<tr>
<td></td>
<td>ENDF</td>
<td>Flag to indicate whether or not period measurement has ended</td>
<td>main, tgint</td>
</tr>
</tbody>
</table>
5. Flowcharts

5.1 Function main

```
main

SP = H'FFFF80
set_imask_ccr(1)
TCSRWD1 = H'9E
TCSRWD1 = H'A2
TCSRWD1 = H'8E
IENTG = 1
set_imask_ccr(0)
ENDF! = 1?
Yes
No

Enable interrupts by setting I bit of CCR to 0.

Disable interrupts by setting I bit of CCR to 1.

Stop the WDT.

Initialize the stack pointer.

Initialize RAM to be used.

Set the TMIG input pin function.

Dummy read to clear the flag.

Set timer mode register G. Clear TCG on the rising edge of the input signal for input capture.

Clear Timer G interrupt request flag.

Enable Timer G interrupts.

Initialize the stack pointer.

```
5.2 Function tgint

```
<table>
<thead>
<tr>
<th>tgint</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRRTG = 0</td>
</tr>
<tr>
<td>IENTG = 0</td>
</tr>
<tr>
<td>SRTF = 1?</td>
</tr>
<tr>
<td>No</td>
</tr>
<tr>
<td>OVFH = 1? or OVFL = 1?</td>
</tr>
<tr>
<td>Yes</td>
</tr>
<tr>
<td>SRTF = 1</td>
</tr>
<tr>
<td>tmp = TMG</td>
</tr>
<tr>
<td>TMG = H'20</td>
</tr>
<tr>
<td>IENTG = 1</td>
</tr>
<tr>
<td>No</td>
</tr>
<tr>
<td>TMG = H'00</td>
</tr>
<tr>
<td>PRDHL = H'FF</td>
</tr>
<tr>
<td>SRTF = 0</td>
</tr>
<tr>
<td>PRDHL = ICRGR</td>
</tr>
<tr>
<td>ENDF = 1</td>
</tr>
<tr>
<td>TMG = H'00</td>
</tr>
<tr>
<td>Return</td>
</tr>
</tbody>
</table>
```

---

- **Clear Timer G interrupt request flag.**
- **Disable Timer G interrupt requests.**
- **Set SRTF to start the measurement.**
- **Dummy read to clear flag.**
- **Clear the overflow flag.**
- **Enable overflow interrupts.**
- **Enable Timer G interrupts.**
- **Clear the overflow flag.**
- **Store H'FF in PRDHL.**
- **Clear SRTF.**
- **Store the TCG value on the 2nd rising edge in PRDHL.**
- **Set ENDF.**
- **Disable overflow interrupts.**
### 6. Link Address Specifications

<table>
<thead>
<tr>
<th>Section Name</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>CV1</td>
<td>H'000000</td>
</tr>
<tr>
<td>CV2</td>
<td>H'0000D8</td>
</tr>
<tr>
<td>P</td>
<td>H'000800</td>
</tr>
<tr>
<td>B</td>
<td>H'FFFF380</td>
</tr>
</tbody>
</table>
Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Mar.15.07</td>
<td>—</td>
<td>—</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>

...
**Notes regarding these materials**

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.

2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.

3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.

4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (http://www.renesas.com)

5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.

6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guaranties regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.

7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.

8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
   (1) artificial life support devices or systems
   (2) surgical implantations
   (3) healthcare intervention (e.g., excision, administration of medication, etc.)
   (4) any other purposes that pose a direct threat to human life

Renesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.

9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.

10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.

11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.

12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.

13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.

© 2007. Renesas Technology Corp., All rights reserved.