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Renesas Electronics Corporation

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H8/300L SLP Series

Using Input-Capture Function to Measure Pulse Period

Introduction

The period of a pulse input to Input Capture Input Pin (TMIG) is measured using the Timer G input capture function. The maximum pulse period that can be measured is 3.277 ms and the measurement accuracy is 12.8 µs.

Target Device

H8/38024

Contents

1. Specifications

1. The period of a pulse input to Input Capture Input Pin (TMIG) is measured using the Timer G input capture function.
2. The counter value of Timer Counter G (TCG) between rising edges of an input pulse is stored in the RAM and the period of an input pulse is measured based on this counter value.
3. The maximum pulse period that can be measured is 3.277 ms and the measurement accuracy is 12.8 µs.

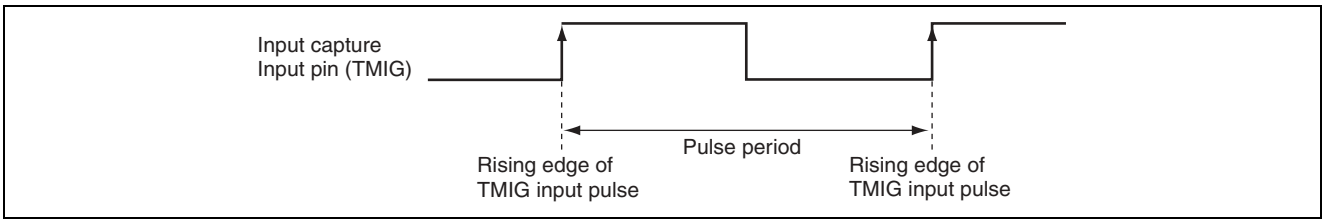


Figure 1.1 Measurement of Input Pulse Period

2. Description of Functions

1. In this task example, the period of pulses input to Input Capture Input Pin (TMIG) is measured using the Timer G input capture function.
   A. Figure 2.1 shows the block diagram of the Timer G input capture function which is described below.
      - The system clock (ϕ) is a 5 MHz clock and is a reference clock to operate the CPU and its peripheral functions.
      - The Prescaler S (PSS) is a 13-bit counter using ϕ as its input clock and is counted up every cycle.
      - The Timer Counter G (TCG) is an 8-bit read/write up-counter and is counted up by an internal or external clock which is input. The input clock can be selected from four clocks obtained by dividing the system clock by 2, 32 and 64, and an external clock. In this task example, a clock obtained by dividing the system clock by 64 is selected as the TCG input clock.
      - The Timer Mode Register G (TMG) is an 8-bit read/write register. It selects TCG input clock, counter clearing, and the interrupt request edge of input capture input signal, and controls enable/disable of overflow interrupt request, and indicates the overflow flag.
      - The Input Capture Register GR (ICRGR) is an 8-bit read-only register. When the rising edge of an input pulse to the input capture pin is detected, the value of the TCG at that time is transferred to ICRGR. If IRRTG in IRR2 is set to 1, an interrupt request will be sent to the CPU.
      - A pulse, whose frequency is subject to measurement, is input through Input Capture Input Pin (TMIG).
      - The method to calculate input pulse periods in this task example is shown below. Pulse periods cannot be measured accurately if the TCG overflows. Input pulse period must therefore be shorter than the TCG overflow period (3.277 ms)
      - If the TCG overflows after the first rising edge of the input pulse is captured, the value of H'FF is stored in PDRHL.

Input pulse period = (TCG counter value stored in PDRHL) × (TCG input clock period)

= (TCG counter value stored in PDRHL) × 12.8 µs (1/ (ϕ: 5 MHz/PSS:64))

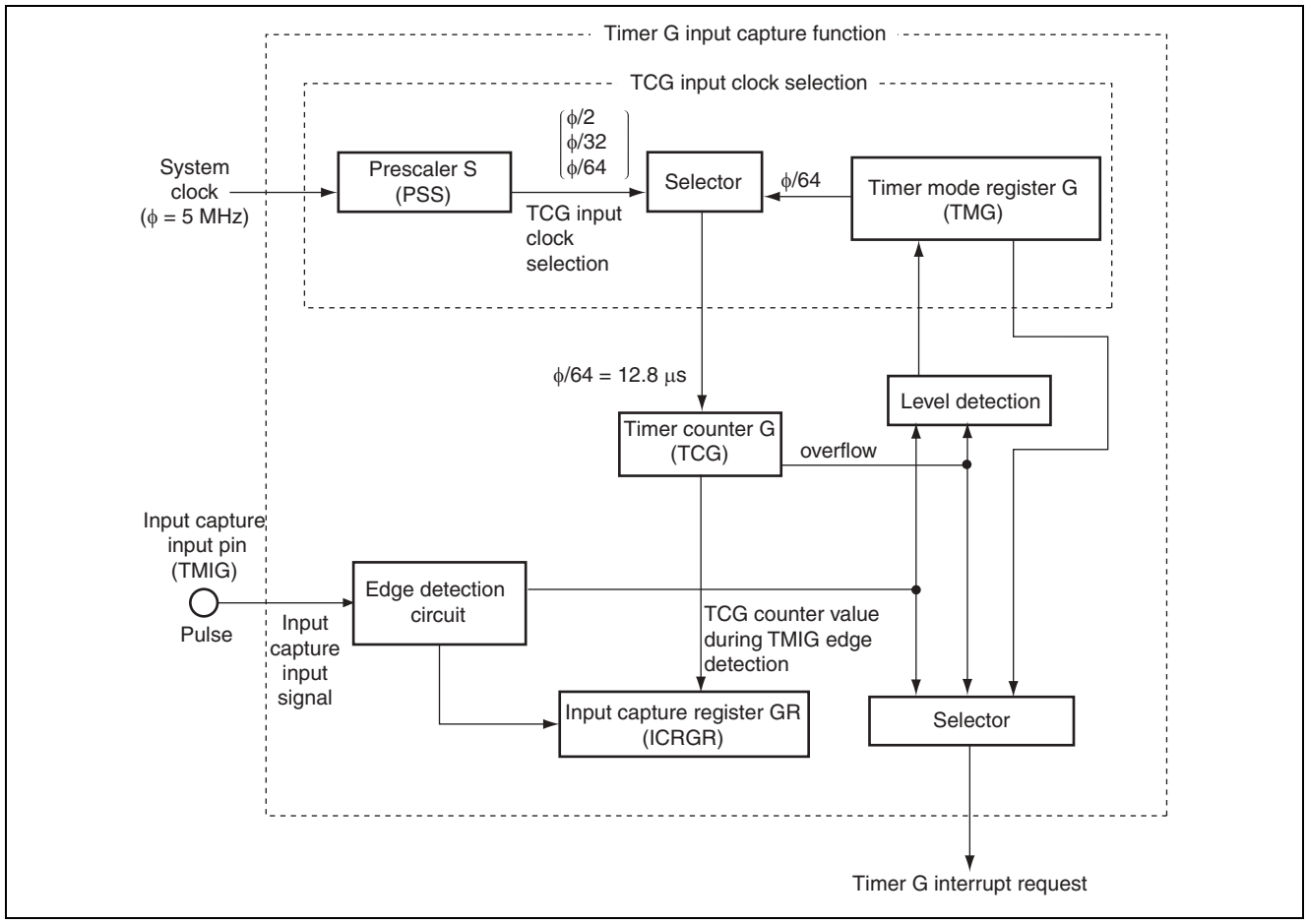


Figure 2.1 Block Diagram of Timer G Input Capture Function

2. Table 2.1 shows function assignment in this task example. The functions are assigned as shown in table 2.1 and frequencies are measured by the Timer G input capture function.

Table 2.1 Assignment of Functions

Function	Assignment
PSS	A 13-bit counter using the system clock as input
TMG	Selects the interrupt request edge of the input capture input signal, enables TCG overflow interrupts, and sets TCG input clock.
TCG	An 8-bit up counter using the system clock/64 as input
ICRGR	When rising edge of an TMIG input pulse is detected, the TCG counter value at this time is stored.
NCS	Controls noise cancellation function not to be used.
IENTG	Enables interrupt requests at the rising edge of TMIG pin input.
IRRTG	An interrupt flag of rising edge of TMIG pin input.
TMIG	Pulses to be measured are input.

3. Principle of Operation

1. Figure 3.1 illustrates the principle of operation of this sample task. As shown in figure 3.1, pulse periods are measured by the Timer G input capture function by means of hardware processing and software processing.

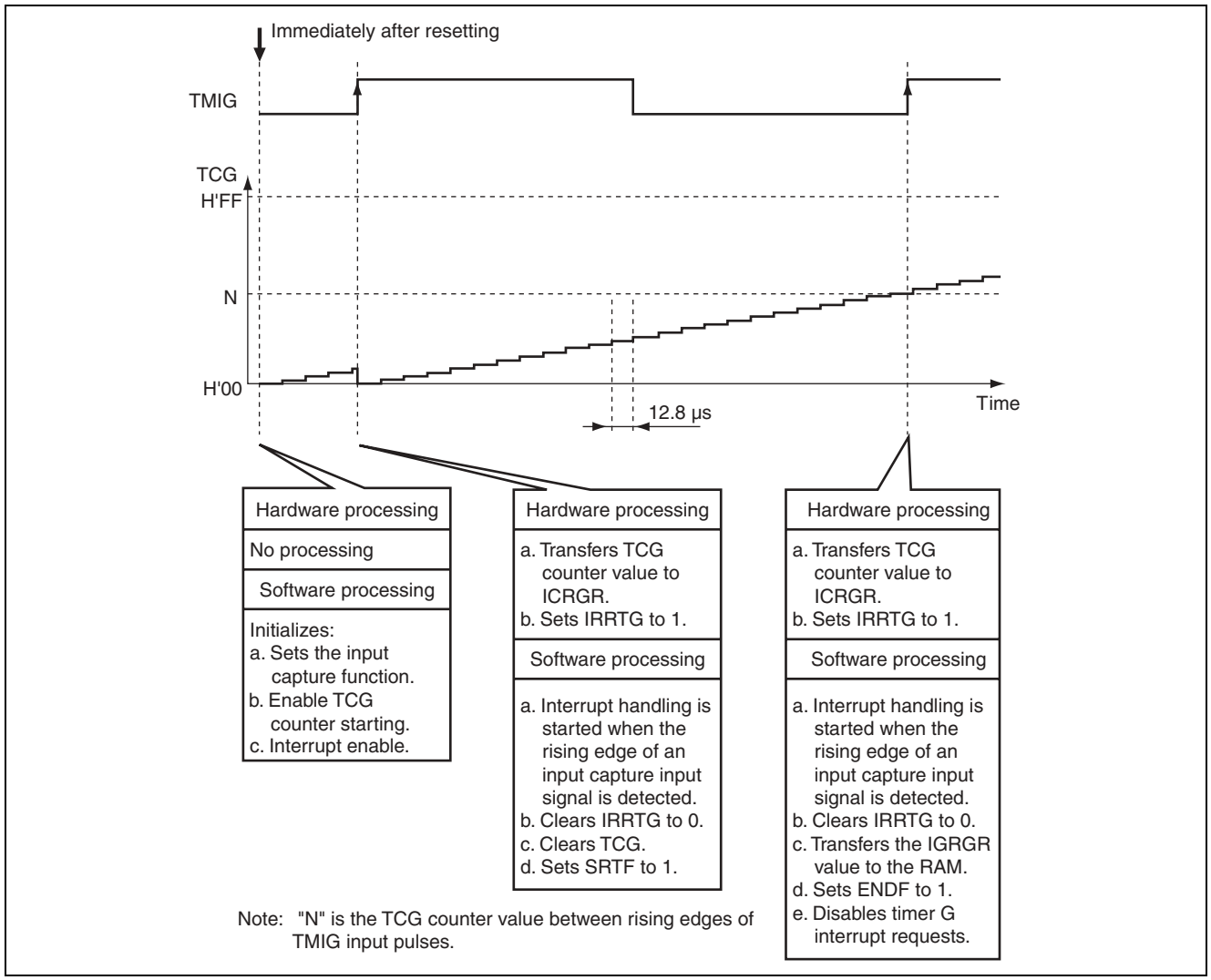


Figure 3.1 Operation Principle of Pulse Period Measurement by Timer G Input Capture Function

4. Description of Software

4.1 Modules

Table 4.1 describes the modules in this task example.

Table 4.1 Description of Modules

Module	Label	Function
Main Routine	main	Sets the timer G input capture function, and enables interrupts.
Period Measurement End	tgint	During the Timer G interrupt handling, initializes TCG to H'00 when the first IRRTG interrupt occurs, stores ICRGR data in the RAM when the second IRRTG interrupt occurs, and disables Timer G interrupt requests.

4.2 Arguments

The arguments used in this task example are described in table 4.2.

Table 4.2 Description of Arguments

Argument	Function	Used in	Data Length	Input/ Output
PRDHL	The counter value between rising edges of TMIG input pulse	Main Routine	1 byte	Output

4.3 Internal registers

Table 4.3 describes the internal registers in this task example.

Table 4.3 Description of Internal Registers

Register		Function	Address	Setting
TMG	OVFH	Timer Mode Register G (Timer Overflow Flag H) If OVFH = 0, the level of input capture input signal is high and TCG does not overflow. If OVFH = 1, the level of input capture input signal is high and TCG overflows.	H'FFBC Bit 7	0
	OVFL	Timer Mode Register G (Timer Overflow Flag L) If OVFL = 0, the level of input capture input signal is low and TCG does not overflow. If OVFL = 1, the level of input capture input signal is low and TCG overflows.	H'FFBC Bit 6	0
	OVIE	Timer Mode Register G(Timer Overflow Interrupt Enable) If OVIE = 0, TCG overflow interrupt requests are disabled. If OVIE = 1, TCG overflow interrupt requests are enabled.	H'FFBC Bit 5	0
	IIEGS	Timer Mode Register G (Input Capture Interrupt Edge Select) If IIEGS = 0, an interrupt is generated at the rising edge of input capture signal. If IIEGS = 1, an interrupt is generated at the falling edge of input capture signal.	H'FFBC Bit 4	0

Register		Function	Address	Setting
TMG	CCLR1 CCLR0	Timer Mode Register G (Counter Clear 1,0) If CCLR1 = 1 and CCLR0 = 0, TCG is cleared at the rising edge of input capture input signal.	H'FFBC Bit 3 Bit 2	CCLR1 = 1 CCLR0 = 0
	CKSH1 CKSH0	Timer Mode Register G (Clock Select 1,0) If CKS1 = 0 and CKS0 = 0, TCG input count is set to $\phi/64$.	H'FFBC Bit 1 Bit 0	CKS1 = 0 CKS0 = 0
TCG		Timer Counter G An 8-bit register which cannot be read from or written to. It is counted up by input clock. When the rising edge of input capture input signal is detected, the value of TCG at that time is transferred to Input Capture Register GR (ICRGR).	—	—
ICRGR		Input Capture Register GR An 8-bit read-only register. When the rising edge of input capture input signal is detected, the value of TCG at that time is transferred to ICRGR.	H'FFBE	—
PMR1	TMIG	Port Mode Register 1 (P13/TMIG Pin Function Switch) If TMIG = 0, P13/TMIG pin functions as P13 input/output pin. If TMIG = 1, P13/TMIG pin functions as TMIG input pin.	H'FFC8 Bit 3	1
PMR2	NCS	Port Mode Register 2 (TMIG Noise Canceler Select) If NCS = 0, the noise cancellation function of input capture input signal is not used. If NCS = 1, the noise cancellation function of input capture input signal is used.	H'FFC9 Bit 1	0
IENR2	IENTG	Interrupt Enable Register 2 (Timer G Interrupt Enable) Controls enable/disable of Timer G interrupt requests. If IENTG = 0, Timer G interrupt requests are disabled. If IENTG = 1, Timer G interrupt requests are enabled.	H'FFF4 Bit 4	1
IRR2	IRRTG	Interrupt Request Register 2 (Timer G Interrupt Request Flag) Indicates whether or not a Timer G interrupt is requested. If IRRTG = 0, a Timer G interrupt is not requested. If IENTG = 1, a Timer G interrupt is requested.	H'FFF7 Bit 4	0

4.4 Description of RAM

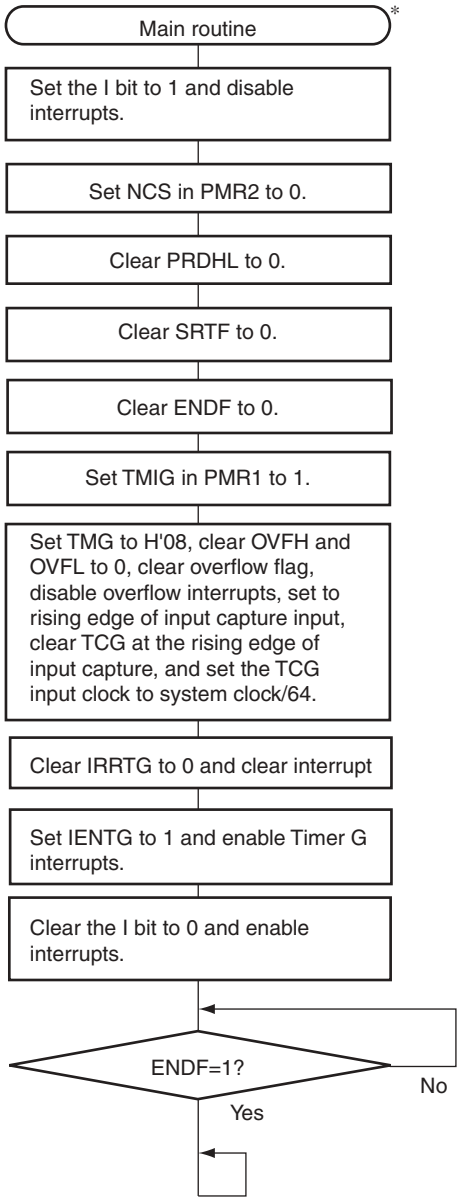
The RAMs used in this task example are described in table 4.4.

Table 4.4 Description of RAM

Label		Function	Address	Used in
PRDHL		Stores the TCG count value between rising edges of the TMIG input captuer input signal	H'FB80	Period Measurement End
USRF	SRTF	Flag to indicate whether or not the interrupt is the second Timer G interrupt	H'FB81 Bit 1	Period Measurement End
	ENDF	Flag to indicate whether or not period measurement has ended	H'FB81 Bit 0	Main Routine Period Measurement End

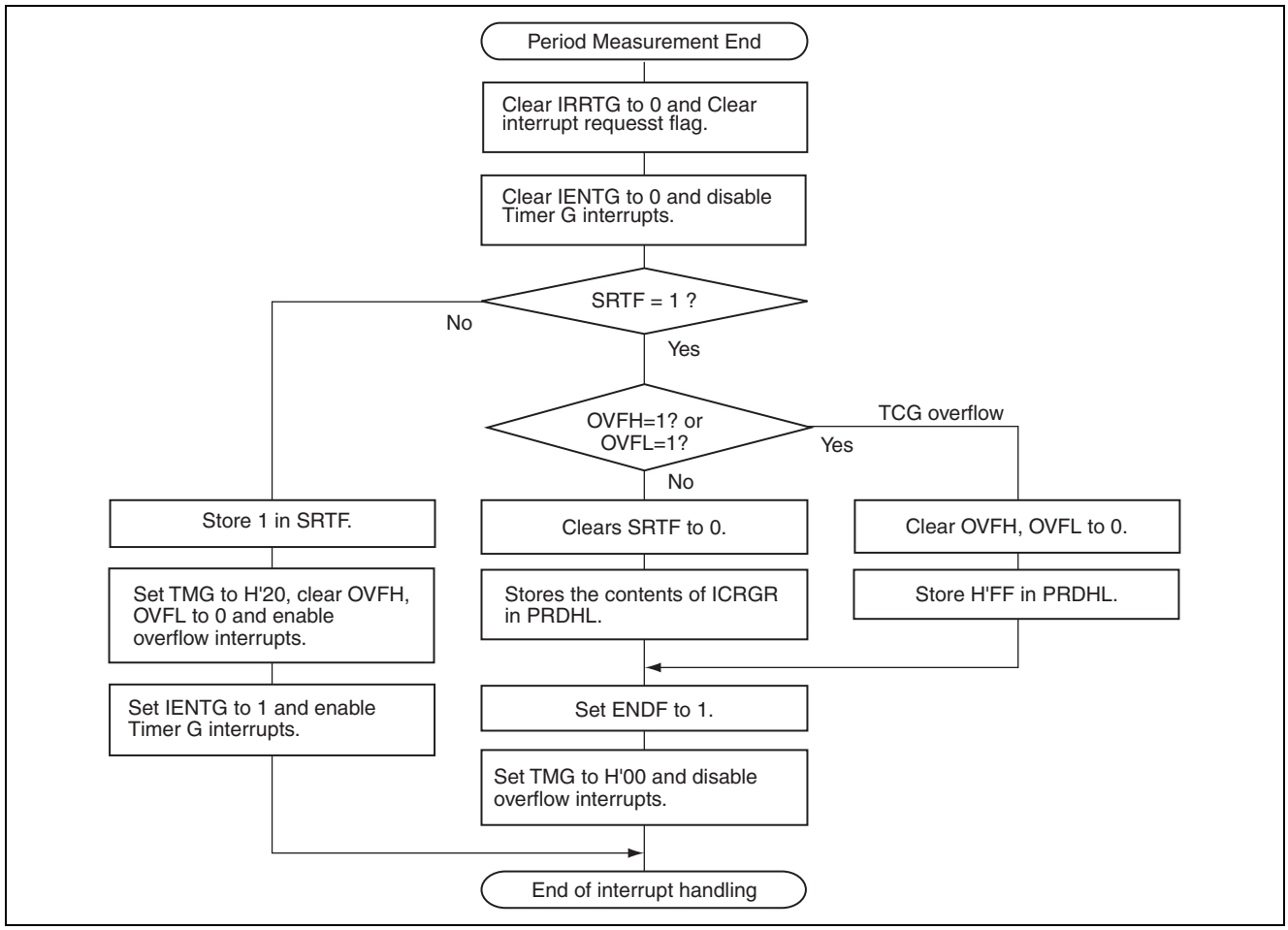
5. Flowchart

1. Main routine



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

2. Timer G Overflow Interrupt routine



6. Program Listing

INIT.SRC (Program listing)

```
    .EXPORT   _INIT
    .IMPORT   _main
;
    .SECTION  P,CODE
_INIT:
    MOV.W     #H'FF80,R7
    LDC.B     #B'10000000,CCR
    JMP       @_main
;
    .END
```

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*  H8/300L Super Low Power Series                                                                                      */
/*      -H8/38024 Series-                                                                                               */
/*  Application Note                                                                                                    */
/*                                                                                                                      */
/*  'Pulse Period Measurement by Input                                                                                  */
/*   Caputure Function'                                                                                                 */
/*                                                                                                                      */
/*  Function                                                                                                            */
/*  : Timer G Input Capture                                                                                             */
/*                                                                                                                      */
/*  External Clock : 10MHz                                                                                              */
/*  Internal Clock : 5MHz                                                                                               */
/*  Sub Clock      : 32.768kHz                                                                                          */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*  Symbol Definition                                                                                                   */
/************************************************************************************************************************/
struct BIT {
    unsigned char    b7:1;      /* bit7 */
    unsigned char    b6:1;      /* bit6 */
    unsigned char    b5:1;      /* bit5 */
    unsigned char    b4:1;      /* bit4 */
    unsigned char    b3:1;      /* bit3 */
    unsigned char    b2:1;      /* bit2 */
    unsigned char    b1:1;      /* bit1 */
    unsigned char    b0:1;      /* bit0 */
};

#define     TMG         *(volatile unsigned char *)0xFFBC        /* Timer Mode Register G                    */
#define     TMG_BIT     (*(struct BIT *)0xFFBC)                  /* Timer Mode Register G                    */
#define     OVFH        TMG_BIT.b7                               /* Timer Overflow Flag H                    */
#define     OVFL        TMG_BIT.b6                               /* Timer Overflow Flag L                    */
#define     OVIE        TMG_BIT.b5                               /* Timer Overflow Interrupt Enable          */
#define     IIEGS       TMG_BIT.b4                               /* Input Caputure Interrupt Edge Select     */
#define     CCLR1       TMG_BIT.b3                               /* Counter Clear 1                          */
#define     CCLR0       TMG_BIT.b2                               /* Counter Clear 0                          */
#define     CKS1        TMG_BIT.b1                               /* Clock Select 1                           */
#define     CKS0        TMG_BIT.b0                               /* Clock Select 0                           */
```

```
#define     ICRGR       *(volatile unsigned char *)0xFFBE       /* Input Caputure Register GR              */
#define     PMR1        *(volatile unsigned char *)0xFFC8       /* Port Mode Register 1                    */
#define     PMR1_BIT    (*(struct BIT *)0xFFC8)                 /* Port Mode Register 1                    */
#define     TMIG        PMR1_BIT.b3                             /* P13/TMIG Input Select                   */
#define     PMR2        *(volatile unsigned char *)0xFFC9       /* Port Mode Register 2                    */
#define     PMR2_BIT    (*(struct BIT *)0xFFC9)                 /* Port Mode Register 2                    */
#define     NCS         PMR2_BIT.b1                             /* TMIG Noise Canceler Select              */
#define     IENR2_BIT   (*(struct BIT *)0xFFF4)                 /* Interrupt Enable Register 2             */
#define     IENTG       IENR2_BIT.b4                            /* Timer G Interrupt Enable                */
#define     IRR2_BIT    (*(struct BIT *)0xFFF7)                 /* Interrupt Request Register 2            */
#define     IRRTG       IRR2_BIT.b4                             /* Timer G Interrupt Request Flag          */

#pragma interrupt   (tgint)
/************************************************************************************************************/
/*  Function define                                                                                         */
/************************************************************************************************************/
extern void INIT ( void );                                      /* SP Set                                  */
void        main ( void );
void        tgint ( void );

/************************************************************************************************************/
/*  RAM define                                                                                              */
/************************************************************************************************************/
unsigned char   PRDHL;                                          /* Period Higher & Lower                   */
unsigned char   USRF;                                           /* User Flag Area                          */

#define     USRF_BIT    (*(struct BIT *)&USRF)
#define     SRTF        USRF_BIT.b1                             /* Start Flag                              */
#define     ENDF        USRF_BIT.b0                             /* End Flag                                */

/************************************************************************************************************/
/*  Vector Address                                                                                          */
/************************************************************************************************************/
#pragma section     V1                                          /* Vector Section Set                      */
void (*const VEC_TBL1[])(void) = {                              /* 0x0000 - 0x000F                         */
    INIT                                                        /* 0x0000 Reset Vector                     */
};
#pragma section     V2                                          /* Vector Section Set                      */
void (*const VEC_TBL2[])(void) = {
    taint                                                       /* 0x0020 Timer G Interrupt Vector         */
};

#pragma section                                                 /* P                                       */
/************************************************************************************************************/
/*  Main Program                                                                                            */
/************************************************************************************************************/
void    main ( void )
{
    int tmp;

    set_imask_ccr(1);                                           /* Interrupt Disable                       */

    NCS = 0;                                                    /* No noise Cancellation circuit           */

    PRDHL = 0;                                                  /* Caputure Data Ramcopy                   */
    SRTF = 0;
    ENDF = 0;

    TMIG = 1;                                                   /* P13/TMIG input selectb                  */
```

```
    tmp = TMG;                                          /* Dummy Read for Flag Clear          */
    TMG  = 0x08;                                        /* Timer Mode Register Set            */

    IRRTG = 0;                                          /* Clear IRRTG                        */
    IENTG = 1;                                          /* Timer G Interrupt Enable           */

    set_imask_ccr(0);                                   /* Interrupt Enable                   */

    while(ENDF ! = 1){                                  /* ENDF = 1 ?                         */
        ;
    }

    while(1){
        ;
    }
}

/*****************************************************************************************************************/
/*  Timer G Interrupt                                                                                            */
/*****************************************************************************************************************/
void    tgint ( void )
{
    int tmp;

    IRRTG = 0;                                          /* Clear IRRTG                        */
    IENTG = 0;                                          /* Timer G Interrupt Disable          */

    if ( SRTF == 1 ){
        if((OVFH == 1)|(OVFL == 1)){
            tmp = TMG;                                  /* Dummy Read for Flag Clear          */
            TMG  = 0;                                   /* Timer Mode Register Set            */
            PRDHL = 0xFF;
        }
        else{
            SRTF = 0;                                   /* Clear SRTF                         */
            PRDHL = ICRGR;                              /* Caputure Data Ramcopy              */
        }
        ENDF = 1;                                       /* Set ENDF                           */
        TMG = 0;                                        /* Overflow Interrupt Disable         */
    }
    else{
        SRTF = 1;                                       /* Set SRTF                           */
        tmp = TMG;                                      /* Dummy Read for Flag Clear          */
        TMG = 0x20;                                     /* Overflow Interrupt Enable          */
        IENTG = 1;                                      /* Timer G Interrupt Enable           */
    }
}
```

Link address specifications

Section Name	Address
CV1	H'0000
CV2	H'0020
P	H'0100
B	H'FB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Dec.19.03	—	First edition issued

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