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H8/300L SLP Series
Using an Infrared Transceiver to Transmit and Receive Character Data

Introduction
Character reception/transmission via a physical layer is performed with a microcomputer to which an infrared light transceiver is connected using an IrDA communication port in a personal computer.

Target Device
H8/38024

Contents

1. Specifications ...................................................................................................................... 2
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6. Program Listing ............................................................................................................ 14
1. Specifications

1. Figure 1.1 shows a hardware structure for data reception/transmission using an infrared light transceiver.
2. In this sample task, a character transmitted from an IrDA port in a personal computer is received by the infrared light transceiver, ASCII code of the received character is incremented, and the character is returned to the personal computer via the infrared light transceiver. On the monitor of the personal computer, a character corresponding to the incremented ASCII code is displayed.
3. In this sample task, the operating voltage (Vcc) and the analog power supply voltage (AVcc) of the H8/38024 are 3.3 V, the OSC clock frequency is 10 MHz, and the watch clock frequency is 32.768 kHz.

![Figure 1.1 Hardware Structure](image)

**Figure 1.1** Hardware Structure

4. The infrared light transceiver used in this sample task is manufactured by ROHM (type name: RPM851A).

![Figure 1.2 Example of Infrared Light Transceiver Operation Timing Chart](image)

**Figure 1.2** Example of Infrared Light Transceiver Operation Timing Chart
A. Features of the RPM851A are as follows.
   a. Conforms to IrDA Ver. 1.0.
   b. Designed for saving current during standby mode (typ. 220 μA)
   c. Most appropriate for using with a battery through a power down control function
   d. Power supply voltage range: 2.7 V to 5.5 V
   e. Package allowing surface mounting on both top and side surfaces

B. Figure 1.2 shows an example of infrared light transceiver operation timing chart.
C. Figure 1.3 shows the block diagram of the infrared light transceiver and an example of the application circuit.

Figure 1.3  Block Diagram of Infrared Light Transceiver and Example of Application Circuit

5. This sample task operates as follows.
   A. Communication via a physical layer is performed by a terminal software in a personal computer using a waveform of IrDA 1.0.
   B. For example, a character '!' corresponding to ASCII code 'H31' is input from the keyboard of the personal computer.
   C. A modulated signal is transmitted from the IrDA port of the personal computer in LSB first.
   D. The infrared light transceiver connected to a microcomputer receives the signal and captures data 'H31'.
   E. The microcomputer increments the data to 'H32', modulates it, and immediately returns it via the infrared light transceiver.
   F. The signal received by the IrDA port of the personal computer is demodulated, and 'H32' is captured. '2' is displayed on the monitor since the ASCII code 'H32' corresponds to the character '2'.

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2. Description of Functions

1. Figure 2.1 shows a block diagram of functions of the H8/38024 in this sample task; table 2.1 shows function allocations.

![Block Diagram of Functions](image)

**Figure 2.1 Block Diagram of Functions**

<table>
<thead>
<tr>
<th>Function</th>
<th>Function Allocation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer F</td>
<td>Outputs toggle signal using a compare-match function. Changes the output frequency by setting a value to the output compare register (OCRFL).</td>
</tr>
<tr>
<td>Port 1</td>
<td>Transmits infrared ray data from P17 output pin of port 1</td>
</tr>
<tr>
<td>Port 7</td>
<td>Receives infrared ray data from P83 input pin of port 8</td>
</tr>
</tbody>
</table>
3. Principles of Operation

1. Figure 3.1 shows the principle of operation when infrared ray communication is performed using the timer F. Transmission is performed through a timer F compare-match interrupt, and reception is performed by using a TCFL value without using an interrupt.

![Principle of Operation of Infrared Ray Communication Using Timer F](image-url)

**Figure 3.1 Principles of Operation of Infrared Ray Communication Using Timer F**
4. **Description of Software**

4.1 **Modules**

Table 4.1 describes the modules used in this sample task.

<table>
<thead>
<tr>
<th>Module</th>
<th>Label</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>main</td>
<td>Initializes, and calls infrared ray data reception processing routine and infrared ray data transmission processing routine alternately</td>
</tr>
<tr>
<td>Infrared ray data reception</td>
<td>irda_rcv</td>
<td>Receives data through an infrared ray</td>
</tr>
<tr>
<td>Infrared ray data transmission</td>
<td>irda_snd</td>
<td>Transmits data through an infrared ray</td>
</tr>
<tr>
<td>Timer F interrupt processing</td>
<td>tmrw</td>
<td>This is used as a 52-µs timer</td>
</tr>
</tbody>
</table>

4.2 **Arguments**

This sample task does not use arguments.

4.3 **Internal Registers**

The internal registers used in this sample task are described in table 4.2.

<table>
<thead>
<tr>
<th>Register</th>
<th>Function</th>
<th>Address</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCRF</td>
<td>Timer control register F</td>
<td>H'FFB6</td>
<td>H'66 (initial setting)</td>
</tr>
<tr>
<td></td>
<td>Switches over 16-bit/8-bit mode, selects from four internal clocks and external events, and sets the TMOFH/TMOFL pin output level.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TOLH</td>
<td>Toggle output level H</td>
<td>Bit 7</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Sets the TMOFH pin output level.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When TOLH = 0: Low.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CKSH2</td>
<td>Clock select H</td>
<td>Bit 6</td>
<td>1</td>
</tr>
<tr>
<td>CKSH1</td>
<td>When CKSH2 = 1, CKSH1 = 1, and CKSH0 = 0, counts with the internal clock ϕ/4.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CKSH0</td>
<td></td>
<td>Bit 5</td>
<td>1</td>
</tr>
<tr>
<td>TOLL</td>
<td>Toggle output level L</td>
<td>Bit 4</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Sets the TMOFL pin output level.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When TOLL = 0: Low.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CKSL2</td>
<td>Clock select L</td>
<td>Bit 3</td>
<td>0</td>
</tr>
<tr>
<td>CKSL1</td>
<td>When CKSL2 = 1, CKSL1 = 1, and CKSL0 = 0, counts with the internal clock ϕ/4.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CKSL0</td>
<td></td>
<td>Bit 2</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 0</td>
<td>0</td>
</tr>
<tr>
<td>Register</td>
<td>Function</td>
<td>Address</td>
<td>Setting</td>
</tr>
<tr>
<td>------------</td>
<td>--------------------------------------------------------------------------</td>
<td>----------</td>
<td>-----------</td>
</tr>
<tr>
<td>TCSRF</td>
<td>Timer control/status register F</td>
<td>H'FFB7</td>
<td>H'01</td>
</tr>
<tr>
<td></td>
<td>Selects counter clear, sets overflow flag, sets compare-match flag</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>enables/disables overflow interrupt request</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OVFH</td>
<td>Timer overflow flag H</td>
<td>Bit 7</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Status flag which indicates that the TCFH overflow (H'FF → H'00) has</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>occurred.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMFH</td>
<td>Compare-match flag H</td>
<td>Bit 6</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Status flag which indicates that TCFH and OCRFH match.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OvieH</td>
<td>Timer overflow interrupt enable H</td>
<td>Bit 5</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>When OvieH = 0, disables TCFH overflow interrupt requests.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CCLRH</td>
<td>Counter clear H</td>
<td>Bit 4</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>When CCLRH = 1, enables TCF clear when compare-match occurs.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OVFL</td>
<td>Timer overflow flag L</td>
<td>Bit 3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Status flag which indicates that TCFL overflow (H'FF → H'00) has</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>occurred.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMFL</td>
<td>Compare-match flag L</td>
<td>Bit 2</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Status flag which indicates that TCFL and OCRFL match.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OvieEL</td>
<td>Timer overflow interrupt enable L</td>
<td>Bit 1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>When OvieEL = 0, disables TCFL overflow interrupt requests.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CCLR L</td>
<td>Counter clear L</td>
<td>Bit 0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>When CCLR L = 1, enables TCFL clear when compare-match occurs.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TCFL</td>
<td>8-bit timer counter</td>
<td>H'FFB9</td>
<td>H'00</td>
</tr>
<tr>
<td></td>
<td>An 8-bit readable/writable up-counter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OCRFL</td>
<td>16-bit output compare register</td>
<td>H'FFBB</td>
<td>255/65</td>
</tr>
<tr>
<td></td>
<td>Generates interrupts when a value matches with TCFL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CKSTPR1</td>
<td>Clock stop register 1</td>
<td>H'FFFFA</td>
<td>H'FB/H'FF</td>
</tr>
<tr>
<td></td>
<td>Controls module standby mode.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When TFCKSTP = 0 (CKSTPR1 = H'FB): sets timer F to module standby mode.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When TFCKSTP = 1 (CKSTPR1 = H'FF): cancels timer F module standby mode.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IENR2</td>
<td>Interrupt enable register 2</td>
<td>H'FFF4</td>
<td>H'04/H'00</td>
</tr>
<tr>
<td>IENTFL</td>
<td>When IENTFL = 0, enables timer FL interrupt requests</td>
<td>Bit 2</td>
<td>1/0</td>
</tr>
<tr>
<td>IRR2</td>
<td>Interrupt request register 2</td>
<td>H'FFF7</td>
<td>H'00</td>
</tr>
<tr>
<td>IRRTFL</td>
<td>This register can be cleared when 0 is written to IRRTFL while</td>
<td>Bit 2</td>
<td>1/0</td>
</tr>
<tr>
<td></td>
<td>IRRTFL = 1.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>This register is set to 1 when TCFL and OCRFL match in 8-bit timer mode.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCR1</td>
<td>Port control register 1</td>
<td>H'FFE4</td>
<td>H'80</td>
</tr>
<tr>
<td></td>
<td>Selects, for each bit, the pin I/O to use as the port 1 general-</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>purpose I/O port.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When PCR1 = H'80, pin P17 functions as a general-purpose</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>output pin, and other pins function as general-purpose input pins.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Using an Infrared Transceiver to Transmit and Receive
4.4 Description of RAM

Table 4.3 describes the RAM used in this sample task.

Table 4.3 Description of RAM

<table>
<thead>
<tr>
<th>Label</th>
<th>Function</th>
<th>Address</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>sdata</td>
<td>Transmit data (1 byte)</td>
<td>H'FB86</td>
<td>main, tmrw</td>
</tr>
<tr>
<td>rdata</td>
<td>Receive data (1 byte)</td>
<td>H'FB87</td>
<td>main, tmrw</td>
</tr>
<tr>
<td>bitdata</td>
<td>Store 10-bit transmit data (10 bytes)</td>
<td>H'FB88</td>
<td>main, tmrw</td>
</tr>
<tr>
<td>i</td>
<td>Store loop counter (2 bytes)</td>
<td>H'FB80</td>
<td>input_key</td>
</tr>
<tr>
<td>j</td>
<td>Store loop counter (2 bytes)</td>
<td>H'FB82</td>
<td>input_key</td>
</tr>
<tr>
<td>bit</td>
<td>Store bit data during reception (1 byte)</td>
<td>H'FB92</td>
<td>main</td>
</tr>
<tr>
<td>indata</td>
<td>Store input data (1 byte)</td>
<td>H'FB93</td>
<td>input_key</td>
</tr>
<tr>
<td>Wtimeup</td>
<td>Timer F timeup flag (2 bytes)</td>
<td>H'FB84</td>
<td>input_key</td>
</tr>
<tr>
<td>bitpos</td>
<td>For bit on/off determination (1 byte)</td>
<td>H'FB94</td>
<td>input_key</td>
</tr>
<tr>
<td>dummy</td>
<td>Dummy (1 byte)</td>
<td>H'FB95</td>
<td></td>
</tr>
</tbody>
</table>
5. Flowchart

1. Main routine

```
Main

CCR l-bit ← 1

Port 1 initial settings
P17/IRQ3/TMIF: P17 output pin (output data = 0).

PCR1 ← H'80

Port 8 initial settings
P83/SEG28: P83 input pin

PCR8 ← H'F7

Set clock (φ/4)

TCRF ← H'66

Enable TCFL clear when compare-matches occurs.

TCSRF ← H'01

IrDA reception processing.

irda_rcv

set 'received data + 1' as transmit data.

sdata ← data + 1

IrDA transmission processing.

ida_snd
```

Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).
2. Infrared ray data reception processing routine (irda_recv)

```
irda_recv
indata ← 0  --------------- Initialize input data.
CKSTPR1 ← H'FF

Yes
PDR8 ! = 0 ?
No

TCFL ← H'00  --------------- Clear the timer counter FL to 0.
OCRFL ← H'FF  --------------- Set the output compare register.

Yes
TCFL < 35 ?
No

i ← 0

TCFL ← H'00  --------------- Clear the timer counter FL to 0.
OCRFL ← H'FF  --------------- Set the output compare register.
```

Delay.
Using an Infrared Transceiver to Transmit and Receive

```
1

dummy ← indata

bit ← PDR8

dummy ← indata

indata ← indata >> 1

Is the input bit High?

bit ! = 0 ?

Yes

Set the bit to on.

indata ← indata | H'80

No

Delay.

TCFL < 56

Yes

8 bits or less?

i < 8

No

Delay.

i < 8

Yes

CKSTPR1 ← HFB

rdata ← indata

RTE

2

---- Delay.

---- Read bit data twenty times.

---- Delay.

---- Shift a bit.

i ← i + 1

Increment the bit by 1
```
3. Infrared ray data transmission processing routine (irda_snd)

```plaintext
irda_snd

bitpos ← H'01  Initialize the bit position.
i ← 0  Initialize the bit counter.

Start bit?  Yes

i = 0?
No  Stop bit?  Yes

i = 9?
No  Is transmit data off?  Yes

(bitpos & sdata) = 0 ?
No  Set to off

bitdata[i] ← 0  Set to on

bitpos ← bitpos << 1  Change to the next bit position

Within 10 bits?  Yes

i < 10 ?
No

CKSTPR1 ← H'FF

TCFL ← H'00  Clear timer counter FL to 0.

OCRFL ← 65  65 → 52 µs

IENR2 ← H'04  Set timer FL compare match interrupt enable to on.

CCR i-bit ← 0  Enable interrupt.
```

bitdata[0] ← 1

bitdata[9] ← 0

i ← i + 1
1. Initialize the timeup flag.
2. Initialize the bit counter.
3. Is timer F operating?
   - Yes
     - Transmit bit data.
     - Delay
     - Transmit bit data.
     - Return to Low.
   - No
     - Increment the bit counter by 1.
     - Initialize the timeup flag.
     - Increment the bit counter by 1.
     - Is timer F operating?
     - Yes
       - Increment the bit counter by 1.
     - No
       - Set the timer FL compare match interrupt enable to off.
       - Disable interrupt.
       - Set the clock F standby mode to on.
       - Return

4. Timer F interrupt processing routine (tmrw)

   tmrf

   No

   IRRTFL = 1 ?
   - Yes
     - Clear the timer FL compare match flag to 0.
       - Clear the timeup flag to 0.
     - RTE
   - Is the timer FL compare match flag set to on?

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6. Program Listing

INIT.SRC (Program listing)

```
.EXPORT _INIT
.IMPORT _main
;
.SECTION P, CODE
_INIT:
    MOV.W #H'FF80,R7
    LDC.B #B'10000000,CCR
    JMP @_main
;
.END
```

มือ-include <machine.h>

```
#include <machine.h>
```

```
/* H8/300L Super Low Power Series */
/* —H8/38024 Series— */
/* Application Note */
/* */
/* * Using an Infrared Transceiver to Transmit and Receive Character Data */
/* */
/* */
/* Function */
/* : IrDA */
/* */
/* External Clock : 10MHz */
/* Internal Clock : 5MHz */
/* Sub Clock : 32.768kHz */
/* */
```

```
#include <machine.h>

/* Symbol Definition */
```

```
struct BIT {
    unsigned char   b7:1;       /* bit7 */
    unsigned char   b6:1;       /* bit6 */
    unsigned char   b5:1;       /* bit5 */
    unsigned char   b4:1;       /* bit4 */
    unsigned char   b3:1;       /* bit3 */
    unsigned char   b2:1;       /* bit2 */
    unsigned char   b1:1;       /* bit1 */
    unsigned char   b0:1;       /* bit0 */
};
```

```
#define    PDR1         *(volatile unsigned char *)0xFFD4        /* Port Data Register 1                     */
#define    PDR1_BIT     (*(struct BIT *)0xFFD4)
#define    TXD          PDR1_BIT.b7                              /* Transfer Data                            */
#define    PCR1         *(volatile unsigned char *)0xFFE4        /* Port Control Register 1                  */
#define    PDR8         *(volatile unsigned char *)0xFFDB        /* Port Data Register 8                     */
#define    PDR8_BIT     (*(struct BIT *)0xFFDB)
#define    RXD          PDR8_BIT.b1                              /* Receive Data                             */
#define    PCR8         *(volatile unsigned char *)0xFFEB        /* Port Control Register 8                  */
```
#define TCRF *(volatile unsigned char *)0xFFB6        /* Timer Control Register F */
#define TCSRFP *(volatile unsigned char *)0xFFB7        /* Timer Control Status Register F */
#define TCFR BIT (*(struct BIT *)0xFFB7)
#define CMFL TCFR_BIT.b2                             /* Compare-Match Flag L */
#define TCF *(volatile unsigned int *)0xFFB8        /* 16 bit Timer Counter F */
#define TCFH *(volatile unsigned char *)0xFFB8        /* 8 bit Timer Counter F(HIGH) */
#define TCFL *(volatile unsigned char *)0xFFB9        /* 8 bit Timer Counter F(LOW) */
#define OCRF *(volatile unsigned int  *)0xFFBA        /* 16 bit Output Compare Register */
#define OCRFH *(volatile unsigned char *)0xFFBA        /* 8 bit Output Compare Register F(HIGH) */
#define OCRFL *(volatile unsigned char *)0xFFBB        /* 8 bit Output Compare Register F(LOW) */
#define CKSTPR1 *(volatile unsigned char *)0xFFFA        /* Clock Stop Register 1 */
#define IENR2 *(volatile unsigned char *)0xFFF4        /* Interrupt Enable Register 2 */
#define IRR2 *(volatile unsigned char *)0xFFF7        /* Interrupt Request Register 2 */
#define IRR2_BIT (*(struct BIT *)0xFFF7)
#define IRR2_BIT.b2 IRR2_BIT.b3 /* Timer FL Interrupt Enable */

#pragma interrupt (tmrf)
/******************************************************************************
/* Function Define
*******************************************************************************/
extern void INIT( void );                                      /* Stack Pointer Set */
void main(void);                                               /* Main Routine */
void irda_rcv(void);                                            /* Main Routine */
void irda_snd(void);                                            /* Main Routine */
void tmrf(void);                                                /* Timer A Interrupt Routine */

/******************************************************************************
/* RAM Define
*******************************************************************************/
volatile unsigned char   sdata;                                  /* Send Data */
volatile unsigned char   rdata;                                  /* Receive Data */
unsigned char bitdata[10];                                      /* Bit Data (send) */
int i,j;                                                         /* Loop Counter */
unsigned char bit, indata;                                      /* Input Data */
volatile int   Wtimeup;                                           /* F Timer Time Up */
unsigned char bitpos;                                           /* Bit Position */
char dummy;

/******************************************************************************
/* Vector Address
*******************************************************************************/
#pragma section V1                                              /* Vector Section Set */
void (*const VEC_TBL1[])(void) = {                               /* 0x0000 Reset Vector */
  INIT
/**
};
#pragma section V2                                              /* Vector Section Set */
void (*const VEC_TBL2[])(void) = {                               /* 0x001C Timer F Interrupt Vector */
  tmrf
/**
};
#pragma section                                                  /* P */
void main( void )
{
    set_imask_ccr(1); /* CCR I-bit = 1 */
    PCR1 = 0x80; /* Initialize for IrDA */
    PCR8 = 0xF7;
    TCRF = 0x66; /* Set Internal Clock: phi/4 */
    TCSR8 = 0x01; /* Enable TCF Clear */

    while(1){
        irda_rcv(); /* Receive Routine */
        sdata = rdata + 1;
        irda_snd(); /* Send Routine */
    }
}

void irda_rcv( void )
{
    indata = 0; /* Input Data Initialize */
    CKSTPR1 = 0xFF; /* Clock F STAND-BY-MODE OFF */

    while(PDR8);
    TCFL = 0x00; /* Clear Timer Counter FL to 0 */
    OCRFL = 0x0FF; /* Set Output Compare Register */
    while(TCFL < 35); /* 28us */

    for(i = 0; i<8; i++)
    {
        TCFL = 0x00; /* Clear Timer Counter FL to 0 */
        OCRFL = 0x0FF; /* Set Output Compare Register */
        dummy = indata; /* Dummy Wait(8 cycle) */
        dummy = indata; /* Dummy Wait(8 cycle) */
        indata >> = 1; /* Shift Input Data */
        if(bit) { /* If Input is High level */
            indata | = 0x80; /* Then Data Set */
        }
        while(TCFL < 56); /* 44.8us */
    }
    CKSTPR1 = 0xFB; /* Clock F STAND-BY-MODE ON */

    rdata = indata;
}
/* Send Routine */

void irda_snd( void )
{
    /* Set Send Data */
    bitpos = 0x01; /* Set Bit Position (0 Bit) */
    for(i = 0; i < 10; i++) {
        if(i == 0) {
            bitdata[0] = 1; /* Set Start Bit */
        } else if(i == 9) {
            bitdata[9] = 0; /* Set Stop Bit */
        } else {
            if((bitpos & sdata) == 0) { /* Set Data Bit */
                bitdata[i] = 1;
            } else {
                bitdata[i] = 0;
            }
            bitpos <<= 1; /* Shift Bit Position */
        }
    }
    CKSTPR1 = 0xFF; /* Clock F STAND-BY-MODE OFF */
    TCFL = 0x00; /* Clear Timer Counter FL to 0 */
    OCRFL = 65; /* Set Output Compare Register */
    IENR2 = 0x04; /* FL Interrupt Enable */
    set_imask_ccr(0); /* CCR I-bit = 0 */

    Wtimeup = 1;
    for(i = 0; i < 10; i++) {
        while(Wtimeup); /* Wait 52us */
        TXD = bitdata[i]; /* TXD ON */
        for(j = 0; j < 1; j++); /* TXD OFF */
        Wtimeup = 1;
    }
    IENR2 = 0x00; /* FH Interrupt Disable */
    set_imask_ccr(1); /* CCR I-bit = 1 */
    CKSTPR1 = 0xFB; /* Clock F STAND-BY-MODE ON */
}

/* Timer F Interrupt (every 52us) */

void tmrf(void)
{
    if ( IRRTFL == 1 ) {
        IRRTFL = 0; /* Clear Compare Match Flag A */
        Wtimeup = 0; /* Set Time Up */
    }
}
## Link address specifications

<table>
<thead>
<tr>
<th>Section Name</th>
<th>Address</th>
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<tbody>
<tr>
<td>CV1</td>
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<tr>
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# Revision Record

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