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---

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Renesas Electronics Corporation

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H8/300L SLP Series
Using an Infrared Remote Controller in Transmission and Reception

Introduction
Timers C and F are used for transmission by the infrared remote controller.

Target Device
H8/38024

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1. Specifications

1. Timers C and F are used for transmission by the infrared remote controller.
2. Timer G is used for reception by the infrared remote controller.
3. The sample task is such that the key switches (0 to 9 and A to F) connected to the transmit side are pressed to display their key numbers on the LCD on the receive side.
4. The infrared remote controller operates in half-duplex communications mode.
5. Figure 1.1 shows the connection of the infrared remote controller.

![Diagram of Infrared Remote Controller Connection](image.png)

Figure 1.1 Example of Connection of Infrared Remote Controller
2. Concepts

1. Figure 2.1 shows examples of signals for infrared remote control processing used in the sample task. The infrared light reception element used for the sample task outputs the low level when it receives a carrier frequency of 38 kHz.

![Waveform transmitted by infrared remote controller](image)

![Waveform received by infrared remote controller](image)

**Figure 2.1 Examples of Signals Used for Infrared Remote Control Processing**

2. Discrimination between 0 and 1

The sample task discriminates between 0 and 1 depending on the length of the carrier wave.

![Signal 0 transmission](image)

![Signal 0 reception](image)

![Signal 1 transmission](image)

![Signal 1 reception](image)

**Figure 2.2 Discrimination between 0 and 1**
3. Description of Functions

1. Table 3.1 lists specifications of infrared light-emitting diode GL538 used for the sample task. Table 3.2 lists specifications of infrared light reception device NJL71V380A used for the sample task. (If stands for the forward current, Ifm for the peak forward current, and Vr for the reverse voltage.)

Table 3.1 Specifications of Infrared Light-Emitting Diode

<table>
<thead>
<tr>
<th>Item</th>
<th>Condition</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Product type</td>
<td>—</td>
<td>GL538</td>
</tr>
<tr>
<td>Manufacturer</td>
<td>—</td>
<td>SHARP CORPORATION</td>
</tr>
<tr>
<td>Operating power supply voltage Vf</td>
<td>If = 50 mA</td>
<td>1.3 V to 1.5 V</td>
</tr>
<tr>
<td>Peak forward voltage Vfm</td>
<td>Ifm = 0.5 A</td>
<td>1.9 V to 3.0 V</td>
</tr>
<tr>
<td>Reverse current Ir</td>
<td>Vr = 3 V</td>
<td>10 µA</td>
</tr>
<tr>
<td>Emitted peak waveform λp</td>
<td>If = 5 mA</td>
<td>950 nm</td>
</tr>
<tr>
<td>Half-value waveform ∆λ</td>
<td>If = 5 mA</td>
<td>45 nm</td>
</tr>
<tr>
<td>Emitted output Ie</td>
<td>If = 50 mA</td>
<td>15 to 30 mW/sr</td>
</tr>
<tr>
<td>Half-value angle ∆θ</td>
<td>If = 20 mA</td>
<td>±13 deg</td>
</tr>
<tr>
<td>Oscillation</td>
<td>—</td>
<td>300 kHz</td>
</tr>
</tbody>
</table>

Table 3.2 Specifications of Infrared Light Reception Device

<table>
<thead>
<tr>
<th>Item</th>
<th>Condition</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Product type</td>
<td>—</td>
<td>NJL71V380A</td>
</tr>
<tr>
<td>Manufacturer</td>
<td>—</td>
<td>New Japan Radio Co., Ltd.</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>—</td>
<td>38 kHz</td>
</tr>
<tr>
<td>Operating power supply voltage</td>
<td>—</td>
<td>2.4 V to 5.5 V</td>
</tr>
<tr>
<td>Current consumption</td>
<td>No incident light</td>
<td>0.6 mA (Maximum value)</td>
</tr>
<tr>
<td>Reach</td>
<td>Optical axis center direction, carrier frequency</td>
<td>18 m</td>
</tr>
<tr>
<td>Vertical half-value angle</td>
<td>Horizontal directivity at the half of the reach</td>
<td>45 deg</td>
</tr>
<tr>
<td></td>
<td>Vertical directivity at the half of the reach</td>
<td>30 deg</td>
</tr>
<tr>
<td>Low-level output voltage</td>
<td>30 cm in the optical axis direction</td>
<td>0.5 V (Maximum value)</td>
</tr>
<tr>
<td>High-level output voltage</td>
<td>30 cm in the optical axis direction</td>
<td>2.8 V</td>
</tr>
<tr>
<td>Low-level pulse width (TwL)</td>
<td>Defined by the period width of output TwL and TWH in the range from 30 cm in the optical axis direction to the reach. (Average value of 50 pulses)</td>
<td>350 to 800 µs</td>
</tr>
<tr>
<td>High-level pulse width (TWH)</td>
<td>—</td>
<td>400 to 850 µs</td>
</tr>
</tbody>
</table>
2. This paragraph explains the functions supported by the infrared remote controller.  
A. Figure 3.1 shows the block diagram of the H8/38024 functions used for infrared remote control processing.

**Figure 3.1 Block Diagram of Infrared Remote Control Processing**

B. The following explains the H8/38024 functions supported by the infrared remote controller.

- **System clock (ϕ)**  
  This is a 5-MHz clock obtained by dividing the 10-MHz OSC clock by two, being the reference clock used to operate the CPU and its peripheral functions.

- **Prescaler S (PSS)**  
  This is a 13-bit counter that receives ϕ as the input, counting up every cycle.

- **Port 4**  
  Uses P42 as the output pin to output the carrier wave.

- **Port 5**  
  This port is connected to the key switch to select infrared transmit data.

- **Timer C automatic reloading function**  
  Controls the interval between carrier wave output and termination.

- **Timer F compare match function**  
  Generates the 38-kHz carrier wave.

- **Timer G input capture function**  
  Receives an output value from the infrared light reception device for receive data determination.

- **LCD controller/driver**  
  Displays receive data on the LCD.
3. This paragraph explains the functions supported by port 4.

   A. Figure 3.2 shows the block diagram of carrier wave transmission by port 42.

   ![Figure 3.2 Block Diagram of Port 4]

   B. The sample task uses port 42 to output a carrier wave. The following explains the block diagram of port 4.
   
   - Port control register 4 (PCR4)
     Sets input/output for port 4. When PCR4 = 0xFC, PCR4 sets P42 as the output port.
   
   - Port data register 4 (PDR4)
     Sets data to be stored into output port P42. Using timer F interrupt, PDR4 toggles P42 to output the 38-kHz carrier wave.

4. This paragraph explains the functions supported by port 5.

   A. Figure 3.3 shows the block diagram of the key input circuit supported by port 5.

   ![Figure 3.3 Block Diagram of Key Input Circuit Supported by Port 5]

   B. The sample task uses port 5 for key input. The following explains the block diagram of the key input circuit.
   
   - Port control register 5 (PCR5)
     Sets input/output for port 5. When PCR5 = 0xF0, PCR5 sets P54 to P57 as the output ports, and P50 to P53 as the input ports.
   
   - Port data register 5H (PDR5H)
     Uses the upper four bits of PDR5 as PDR5H to set data to be stored into output ports P54 to P57. Out of P54 to P57, the status of a key row set at the low level is reflected in P50 to P53.

   - Port data register 5L (PDR5L)
     Uses the lower four bits of PDR5 as PDR5L to reflect the values of input ports P50 to P53 in PDR5L. The value stored in PDR5L provides the status of a key row selected by PDR5H.
5. This paragraph explains the timer C automatic reloading function.
   A. Figure 3.4 shows the block diagram of the timer C automatic reloading function.

   ![Block Diagram of Timer C Automatic Reloading Function](image)

   **Figure 3.4 Block Diagram of Timer C Automatic Reloading Function**

   B. The following explains the block diagram of the timer C automatic reloading function.
   - **Timer mode register C (TMC)**
     This is an eight-bit readable/writable register that selects the automatic reloading function, controls increment/decrement of the timer counter C (TCC), and selects an input clock. For control over the increment/decrement of TCC, it selects hardware control by UD pin input, or the up/down counter by software control.
   - **Timer counter C (TCC)**
     This is an eight-bit readable counter that is counted up or down by an internal input clock or an external event. As the input clocks, the system clock divided by 8192, 2048, 512, 64, 16, or 4, the watch clock divided by 4, and an external clock can be selected. The sample task sets TCC as the up-counter, and selects the system clock divided by 64 as the TCC input clock.
   - **Timer load register C (TLC)**
     This is an eight-bit write-only register that sets a value to be reloaded to TCC.
   - **Timer C interrupt request flag (IRRTC)**
     This flag is set to 1 by a TCC overflow. A timer C interrupt is accepted with the IRRTC at 1, the timer C interrupt enable (IENTC) for the interrupt enable register 2 (IENR2) set at 1, and bit 1 in the condition code register (CCR) cleared to 0. Then, timer C interrupt processing starts.
6. This paragraph explains the timer F output compare function.
   A. Figure 3.5 shows the block diagram of the timer F output compare function.

   ![Block Diagram of Timer F Output Compare Function](image)

   **Figure 3.5 Block Diagram of Timer F Output Compare Function**

   B. The following explains the block diagram of the timer F output compare function.
   - Timer counter FH (TCFH)
     This is an eight-bit readable/writable up-counter that is incremented by an input internal/external clock. Four internal clocks obtained by dividing \( \phi \), and one external clock can be selected as the input clock.
   - Timer control register F (TCRF)
     This is an eight-bit writable register that sets the TCFH input clock. The sample task uses \( \phi \) divided by four as the TCFH input clock.
   - Timer control status register F (TCSRIF)
     This is an eight-bit register that selects counter clearing, sets the compare match flag and timer overflow flag, and controls enabling an interrupt request resulting from an overflow. The sample task enables TCFH clearing by a compare match FH, and disables an interrupt resulting from a timer FH overflow.
   - Output compare register FH (OCRFH)
     This is an eight-bit readable/writable register. The contents of OCRFH are always compared with that of TCFH. If they match, the compare match flag H (CMFH) in TCSRIF is set to 1. Then, a compare match FH is generated, requesting a CPU interrupt.
7. This paragraph explains the timer G input capture function.
   A. Figure 3.6 shows the block diagram of the timer G input capture function.

   ![Block Diagram of Timer G Input Capture Function](image)

   **Figure 3.6 Block Diagram of Timer G Input Capture Function**

   B. The following explains the timer G input capture function.
   - **Timer counter G (TCG)**
     This is an eight-bit unreadable/unwritable up-counter that is incremented by an input internal/external clock. As the input clocks, the system clock divided by 2, 32, and 64, and an external clock can be selected. The sample task selects the system clock divided by 64 as the TCG input clock.
   - **Timer mode register G (TMG)**
     This is an eight-bit readable/writable register that selects the TCG input clock, counter clearing, and the edge of an interrupt request by an input capture input signal, controls enabling/disabling an interrupt request resulting from an overflow, and displays the overflow flag.
   - **Input capture register GR (ICRGR)**
     This is an eight-bit read-only register that transfers the TCG value to ICRGR upon detection of the rising edge of the input capture input signal. When the IRRTG bit in IRR2 is set to 1, a CPU interrupt is requested.
   - **Input capture input pin (TMIG)**
     Receives an output value from the infrared light reception device, measuring the low and high periods.
8. This paragraph explains the LCD controller/driver.
   A. Figure 3.7 shows the block diagram of the LCD controller/driver.

![Figure 3.7 Block Diagram of LCD Controller/Driver]

B. The following explains the functions supported by the LCD controller/driver.
   - LCD port control register (LPCR)
     This is an eight-bit readable/writable register that selects a duty cycle, LCD driver, and pin functions.
   - LCD control register (LCR)
     This is an eight-bit readable/writable register that turns on or off the LCD drive power supply, controls the start of the display function and display data, and selects a frame frequency.
   - LCD control register 2 (LCR2)
     This is an eight-bit readable/writable register that controls waveform A or B selection, and selects a clock for the triple step-up circuit, a drive power supply, and a duty cycle in a period when the split-resistor for the power supply is connected to the power supply circuit.
   - Segment output pins (SEG1 to SEG32)
     These pins are used to drive the LCD segment. All pins are shared with ports and can be set in a programmable way.
   - Common output pins (COM1 to COM4)
     These are the common drive pins for the LCD. In static or 1/2 duty cycle mode, pins can be used in parallel.
   - LCD power supply pins (V1, V2, V3)
     These pins are used to connect an external bypass capacitor or to use an external power supply circuit.
   - LCD RAM
     Sets display data. The relationship between the LCD RAM and the display segment depends on the duty cycle. Automatic displays are started by setting a register group needed for them, followed by writing data into the section for a duty cycle by the same instruction as for the normal RAM and turning on them. The word/byte access instructions can be used to set the RAM.
C. Table 3.3 lists SEG21 and SEG22 displays in the three-digit eight-segment LCD and sample display data.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Display</th>
<th>Address</th>
<th>Binary data</th>
<th>Hexadecimal data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0x746</td>
<td>1 1 0 1 1 1</td>
<td>0xD7</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0x746</td>
<td>0 0 0 0 1 1</td>
<td>0x26</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>0x746</td>
<td>1 1 1 0 1 1</td>
<td>0xE3</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>0x746</td>
<td>1 0 1 0 1 1</td>
<td>0xA7</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>0x746</td>
<td>0 0 1 1 0 1</td>
<td>0x36</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>0x746</td>
<td>1 0 1 1 0 1</td>
<td>0xB5</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>0x746</td>
<td>1 1 1 1 0 1</td>
<td>0xF5</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>0x746</td>
<td>0 0 0 0 1 1</td>
<td>0x07</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>0x746</td>
<td>1 1 1 1 0 1</td>
<td>0xF7</td>
</tr>
<tr>
<td>9</td>
<td>9</td>
<td>0x746</td>
<td>1 0 1 1 0 1</td>
<td>0xB7</td>
</tr>
<tr>
<td>A</td>
<td>A</td>
<td>0x746</td>
<td>0 1 1 1 0 1</td>
<td>0x77</td>
</tr>
<tr>
<td>B</td>
<td>B</td>
<td>0x746</td>
<td>1 1 1 1 0 1</td>
<td>0xF4</td>
</tr>
<tr>
<td>C</td>
<td>C</td>
<td>0x746</td>
<td>1 1 0 1 0 0</td>
<td>0xD1</td>
</tr>
<tr>
<td>D</td>
<td>D</td>
<td>0x746</td>
<td>1 1 1 0 0 1</td>
<td>0xE6</td>
</tr>
<tr>
<td>E</td>
<td>E</td>
<td>0x746</td>
<td>1 1 1 1 0 0</td>
<td>0xF1</td>
</tr>
<tr>
<td>F</td>
<td>F</td>
<td>0x746</td>
<td>0 1 1 1 0 0</td>
<td>0x71</td>
</tr>
</tbody>
</table>
Table 3.4  Functions Assigned on Transmit Side

<table>
<thead>
<tr>
<th>Function</th>
<th>Function Allocation</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSS</td>
<td>13-bit counter that receives the system clock as the input.</td>
</tr>
<tr>
<td>TMC</td>
<td>Sets the timer C automatic reloading register function and input clock.</td>
</tr>
<tr>
<td>TLC</td>
<td>Sets the duration for outputting/terminating the carrier wave.</td>
</tr>
<tr>
<td>TCRF</td>
<td>Sets the input clock for timer FH.</td>
</tr>
<tr>
<td>TCSRF</td>
<td>Sets TCFH clearing by compare match.</td>
</tr>
<tr>
<td>TCFH</td>
<td>Counter for timer FH</td>
</tr>
<tr>
<td>OCRFH</td>
<td>Generates timing for the carrier wave.</td>
</tr>
<tr>
<td>PCR4</td>
<td>Sets P42 as the output port.</td>
</tr>
<tr>
<td>PDR4 (P42)</td>
<td>Carrier wave output pin</td>
</tr>
<tr>
<td>PMR5</td>
<td>Selects a pin function for port 5.</td>
</tr>
<tr>
<td>PDR5</td>
<td>Key switch input pin</td>
</tr>
<tr>
<td>PUCR5</td>
<td>Turns off the pull-up MOS for port 5.</td>
</tr>
<tr>
<td>PCR5</td>
<td>Sets input/output for port 5.</td>
</tr>
<tr>
<td>TMG</td>
<td>Clears TCG, and sets the input clock and an interrupt edge.</td>
</tr>
<tr>
<td>TCG</td>
<td>Counter for timer G</td>
</tr>
<tr>
<td>ICRGR</td>
<td>Stores data received by the infrared light reception device.</td>
</tr>
<tr>
<td>LPCR</td>
<td>Selects a duty cycle for the LCD, and a segment pin.</td>
</tr>
<tr>
<td>LCR</td>
<td>Turns on and off the LCD, and sets a frame frequency.</td>
</tr>
<tr>
<td>LCR2</td>
<td>Selects waveform A or B for the LCD.</td>
</tr>
<tr>
<td>LCDRAM</td>
<td>Stores LCD display data.</td>
</tr>
<tr>
<td>TMIG</td>
<td>Receives the output value of the infrared light reception device as the input.</td>
</tr>
<tr>
<td>NCS</td>
<td>Turns on and off the noise elimination function for an input capture input signal.</td>
</tr>
<tr>
<td>IENTG</td>
<td>Enables an interrupt request by an input capture input signal.</td>
</tr>
<tr>
<td>IENTFH</td>
<td>Enables an interrupt request by timer FH compare match.</td>
</tr>
<tr>
<td>IENTC</td>
<td>Enables an interrupt request resulting from timer C overflow.</td>
</tr>
<tr>
<td>IRRTG</td>
<td>Interrupt flag by an input capture input signal</td>
</tr>
<tr>
<td>IRRTFH</td>
<td>Interrupt flag by timer FH compare match</td>
</tr>
<tr>
<td>IRRRTC</td>
<td>Interrupt flag resulting from timer C overflow</td>
</tr>
</tbody>
</table>
4. Principle of Operation

1. Figure 4.1 shows the flowchart for the infrared remote controller. Following that flowchart, infrared remote control processing is carried out.

---

**Figure 4.1** Flowchart for Infrared Remote Controller
2. Discrimination between 0 and 1
The length of a carrier wave is used to discriminate between 0 and 1.

<table>
<thead>
<tr>
<th>Transmit Bit</th>
<th>Carrier Wave Output Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>380 µs</td>
</tr>
<tr>
<td>1</td>
<td>770 µs</td>
</tr>
</tbody>
</table>

The carrier wave termination period during one-bit data transmission is 600 µs, being constant.

- Timer C setting
  - Timer C input clock: $\phi/64 = 78.1$ kHz
  - Timer C count time: $1 / 78.1$ kHz = 12.8 µs
- Transmit bit 0 (380 µs) setting
  - Timer C count needed for 380 µs
    - $380 \text{ µs} / 12.8 \text{ µs} = 29.6 = 30$
  - TLC setting
    - (For the up-counter) $256 – 30 = 226$
- Transmit bit 1 (770 µs) setting
  - Timer C count needed for 770 µs
    - $770 \text{ µs} / 12.8 \text{ µs} = 60.1 = 61$
  - TLC setting
    - (For the up-counter) $256 – 61 = 195$
- Setting the carrier wave termination period during one-bit data transmission (600 µs)
  - Timer C count needed for 600 µs
    - $600 \text{ µs} / 12.8 \text{ µs} = 46.8 = 47$
  - TLC setting
    - (For the up-counter) $256 – 47 = 209$

3. One-byte data determination
The transmit side transmits the same data 10 times. If it has been received continuously five times, the data is stored as the correct value.

4. One-byte transmit interval
The carrier wave termination period during one-byte data transmission is 2 ms.
If the carrier wave termination period exceeds 2 ms, the receive side identifies the start bit of the data.
- Setting the carrier wave termination period during one-byte data transmission (2 ms)
  - Timer C count needed for 2 ms
    - $2000 \text{ µs} / 12.8 \text{ µs} = 156.2 = 157$
  - TLC setting
    - (For the up-counter) $256 – 157 = 99$

5. Discrimination between retransmit and new data on receive side
If the carrier wave termination period exceeds 3.2 ms, the receive side identifies new data.
5. Description of Software

5.1 Modules

Table 5.1 lists the modules used for the sample task.

<table>
<thead>
<tr>
<th>Module</th>
<th>Label</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>main</td>
<td>Sets an interrupt, initializes the LCD, receives one byte of infrared data for data determination, and displays data on the LCD.</td>
</tr>
<tr>
<td>Initialization of remote controller transmission</td>
<td>sendir_init</td>
<td>Initializes transmit processing by the remote controller.</td>
</tr>
<tr>
<td>One-byte infrared transmission</td>
<td>sendir</td>
<td>Converts infrared data by bit.</td>
</tr>
<tr>
<td>Key scan</td>
<td>keyscan</td>
<td>Identifies a selection key, and transmits one-byte data 10 times by infrared.</td>
</tr>
<tr>
<td>Port 5L reading</td>
<td>keyread</td>
<td>Returns the contents of P50 to P53.</td>
</tr>
<tr>
<td>Timer C interrupt</td>
<td>tcint</td>
<td>Generates a timer C interrupt to set the flag.</td>
</tr>
<tr>
<td>Timer F interrupt</td>
<td>tfint</td>
<td>Generates a timer FH interrupt to toggle P42 for carrier wave generation.</td>
</tr>
<tr>
<td>Timer G interrupt</td>
<td>tgint</td>
<td>Starts and measures input capture, and sets the flag.</td>
</tr>
<tr>
<td>LCD initialization</td>
<td>lcd_init</td>
<td>Initializes the LCD RAM.</td>
</tr>
</tbody>
</table>

5.2 Arguments

Table 5.2 lists the arguments used for the sample task.

<table>
<thead>
<tr>
<th>Argument</th>
<th>Function</th>
<th>Used in</th>
<th>Data Length</th>
<th>Input/Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>sdt</td>
<td>One-byte transmit data</td>
<td>sendir</td>
<td>One byte</td>
<td>Input</td>
</tr>
</tbody>
</table>
5.3 Internal Registers

Table 5.3 lists the internal registers used for the sample task.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Function</th>
<th>Address</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMC TMC7</td>
<td>Timer mode register C (automatic reloading function selection)</td>
<td>0xFFB4</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>When TMC7 = 0, sets the timer C function as the interval function.</td>
<td>Bit 7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When TMC7 = 1, sets the timer C function as the automatic reloading function.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMC6 TMC5</td>
<td>Timer mode register C (counter increment/decrement control)</td>
<td>0xFFB4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When TMC6 = 0 and TMC5 = 0, TCC increments.</td>
<td>Bit 6</td>
<td>TMC6 = 0</td>
</tr>
<tr>
<td></td>
<td>When TMC6 = 0 and TMC5 = 1, TCC decrements.</td>
<td>Bit 5</td>
<td>TMC5 = 0</td>
</tr>
<tr>
<td></td>
<td>When TMC6 = 1 and TMC5 = x, TCC is controlled by hardware according to UD pin input.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Note: x = Don't care</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMC2 TMC1 TMC0</td>
<td>Timer mode register C (clock selection)</td>
<td>0xFFB4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When TMC2 = 0, TMC1 = 1, and TMC0 = 1, TCC counts at ( \phi/64 ).</td>
<td>Bit 2</td>
<td>TMC2 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 1</td>
<td>TMC1 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 0</td>
<td>TMC0 = 1</td>
</tr>
<tr>
<td>TCC</td>
<td>Timer counter C</td>
<td>0xFFB5</td>
<td>0x00</td>
</tr>
<tr>
<td></td>
<td>This is an eight-bit up-counter that receives the system clock divided by 16 as the input. TCC is loaded with TLC settings upon an overflow.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TLC</td>
<td>Timer load register C</td>
<td>0xFFB5</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>With a value set in TLC, TCC starts to count up from TLC settings. It is loaded with TLC settings upon an overflow.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TCRF CKSH2</td>
<td>Timer control register F (clock selection H)</td>
<td>0xFFB6</td>
<td></td>
</tr>
<tr>
<td>CKSH1</td>
<td>When CKSH2 = 1, CKSH1 = 1, and CKSH0 = 0, TCFH counts at ( \phi/4 ).</td>
<td>Bit 6</td>
<td>CKSH2 = 1</td>
</tr>
<tr>
<td>CKSH0</td>
<td></td>
<td>Bit 5</td>
<td>CKSH1 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 4</td>
<td>CKSH0 = 0</td>
</tr>
<tr>
<td>TCSRF TFOVFH</td>
<td>Timer control status register F (timer overflow flag H)</td>
<td>0xFFB7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When TFOVFH = 0, TCF has not overflowed.</td>
<td>Bit 7</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>When TFOVFH = 1, TCF has overflowed.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMFH</td>
<td>Timer control status register F (compare match flag H)</td>
<td>0xFFB7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When CMFH = 0, a compare match F has not occurred.</td>
<td>Bit 6</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>When CMFH = 1, a compare match F has occurred.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OVIEH</td>
<td>Timer control status register F (timer overflow interrupt enable H)</td>
<td>0xFFB7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When OVIEH = 0, disables an interrupt request resulting from TCF overflow.</td>
<td>Bit 5</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>When OVIEH = 1, enables an interrupt request resulting from TCF overflow.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CCLRH</td>
<td>Timer control status register F (counter clear H)</td>
<td>0xFFB7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When CCLRH = 0, disables TCFH clearing by compare match.</td>
<td>Bit 4</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>When CCLRH = 1, enables TCFH clearing by compare match.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Using an Infrared Remote Controller in Transmission

#### Register Function

<table>
<thead>
<tr>
<th>Register</th>
<th>Function</th>
<th>Address</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCFH</td>
<td>Eight-bit timer counter FH</td>
<td>0xFFFFB8</td>
<td>0x00</td>
</tr>
<tr>
<td></td>
<td>Eight-bit up-counter that receives $\phi$4 as the input</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OCRFH</td>
<td>Output compare register FH</td>
<td>0xFFFFBA</td>
<td>0x80</td>
</tr>
<tr>
<td></td>
<td>Compared with TCFH. If the OCRFH value matches the TCFH one, the CMF in TCSR is set to 1.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMR5</td>
<td>Port mode register 5</td>
<td>0xFFFFCC</td>
<td>0x00</td>
</tr>
<tr>
<td></td>
<td>(P5n/WKPn/SEGn+1 pin function selection)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pin function with pin SEGn+1 not used</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When PMR5 = 0x00, pin P5n/WKPn/SEGn+1 functions as the P5n input/output pin.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PDR4</td>
<td>Port data register 4 (P42)</td>
<td>0xFFFFD7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When P42 = 0, sets pin P42 at the low level.</td>
<td>Bit 2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When P42 = 1, sets pin P42 at the high level.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PDR5</td>
<td>Port data register 5 (P54 to P57)</td>
<td>0xFFFFD8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>The upper four bits of PDR5 provide PDR5H to set data to be stored into output ports P54 to P57. Out of the data in P54 to P57, the status of a key row set at the low level is reflected in P50 to P53.</td>
<td>Bits 4 to 7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When PDR5 = 0xE0, selects the key row (0, 4) in P54.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When PDR5 = 0xD0, selects the key row (1, 5) in P55.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When PDR5 = 0xB0, selects the key row (2, 6) in P56.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When PDR5 = 0x70, selects the key row (3, 7) in P57.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PDR5L</td>
<td>Port 7 register (P50 to P53)</td>
<td>0xFFFFD8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>The lower four bits of PDR5 provide PDR5L to reflect the values of input ports P50 to P53.</td>
<td>Bits 0 to 3</td>
<td></td>
</tr>
<tr>
<td>PUCR5</td>
<td>Port pull-up control register 5</td>
<td>0xFFE2</td>
<td>0x00</td>
</tr>
<tr>
<td></td>
<td>When PUCR5 = 0x00, turns off the pull-up MOS.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCR4</td>
<td>Port control register 4</td>
<td>0xFFE8</td>
<td>0xFC</td>
</tr>
<tr>
<td></td>
<td>When PCR4 = 0xFC, sets P42 as the output port.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCR5</td>
<td>Port control register 5</td>
<td>0xFFE8</td>
<td>0xF0</td>
</tr>
<tr>
<td></td>
<td>When PCR5 = 0xF0, sets P54 to P57 as the output ports, and P50 to P53 as the input ports.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMG</td>
<td>Timer mode register G (timer overflow flag H)</td>
<td>0xFFFFB0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>When TGOVFH = 0, the input capture input signal is at the high level, and TCG has not overflowed.</td>
<td>Bit 7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When TGOVFH = 1, the input capture input signal is at the high level, and TCG has overflowed.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGOVFL</td>
<td>Timer mode register G (timer overflow flag L)</td>
<td>0xFFFFB0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>When TGOVFL = 0, the input capture input signal is at the low level, and TCG has not overflowed.</td>
<td>Bit 6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When TGOVFL = 1, the input capture input signal is at the low level, and TCG has overflowed.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OVIE</td>
<td>Timer mode register G (timer overflow interrupt enable)</td>
<td>0xFFFFB0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>When OVIE = 0, disables an interrupt request resulting from TCG overflow.</td>
<td>Bit 5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When OVIE = 1, enables an interrupt request resulting from TCG overflow.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Register</td>
<td>Function</td>
<td>Address</td>
<td>Setting</td>
</tr>
<tr>
<td>----------</td>
<td>----------</td>
<td>---------</td>
<td>---------</td>
</tr>
<tr>
<td>TMG</td>
<td>IIEGS</td>
<td>0xFFBC</td>
<td>Bit 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 3</td>
<td>CCLR1 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 2</td>
<td>CCLR0 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 1</td>
<td>CKS1 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 0</td>
<td>CKS0 = 0</td>
</tr>
<tr>
<td></td>
<td>Timer mode register G (input capture interrupt edge selection)</td>
<td>Bit 4</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>When IIEGS = 0, generates an interrupt at the rising edge of an input capture input signal.</td>
<td>Bit 3</td>
<td>CCLR1 = 1</td>
</tr>
<tr>
<td></td>
<td>When IIEGS = 1, generates an interrupt at the falling edge of an input capture input signal.</td>
<td>Bit 2</td>
<td>CCLR0 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 1</td>
<td>CKS1 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 0</td>
<td>CKS0 = 0</td>
</tr>
<tr>
<td></td>
<td>Timer counter G</td>
<td>Bit 4</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>This is an eight-bit unreadable/unwritable register that increments by an input clock. Upon detection of the rising edge of an input capture input signal, the TCG value is transferred to the input capture register GR (ICRGR).</td>
<td>Bit 3</td>
<td>CCLR1 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 2</td>
<td>CCLR0 = 0</td>
</tr>
<tr>
<td>ICRGR</td>
<td>Input capture register GR</td>
<td>Bit 4</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>This is an eight-bit read-only register. Upon detection of the rising edge of an input capture input signal, the TCG value is transferred.</td>
<td>Bit 3</td>
<td>CCLR1 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 2</td>
<td>CCLR0 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 1</td>
<td>CKS1 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 0</td>
<td>CKS0 = 0</td>
</tr>
<tr>
<td>LPCR</td>
<td>DTS1</td>
<td>0xFFC0</td>
<td>Bit 7</td>
</tr>
<tr>
<td></td>
<td>DTS0</td>
<td>0xFFC0</td>
<td>Bit 6</td>
</tr>
<tr>
<td></td>
<td>LCD port control register (duty cycle selection 1 and 0)</td>
<td>Bit 5</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>A combination of DTS1 and DTS0 selects the static cycle or a duty cycle of 1/4 to 1/2. When DTS1 = 1 and DTS0 = 1, selects a duty cycle of 1/4.</td>
<td>Bit 3</td>
<td>SGS2 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 2</td>
<td>SGS1 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 1</td>
<td>SGS0 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 0</td>
<td>SGS0 = 1</td>
</tr>
<tr>
<td></td>
<td>LCD port control register</td>
<td>Bit 4</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>(segment driver selection 0 to 3)</td>
<td>Bit 3</td>
<td>SGS2 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 2</td>
<td>SGS1 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 1</td>
<td>SGS0 = 1</td>
</tr>
<tr>
<td>CMX</td>
<td>LCD port control register (segment driver to be used).</td>
<td>Bit 4</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 3</td>
<td>SGS2 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 2</td>
<td>SGS1 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 1</td>
<td>SGS0 = 1</td>
</tr>
<tr>
<td></td>
<td>Selects a segment driver to be used.</td>
<td>Bit 4</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 3</td>
<td>SGS2 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 2</td>
<td>SGS1 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 1</td>
<td>SGS0 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 0</td>
<td>SGS0 = 1</td>
</tr>
<tr>
<td></td>
<td>LCD port control register</td>
<td>Bit 4</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>(segment driver selection 0 to 3)</td>
<td>Bit 3</td>
<td>SGS2 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 2</td>
<td>SGS1 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 1</td>
<td>SGS0 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 0</td>
<td>SGS0 = 1</td>
</tr>
<tr>
<td></td>
<td>Selects a segment driver to be used.</td>
<td>Bit 4</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 3</td>
<td>SGS2 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 2</td>
<td>SGS1 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 1</td>
<td>SGS0 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 0</td>
<td>SGS0 = 1</td>
</tr>
<tr>
<td></td>
<td>LCD port control register</td>
<td>Bit 4</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>(segment driver selection 0 to 3)</td>
<td>Bit 3</td>
<td>SGS2 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 2</td>
<td>SGS1 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 1</td>
<td>SGS0 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 0</td>
<td>SGS0 = 1</td>
</tr>
<tr>
<td></td>
<td>Selects a segment driver to be used.</td>
<td>Bit 4</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 3</td>
<td>SGS2 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 2</td>
<td>SGS1 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 1</td>
<td>SGS0 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 0</td>
<td>SGS0 = 1</td>
</tr>
</tbody>
</table>
## Using an Infrared Remote Controller in Transmission

<table>
<thead>
<tr>
<th>Register</th>
<th>Function</th>
<th>Address</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCR</td>
<td>PSW</td>
<td>0xFFC1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bit 6</td>
</tr>
<tr>
<td></td>
<td>LCD control register (LCD power supply split-resistor connection control)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>If the LCD displays no data in power-down mode or if an external power supply is used, the split-resistor for the LCD power supply can be disconnected from Vcc. When ACT = 0 or in standby mode, the split-resistor for the LCD power supply is disconnected from Vcc regardless of this bit. When PSW = 0, disconnects the split-resistor for the LCD power supply from Vcc. When PSW = 1, connects the split-resistor for the LCD power supply to Vcc.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ACT</td>
<td>LCD control resistor (display function start)</td>
<td>0xFFC1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Selects whether to use the LCD controller/driver. Clearing this bit to 0 terminates the operation of the LCD controller/driver. Furthermore, the LCD drive power supply is turned off regardless of the PSW value. The contents of the register are, however, retained. When ACT = 0, the LCD controller/driver terminates. When ACT = 1, the LCD controller/driver operates.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DISP</td>
<td>LCD control register (display data control)</td>
<td>0xFFC1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Selects whether to display the contents of the LCD RAM or display blank data regardless of those contents. When DISP = 0, displays blank data. When DISP = 1, displays LCDRAM data.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCR</td>
<td>CKS3</td>
<td>0xFFC1</td>
<td>CKS3 = 1</td>
</tr>
<tr>
<td></td>
<td>CKS2</td>
<td></td>
<td>Bit 3</td>
</tr>
<tr>
<td></td>
<td>Selects a clock to be used and frame frequency.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CKS1</td>
<td></td>
<td>Bit 2</td>
</tr>
<tr>
<td></td>
<td>When CKS3 = 1, CKS2 = 1, CKS1 = 1, and CKS0 = 0, selects 1/128 as the clock to be used.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CKS0</td>
<td></td>
<td>Bit 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bit 0</td>
</tr>
<tr>
<td>LCR</td>
<td>LCDAB</td>
<td>0xFFC1</td>
<td>CKS2 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bit 3</td>
</tr>
<tr>
<td></td>
<td>LCD control register 2 (waveform A or B selection control)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Selects whether to use waveform A or B to drive the LCD. When LCDAB = 0, uses waveform A to drive the LCD. When LCDAB = 1, uses waveform B to drive the LCD.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCDRAM</td>
<td>LCDRAM</td>
<td>0xF740 to —</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0xF74F</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Sets display data for the LCD.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMR1</td>
<td>TMIG</td>
<td>0xFFC8</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bit 3</td>
</tr>
<tr>
<td></td>
<td>Port mode register 1 (P13/TMIG pin function selection)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When TMIG = 0, pin P13/TMIG functions as the P13 input/output pin.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When TMIG = 1, pin P13/TMIG functions as the TMIG input pin.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMR2</td>
<td>NCS</td>
<td>0xFFC9</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bit 1</td>
</tr>
<tr>
<td></td>
<td>Port mode register 2 (TMIG noise canceler selection)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When NCS = 0, cancels the noise elimination function for an input capture input signal.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When NCS = 1, activates the noise elimination function for an input capture input signal.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Using an Infrared Remote Controller in Transmission

<table>
<thead>
<tr>
<th>Register</th>
<th>Function</th>
<th>Address</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>IENR2</td>
<td>IENTG</td>
<td>0xFFF4</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Interrupt enable register 2 (timer G interrupt enable) Controls enabling/disabling of a timer G interrupt request. When IENTG = 0, disables a timer G interrupt request. When IENTG = 1, enables a timer G interrupt request.</td>
<td>Bit 4</td>
<td></td>
</tr>
<tr>
<td>IENTFH</td>
<td>Interrupt enable register 2 (timer FH interrupt enable) When IENTFH = 0, disables a timer FH interrupt request. When IENTFH = 1, enables a timer FH interrupt request.</td>
<td>0xFFF4</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Bit 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IENTC</td>
<td>Interrupt enable register 2 (timer C interrupt enable) When IENTC = 0, disables a timer C interrupt request. When IENTC = 1, enables a timer C interrupt request.</td>
<td>0xFFF4</td>
<td>1</td>
</tr>
<tr>
<td>IRR2</td>
<td>IRRTG</td>
<td>0xFFF7</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Interrupt request register 2 (timer G interrupt request flag) Reflects whether a timer G interrupt is requested. When IRRTG = 0, a timer G interrupt is not requested. When IRRTG = 1, a timer G interrupt is requested.</td>
<td>Bit 4</td>
<td></td>
</tr>
<tr>
<td>IRRTFH</td>
<td>Interrupt request register 2 (timer FH interrupt request flag) When IRRTFH = 0, a timer FH interrupt is not requested. When IRRTFH = 1, a timer FH interrupt is requested.</td>
<td>0xFFF7</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Bit 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IRR2</td>
<td>IRRTC</td>
<td>0xFFF7</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Interrupt request register 2 (timer C interrupt request flag) When IRRTC = 0, a timer C interrupt is not requested. When IRRTC = 1, a timer C interrupt is requested.</td>
<td>Bit 1</td>
<td></td>
</tr>
</tbody>
</table>

5.4 Description of RAM

Table 5.4 lists the RAM used for the sample task.

Table 5.4 Description of RAM

<table>
<thead>
<tr>
<th>Label</th>
<th>Function</th>
<th>Address</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>tcflg</td>
<td>Determines a timer C interrupt.</td>
<td>1 byte</td>
<td>main, tcint, sendir</td>
</tr>
<tr>
<td>prdhl</td>
<td>Stores timer G measurement result.</td>
<td>1 byte</td>
<td>main, tgint</td>
</tr>
<tr>
<td>sxf</td>
<td>Determines whether the data is new or the same.</td>
<td>1 byte</td>
<td>main, tgint</td>
</tr>
<tr>
<td>enter</td>
<td>Determines whether to update the LCD.</td>
<td>1 byte</td>
<td>main, tgint</td>
</tr>
<tr>
<td>startf</td>
<td>Flag to determine whether the second timer G interrupt has been received</td>
<td>1 byte</td>
<td>main, tgint</td>
</tr>
<tr>
<td>endif</td>
<td>Flag to determine whether cycle measurement has been ended</td>
<td>1 byte</td>
<td>main, tgint</td>
</tr>
</tbody>
</table>
6. Flowchart

1. Main routine

```
main

i = 1
Disables an interrupt.

SendIR_init()
Initializes infrared reception.

NCS = 0
Cancels the TMIG noise elimination function.

TMIG = 1
Sets pin P13/TMIG as the TMIG input pin.

tmp = TMG
TMG = 0x1C
Sets the timer mode register.

prdh = 0
Clears the TMIG low-period variable.

enter = 0
Clears the receive date linefeed flag.

lcd_init()
Initializes the LCD controller/driver.

lcdram = LCDRAM + 6
Sets the most significant lcd address to 0xF746.

i = 0

i ++
rcvbuf[i] = 16
Sets the initial value.

i < 8?
Are eight bytes of data set?

i >= 8

IRRTG = 0
Clears the timer G interrupt request flag.

iENTG = 0
Disables a timer G interrupt request.

1
```

Note: * In the sample task, the stack pointer is set in INIT.SRC (assembly language).
**Using an Infrared Remote Controller in Transmission**

- `end f = 0` Clears the timer G count end flag.
- `bdt = 0` Clears the receive byte data buffer.
- `I = 0` Enables an interrupt.
- `j = 0`
  - `j < 5?` Is the same value received five times?
  - `j ≥ 5` Disables an interrupt.
- `start f = 0` Clears the timer G count start flag.
- `sxf = 0` Clears the initial data determination flag.
- `tmp = TMG` `TMG = 0x1C` Clears the flag, and sets the TCG count at φ/64.
- `IENTG = 1` Enables a timer G interrupt.
- `I = 1` Enables an interrupt.
- `I = 0` Disables an interrupt.
- `tmp << 1` Left-shifts the buffer for one-byte data by one bit.
- `tmp++` Adds 1 to the buffer.
- `tx[i] > 45` Is receive data 1?
  - `tx[i] = prdhl` Stores measurement data.
Using an Infrared Remote Controller in Transmission

1. Is new data received?
   - enter ≥ 2
   - enter = 1
   - i = 7

2. Is the eight-byte shift completed?
   - i > 0
   - i <= 0
   - rcvbuf[0] = bdt
     Stored new received data at the first array digit.
   - i = 0

3. Is eight-digit processing ended?
   - i > 8
   - i <= 8
   - i++
   - lcdram[i] = lcddate(rcvbuf[i])
     Displays received 8-digit data at the LCD.
2. Remote control transmit initialization

```
<table>
<thead>
<tr>
<th>sendir_init</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMRS = 0x00</td>
</tr>
<tr>
<td>PCRS = 0xF0</td>
</tr>
<tr>
<td>Sets P54 to P57 as the P5 output pins, and P50 to P53 as the P5 input pins.</td>
</tr>
<tr>
<td>PDRS = 0xF0</td>
</tr>
<tr>
<td>Sets P54 to P57 to 1.</td>
</tr>
<tr>
<td>PUCRS = 0x00</td>
</tr>
<tr>
<td>Turns off the pull-up MOS for P50 to P57.</td>
</tr>
<tr>
<td>TMC = 0x9B</td>
</tr>
<tr>
<td>Sets the automatic reloading function and up-counter. Sets φ/64 as the internal clock.</td>
</tr>
<tr>
<td>TLC = 0x00</td>
</tr>
<tr>
<td>Sets the TCC reloaded value to 0.</td>
</tr>
<tr>
<td>PCR4 = 0xFC</td>
</tr>
<tr>
<td>Sets P42 as the output pin.</td>
</tr>
<tr>
<td>TCRF = 0x60</td>
</tr>
<tr>
<td>Counter clock for the timer counter FH (TCFH): Sets φ/4 as the internal clock.</td>
</tr>
<tr>
<td>TCSR = 0x10</td>
</tr>
<tr>
<td>Enables TCFH clearing by compare match.</td>
</tr>
<tr>
<td>OCRFH = 0x10</td>
</tr>
<tr>
<td>Sets a value for comparing with TCFH.</td>
</tr>
<tr>
<td>P42 = 0</td>
</tr>
<tr>
<td>tcfgh = 0</td>
</tr>
<tr>
<td>Clears the timer C interrupt determination flag.</td>
</tr>
</tbody>
</table>
```

```
<table>
<thead>
<tr>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRRRTC = 0</td>
</tr>
<tr>
<td>Clears the timer C interrupt request flag.</td>
</tr>
<tr>
<td>IRRTFH = 0</td>
</tr>
<tr>
<td>Clears the timer FH interrupt request flag.</td>
</tr>
<tr>
<td>IENTC = 0</td>
</tr>
<tr>
<td>Disables a timer C interrupt.</td>
</tr>
<tr>
<td>IENTFH = 0</td>
</tr>
<tr>
<td>Disables a timer FH interrupt.</td>
</tr>
<tr>
<td>End</td>
</tr>
</tbody>
</table>
```
3. Remote control transmit processing

```
sendir

IRRFH = 0
Clears the timer FH interrupt flag.

IENTC = 1
Enables a timer C interrupt.

tcflg = 0
Clears the timer C interrupt determination flag.

bdlt = sdt & 0x80
Sets the most significant bit of transmit data to bdlt.

i = 0

i < 8
Is one-byte data transmission ended?
i ≥ 8
End of one-byte data transmission

TLC = 195
Sets the carrier wave output time for bit 1.

TLC = 226
Sets the carrier wave output time for bit 0.

sdt = sdt<<1
Left-shifts one bit.

bdlt = sdt&0x80
Sets the next transmit bit to bdlt.

IENTFH = 1
Enables a timer FH interrupt.

tcflg = 0
Clears the timer C interrupt determination flag.

P42 = 0
Terminates the carrier wave.

TCSRF = 0x10
Enables TCFH clearing by compare match.

tcflg = 0
Clears the timer C interrupt determination flag.

TLC = 209
Sets the period of carrier wave termination.

TCSRF = 0x10
Enables TCFH clearing by compare match.

tcflg = 0
Clears the timer C interrupt determination flag.
```

End

End of one-byte data transmission
4. Key scan

- **keysca**
  - \( j = 0 \)
  - \( j < 4 \)
  - \( j \geq 4 \)
  - \( i++ \)

  - **PDR5 = keyselect[]**
    - Sets a key row to be read.
  - \( j < 4 \)
  - **keydt = keyread()**
    - Reads P50 to P53 into keydt.
  - \( keydt = keydt >> 1 \)
  - \( keydt = 0x07 - keydt \)
  - **sendir(tmp)**
    - Transmits one-byte data.
  - \( i < 10 \)
  - \( i < 10 \)
  - \( i < 10 \)
  - \( i < 10 \)
  - \( i++ \)

- **sendir(tmp)**
  - Transmits one-byte data.

5. Port 5L reading

- **keyread**
  - **PDR5L**
    - Reads the contents of P50 to P53.
  - End of PDR5L output
6. Timer C interrupt

- tcint
  - IENFH = 0
    - Disables a timer FH interrupt.
  - IRRTC = 0
    - Clears the timer C interrupt request flag.
  - tcfig = 1
    - Sets the timer C interrupt determination flag.
- End

7. Timer F interrupt

- tfint
  - IRRTFH = 0
    - Clears the timer FH interrupt request flag.
  - P42 = P42
    - Inverts P42 output.
- End
8. Timer G interrupt

- **IRRTG = 0**
  - Clears the timer G interrupt request flag.

  - **sxf = 1?**
    - Is the received data the same as the previously received data?
      - **sxf = 1** During reception
        - **startf = 1?**  
          - **startf = 1** Count end
        - **startf = 0** Count start
      - **sxf = 0** New data reception

  - **OVFH = 1? or OVFL = 1?**
    - **Yes**
      - Overflow
      - prdhl = 0xFF
      - **endf = 1**
      - **tmp = TMG**
      - **TMG = 0x1C**
    - **No**
      - **startf = 0**

  - **prdhl = ICRGR**

- **sxf = 1?**
  - Is the received data the same as the previously received data?
    - **Yes**
      - **startf = 1**
    - **No**
      - **OVHF = 1? or OVFL = 1?**
        - **Yes**
          - Overflow
          - prdhl = ICRGR
          - **startf = 0**
        - **No**
          - **startf = 1**

  - **tmp = TMG**
  - **TMG = 0x0C**

- **End**
Using an Infrared Remote Controller in Transmission

1

OVFH = 1? or
OVFL = 1?

Yes, overflow

prdh = 0xFF

No

prdh <= 150
During reception

prdhl = ICRGR

prdhl > 150
Is reception ended?

prdhl > 150
New data reception

prdhl <= 250
The same value as
the previous one is
received.

prdhl > 250
Is receive data a new
value?

prdhl > 250, new value

enter++

startf = 1

tmp = TMG
TMG = 0x0C
sxf = 1

2
Using an Infrared Remote Controller in Transmission

LPCR = 0xCB
Duty cycle of 1/4.
Sets SEG13 to SEG32 as the segment pins.

LCR = 0xFE
Starts LCD display. The LCD uses φ/128 as a clock.
Sets the frame frequency at 30.5 Hz with φ = 5 MHz.

LCR2 = 0xE0
Drives the LCD by waveform A.

lcdram = LCDRAM
Sets the start address of LCDRAM.

i = 0

i++
lcdram[i] = 0
Clears LCDRAM.

i <= 0x0F?
Are all LCDRAM cleared?
i > 0x0F

End
# Program Listing

INIT.SRC (Program list)

```assembly
.export _INIT
.import _main

.section P,CODE

_INIT:
    mov.w #h'ff80,r7
    ldc.b #h'10000000,ccr
    jmp @_main

.end
```

 /***************************************************************************
 /*  H8/300L Super Low Power Series                                       */
 /*  -H8/38024 Series-                                                   */
 /*  Application Note                                                    */
 /*  * 'Infrared radiation Send/Receive Function'                       */
 /*  */
 /*  Function                                                           */
 /*  :Timer C Auto-reload Timer                                          */
 /*  :Timer FH 8-bit Timer                                               */
 /*  :Timer G Input capture Timer                                       */
 /*  */
 /*  External Clock : 10MHz                                              */
 /*  Internal Clock : 5MHz                                               */
 /*  Sub Clock : 32.768kHz                                               */
 /*  */
 /***************************************************************************

#include <machine.h>

 /***************************************************************************
 /*  Symbol Definition                                                  */
 /***************************************************************************

 struct BIT {
    unsigned char b7:1;      /* bit7 */
    unsigned char b6:1;      /* bit6 */
    unsigned char b5:1;      /* bit5 */
    unsigned char b4:1;      /* bit4 */
    unsigned char b3:1;      /* bit3 */
    unsigned char b2:1;      /* bit2 */
    unsigned char b1:1;      /* bit1 */
    unsigned char b0:1;      /* bit0 */
};

 struct P4BIT {
    unsigned char H:4;       /* bit7-bit4 */
    unsigned char L:4;       /* bit3-bit0 */
};

#define TMC       *(volatile unsigned char *)0xFFB4        /* Timer Mode Register C */
#define TCC       *(volatile unsigned char *)0xFFB5        /* Timer Counter C */
#define TLC       *(volatile unsigned char *)0xFFB5        /* Timer Load Register C */
#define TCRF      *(volatile unsigned char *)0xFFB6        /* Timer Control Register F */
```
#define TCRF_BIT *(struct BIT *)0xFFF6  /* Timer Control Register F */
#define TLAL TCRF_BIT.b7                    /* Toggle Output Level F */
#define CKSH2 TCRF_BIT.b6                    /* Clock Select H2 */
#define CKSH1 TCRF_BIT.b5                    /* Clock Select H1 */
#define CKSH0 TCRF_BIT.b4                    /* Clock Select H0 */
#define TCSR *volatile unsigned char*)0xFFF6 /* Timer Control Status Register F */
#define TCSR_BIT *(struct BIT *)0xFFF6 /* Timer Control Status Register F */
#define TFOVFH TCSR_Bit.b7                   /* Timer Overflow Flag H */
#define CMFH TCSR_Bit.b6                    /* Compare Match Flag H */
#define OVIH TCSR_Bit.b5                    /* Timer Overflow Interrupt Enable H */
#define CCLR TCSR_Bit.b4                    /* Counter Clear H */
#define TCNH *(volatile unsigned char*)0xFFF6 /* Timer Counter NH */
#define PCR5 *(volatile unsigned char*)0xFFF8 /* Port mode register 5 */
#define PCR5_BIT *(struct P4BIT *)0xFFF8 /* Port mode register 5 */
#define PDR5 *(volatile unsigned char*)0xFFF8 /* Port data register 5 */
#define PDR5_BIT *(struct P4BIT *)0xFFF8 /* Port mode register 5 */
#define PDR5H PDR5_Bit.H /* P57-P54 */
#define PDR5L PDR5_Bit.L /* P53-P50 */
#define OCR5 *(volatile unsigned char*)0xFFF6 /* Port pull-up control register 5 */
#define PCR4 *(volatile unsigned char*)0xFFF7 /* Port pull-up control register 4 */
#define PCR5 *(volatile unsigned char*)0xFFF7 /* Port control register 5 */
#define LCDRAM *(volatile unsigned char*)0xFFF7 /* LCD RAM */
#define TMG1 *(volatile unsigned char*)0xFFF9 /* Timer Mode Register G */
#define TMG +struct BIT *)0xFFF9 /* Timer Mode Register G */
#define TGOVFH TMG_Bit.b7 /* Timer Overflow Flag H */
#define TGOVFL TMG_Bit.b6 /* Timer Overflow Flag L */
#define OVIH TMG_Bit.b5 /* Timer Overflow Interrupt Enable */
#define IEGS TMG_Bit.b4 /* Input Capture Interrupt Edge Select */
#define CCLR1 TMG_Bit.b3 /* Counter Clear 1 */
#define CCLR0 TMG_Bit.b2 /* Counter Clear 0 */
#define CKSI TMG_Bit.b1 /* Clock Select 1 */
#define CKSO TMG_Bit.b0 /* Clock Select 0 */
#define ICRGF *(volatile unsigned char*)0xFFF8 /* Input Capture Register GF */
#define ICRGR *(volatile unsigned char*)0xFFF8 /* Input Capture Register GR */
#define LPCR *(volatile unsigned char*)0xFFF9 /* LCD Port Control Register */
#define LCR *(volatile unsigned char*)0xFFF9 /* LCD Control Register */
#define LCR2 *(volatile unsigned char*)0xFFF9 /* LCD Control Register 2 */
#define PMR1 *(volatile unsigned char*)0xFFF9 /* Port Mode Register 1 */
#define PMR1_BIT *(struct BIT *)0xFFF9 /* Port Mode Register 1 */
#define TMIG PMR1_Bit.b3 /* P13/TMIG Input Select */
#define PMR2 *(volatile unsigned char*)0xFFF9 /* Port Mode Register 2 */
#define PMR2_BIT *(struct BIT *)0xFFF9 /* Port Mode Register 2 */
#define NCS PMR2_Bit.b1 /* TMIG noise canceler select */
#define IENR2 *(volatile unsigned char*)0xFFF9 /* Interrupt Enable Register 2 */
#define IENR2_BIT *(struct BIT *)0xFFF9 /* Interrupt Enable Register 2 */
#define IENR2_BIT.b4 /* Timer G Interrupt Enable */
#define IENR2_Bit.b3 /* Timer F Interrupt Enable */
#define IENR2_Bit.b1 /* Timer C Interrupt Enable */
#define IR2_BIT *(struct BIT *)0xFFF9 /* Interrupt Request Register 2 */
#define IRRTG IR2_Bit.b4 /* Timer G Interrupt Request Flag */
#define IRRTG IR2_Bit.b3 /* Timer F Interrupt Request Flag */
#define IRRTC IR2_Bit.b1 /* Timer C Interrupt Request Flag */

#pragma interrupt (tcint)
#pragma interrupt (tfint)
#pragma interrupt (tgint)
extern void INIT( void );                   /* SP Set                               */
void main( void );                           /*                                               */
void sendir_init( void );                    /*                                               */
void sendir( unsigned char sdt );            /*                                               */
void keyscan( void );                        /*                                               */
unsigned char keyread( void );               /*                                               */
void tcint( void );                          /*                                               */
void tfint( void );                          /*                                               */
void tgint( void );                          /*                                               */
void lcd_init( void );                       /*                                               */

volatile unsigned char tcflg;                /* Timer C Interrupt Flag                     */
unsigned char prdhl, sxf, enter;             /* Timer G Interrupt Flag                     */
unsigned char startf;                        /* Timer G Count Start Flag                   */
unsigned char endf;                          /* Timer G Count End Flag                     */

unsigned char keyselect[4] = {
  0xE0,
  0xD0,
  0xB0,
  0x70,
};

unsigned char lcedtabl[17] = {                /* LCD Key Select Table                      */
  0x07, /* 7 */
  0xF7, /* 8 */
  0xB7, /* 9 */
  0x06, /* 1 */
  0xE3, /* 2 */
  0xA7, /* 3 */
  0x36, /* 4 */
  0xB5, /* 5 */
  0xF5, /* 6 */
  0x77, /* A */
  0xF4, /* B */
  0xD1, /* C */
  0xE6, /* D */
  0xF1, /* E */
  0x71, /* F */
  0x00, /* * */
};

#pragma section V1                            /* Vector Section Set                      */
void (*const VEC_TBL1[ ])(void) = {
  INIT /* 0x0000 - 0x000F */
};

#pragma section V2                            /* Vector Section Set                      */
void (*const VEC_TBL2[ ])(void) = {
  tcint /* 0x001A Timer C Interrupt Vector */
};
```c
#pragma section V3 /* Vector Section Set */
void (*const VEC_TBL3[])(void) = {
tfint /* 0x001E Timer F Interrupt Vector */
};

#pragma section V4 /* Vector Section Set */
void (*const VEC_TBL4[])(void) = {
tgint /* 0x0020 Timer G Interrupt Vector */
};

#pragma section /* P */
/********************************************************************************************************************/
/*  Main Program                                                                                                   */
/********************************************************************************************************************/
void main( void )
{
    unsigned char i,j,tx[8],rcvbuf[8],tmp,bdt;
    unsigned char *lcdram;

    set_imask_ccr(1); /* Interrupt Disable */
    sendir_init();

    NCS = 0; /* No noise cancellation circuit */
    TMIG = 1; /* P13/TMIG input select */
    tmp = TMG; /* Dummy Read for Flag Clear */
    TMG = 0x1C; /* TMG Set */

    prdhl = 0; /* Capture Data Ram Clear */
    enter = 0; /* Enter flag Clear */

    lcd_init(); /* Initialize LCD */
    lcdram = LCDRAM + 0x0006; /* Set LCDRAM Address */
    for(i = 0; i < 8; i++){
        rcvbuf[i] = 16;
    }

    IRRTG = 0; /* Clear IRRTG */
    IENTG = 0; /* Timer G Interrupt Disable */

    while(1){
        endf = 0; /* Timer G Interrupt End Flag Clear */
        bdt = 0; /* Data Buffer Clear */

        set_imask_ccr(0); /* Interrupt Enable */
        for(j = 0; j < 5; j++){
            startf = 0; /* Timer G Interrupt Start Flag Clear */
            sxf = 0; /* Flag Clear */

            tmp = TMG; /* Dummy Read for Flag Clear */
            TMG = 0x1C; /* Timer Mode Register Set */
            IENTG = 1; /* Timer G Interrupt Enable */
            for(i = 0; i < 8; i++){
                while(endf != 1){
                    IENTG = 0;
                    keyscan(); /* Keyscan and output KeyNo to IR */
                    IENTG = 1;
                }
                endf = 0;
                tx[i] = prdhl; /* Save lbit Receive */
            }
        }
    }
}
```
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```c
IRNTG = 0; /* Timer G Interrupt Disable */

tmp = 0;
for(i = 0; i < 8; i++){ /* Change 1byte Data */
    tmp = tmp<<1;
    if(tx[i] > 45){
        tmp++;
    }
}

if(bdt != tmp){ /* Is Receive Data same past Data? */
    j = 0; /* Receive Data Error */
}

bdt = tmp;
set_imask_ccr(1); /* Interrupt Disable */

if(enter >= 2){ /* First Data? */
    enter = 1; /* Renew Data */
    for(i = 7; i > 0; i--){
        rcvbuf[i] = rcvbuf[i-1]; /* move a figure 1 place to the left */
    }
    rcvbuf[0] = bdt; /* Set Renew Data */
    for(i = 0; i < 8; i++){
        lcdram[i] = lcdtable[rcvbuf[i]]; /* Copy Renew Data -> LCDRAM */
    }
}
else{
    rcvbuf[0] = bdt; /* First Data */
    lcdram[0] = lcdtable[bdt]; /* A/D Data 3 figures on LCD */
}

/************************************************************/
/* Infared radiation Send Initialize */
/************************************************************/
void sendir_init( void )
{
PMR5 = 0x00; /* Pin function Select Port5 */
PCR5 = 0xF0; /* P57-54 Output,P53-50 Input Port */
PDR5 = 0xF0; /* P57-54 Port "1"set */
PUCR5 = 0x00; /* Port5 pull-up OFF */
TMC = 0x9B; /* Select Auto-reload Timer */
TLC = 0x00; /* Clear TCC */
PCR4 = 0x2C; /* Set P42 Output Pin */
TCRF = 0x60; /* Select Timer FH, phi/4 */
TCSRFB = 0x10; /* TCFH clearing by compare match */
OCRFB = 0x10; /* Set Interrupt time is 26us */
P42 = 0; /* P42 Output Low level */
tcflg = 0;
IRRTC = 0; /* Clear IRRTC */
}
```
Using an Infrared Remote Controller in Transmission

```c
void sendir(unsigned char sdt)
{
    unsigned char bdt, i;
    IRRTFH = 0; /* Clear IRRTFH */
    IENTC = 1; /* Timer C Interrupt Enable */
    tcflg = 0;
    bdt = sdt & 0x80; /* Set Send top bit to bdt */
    for(i = 0; i < 8; i++) {
        if(bdt == 0)
            TLC = 226; /* Set bit-0 output time */
        else
            TLC = 195; /* Set bit-1 output time */
        sdt = sdt << 1; /* Set Next bit to bdt */
        bdt = sdt & 0x80;
    }
    IENTFH = 1; /* Timer FH Interrupt Enable */
    while(tcflg == 0); /* 1-bit is Sending */
    P42 = 0; /* P42 is Low level */
    while(tcflg == 0);
    TCSRF = 0x10; /* Initialize Overflow Interrupt */
    
    tcflg = 0;
    TLC = 209; /* Set P42 Low level time */
    while(tcflg == 0);
    TCSRF = 0x10; /* Initialize Overflow Interrupt */
    tcflg = 0;
    TLC = 99; /* Wait Over 2ms */
    while(tcflg == 0);
    IENTC = 0; /* Timer C Interrupt Disable */
}

void keyscan(void)
{
    unsigned char tmp, i, j, keydt;
    for(j = 0; j < 4; j++) {
        PDR5 = keyselect[j]; /* Set Key Select */
        keydt = keyread();
        if(keydt != 0x0F) { /* Touch Key? */
            keydt = keydt >> 1;
            keydt = 0x07 - keydt;
            for(i = 0; keydt != 0; i++) { /* What Key? */
                keydt = keydt >> 1;
            }
        }
    }
}
```
i = i<<2;
tmp = i+j; /* Set KeyNo -> tmp */
for(i = 0; i < 10; i++) {
    sendir(tmp); /* Same Data Output 10 time */
    sendir(tmp); /* Send 1byte data to IR */
}
}

/*******************************************************************************/
/* KeyRead */
/*******************************************************************************/
unsigned char keyread( void )
{
    return(PDR5L);
}

/*******************************************************************************/
/* Timer C Interrupt */
/*******************************************************************************/
void tcint( void )
{
    IENTFH = 0; /* Timer FH Interrupt Disable */
    IRRTC = 0; /* Clear IRRTC */
    tcflg = 1; /* Timer C Interrupt flag Set */
}

/*******************************************************************************/
/* Timer F Interrupt */
/*******************************************************************************/
void tfint( void )
{
    IRRTFH = 0; /* Clear IRRFH */
    P42 = ~P42; /* Toggle Output P42 */
}

/*******************************************************************************/
/* Timer G Interrupt */
/*******************************************************************************/
void tgint( void )
{
    unsigned char tmp;
    IRRTG = 0; /* Clear IRRTG */
    if(sxf == 1){
        if(startf == 1){
            if((TGOVFH == 1)&&(TGOVFL == 1)){
                prdhl = 0xFF;
            } else{
                startf = 0; /* Clear startf */
                prdhl = ICRGR; /* Capture Data Ramcopy */
            }
        }
        endif = 1; /* Set endif */
        tmp = TMG; /* Dummy Read for Flag Clear */
    }
}
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Using an Infrared Remote Controller in Transmission

```c
TMG = 0x1C; // Overflow Interrupt Disable */

} else{
    startf = 1; // Set startf */
    tmp = TMG; // Dummy Read for Flag Clear */
    TMG = 0x0C; // Timer Mode Register Set */
}
} else{
    if((TGOVFH == 1)|(TGOVFL == 1)){
        prdhl = 0xFF; // Not Receive Data */
    } else{
        prdhl = ICRGF; // Capture Data Ramcopy */
    }
}
if(prdhl > 150){
    if(prdhl > 250){
        enter++; // First Data or Renew Data */
    } 
    startf = 1; // Set startf */
    tmp = TMG; // Dummy Read for Flag Clear */
    TMG = 0x0C; // Timer Mode Register Set */
    sxf = 1;
}
}

*******************************************************************************/

/* LCD Initialize */
*******************************************************************************/

void lcd_init( void )
{
    unsigned char i;
    unsigned char *lcdram;

    LPCR = 0xCB; // 1/4 Duty, Select SEG32-SEG13 */
    LCR = 0xFE; // LCD ON */
    LCR2 = 0xE0; // A waveform */
    lcdram = LCDRAM; // Set LCDRAM Address */
    for(i = 0; i <= 0x0F; i++){
        lcdram[i] = 0;
    }
}

Link address specifications

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<tr>
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<tr>
<td>CV3</td>
<td>0x001E</td>
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<tr>
<td>CV4</td>
<td>0x0020</td>
</tr>
<tr>
<td>P, D</td>
<td>0x0100</td>
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<td>B</td>
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## Revision Record

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<td>Dec.19.03</td>
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