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# H8/300H Tiny Series

## Using External Interrupt to Start Incrementing Counter

### Introduction

An IRQ0 interrupt is generated when the switch connected to the $\overline{\text{IRQ0}}$ pin is turned on, and incrementing of the 16-bit counter set in the 16-bit general register, counter_sub, starts.

### Target Device

H8/3664

### Contents

## 1. Specifications

- An IRQ0 interrupt is generated when the switch connected to the $\overline{\text{IRQ0}}$ pin is turned on, and incrementing of the 16-bit counter set in the 16-bit general register, counter_sub, starts.
- An IRQ0 interrupt is requested when the falling edge of the $\overline{\text{IRQ0}}$ pin input is detected.
- The LED is turned on or off whenever the 16-bit counter set in R1 overflows.
- The LED is connected to the P74 output pin of port 7.

Figure 1 shows an example of connecting a switch to the $\overline{\text{IRQ0}}$ input pin.

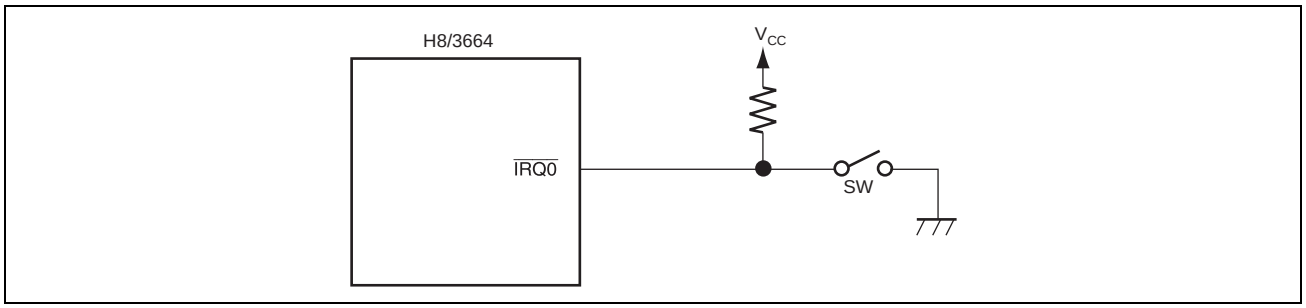



**Figure 1 Example of Connecting Switch to $\overline{\text{IRQ0}}$ Input Pin**

## 2. Description of Functions Used

In this sample task, the counter starts incrementing when an IRQ0 external interrupt occurs.

The external interrupts are described below.

- There are six external interrupts, NMI, IRQ3 to IRQ0, and WKP.
- An NMI interrupt is requested by input signal to pin $\overline{\text{NMI}}$. This interrupt is detected by sensing either the rising edge or falling edge, according to the setting of the NMIEG bit in interrupt edge select register 1 (IEGR1).
- NMI is the highest-priority interrupt, and can always be accepted regardless of the I bit setting in the condition code register (CCR).
- IRQ3 to IRQ0 interrupts are requested by input signals to pins $\overline{\text{IRQ3}}$ to $\overline{\text{IRQ0}}$. These four interrupts are detected individually by sensing either the rising edge or falling edge, according to the settings of the IEG3 to IEG0 bits in IEGR1.
- Pins $\overline{\text{IRQ3}}$ to $\overline{\text{IRQ0}}$ are also used as I/O port pins. To use these pins as $\overline{\text{IRQ3}}$ to $\overline{\text{IRQ0}}$ input pins, set the IRQ3 to IRQ0 bits in port mode register 1 (PMR1) to 1.
- When pins $\overline{\text{IRQ3}}$ to $\overline{\text{IRQ0}}$ are designated for interrupt input by PMR1 and the designated signal edge is input, the corresponding bit among the IRRI3 to IRRI0 bits in interrupt flag register 1 (IRR1) is set to 1, requesting the CPU of an interrupt.
- IRQ3 to IRQ0 interrupts can be disabled by clearing the IEN3 to IEN0 bits in interrupt enable register 1 (IENR1) to 0.
- WKP5 to WKP0 interrupts are requested by input signals to pins $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$. These interrupts are detected individually by either rising edge sensing or falling edge sensing, depending on the settings of the WPEG5 to WPEG0 bits in interrupt edge select register 2 (IEGR2).
- Pins $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$ are also used as I/O pins for port 5. To use these pins as $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$ input pins, set the WKP5 to WKP0 bits in port mode register 5 (PMR5) to 1.

- When pins $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$ are designated for interrupt input by PMR5 and the designated signal edge is input, the corresponding bit among the IWPF5 to IWPF0 bits in the wakeup interrupt flag register (IWPR) is set to 1, requesting the CPU of an interrupt.
- WKP interrupts can be disabled by clearing the IENWP bit in IENR1 to 0.
- All interrupts can be masked by setting the I bit in CCR to 1.
- Interrupt operation is described as follows.
  1. If an interrupt occurs while the corresponding bit in the interrupt enable register is set to 1, an interrupt request signal is sent to the interrupt controller.
  2. On receiving the interrupt request signal, the corresponding interrupt request status flag is set to 1, requesting the CPU of an interrupt.
  3. When multiple interrupt requests are generated, the interrupt controller requests to the CPU for the interrupt handling with the highest priority at that time. Other interrupt requests are held pending.
  4. The CPU checks the I bit setting in CCR. If the I bit is cleared to 0, the interrupt request is accepted. If the I bit is set to 1, the interrupt request is held pending.
  5. If the CPU accepts the interrupt, after processing of the current instruction is completed, interrupt handling will begin. First, both the PC and CCR are pushed onto the stack. The PC value pushed onto the stack is the address of the first instruction to be executed upon return from interrupt handling.
  6. The I bit in CCR is set to 1 to mask further interrupts.
  7. The CPU generates the vector address corresponding to the accepted interrupt, and transfers the address to PC as a start address of the interrupt handling-routine. Then a program starts executing from the address indicated in PC.
- When disabling interrupts by clearing bits in IENR1 or IRR1, always do so while interrupts are masked (I bit is set to 1). If the above clear operations are performed while the I bit is cleared to 0, and as a result a conflict arises between the clear instruction and an interrupt request, exception handling for the interrupt will be executed after the clear instruction has been executed.

Table 1 lists the function allocation for this sample task. The functions listed in table 1 are allocated to start incrementing the counter when an external interrupt occurs.

**Table 1 Function Allocation**

| Function | Description |
|---|---|
| IRRI0 | Indicates whether or not an IRQ0 interrupt is requested |
| IEN0 | Enables $\overline{\text{IRQ0}}$ pin interrupt requests |
| IEG0 | Selects input edge of the $\overline{\text{IRQ0}}$ pin |
| $\overline{\text{IRQ0}}$ | Switch input pin |
| PCR7 | Sets P74 output pin function |
| PDR7 | Stores P74 output pin data |
| P74 | LED output pin |

## 3. Description of Operations

Figure 2 shows this sample task's principle of operation. The hardware and software processing shown in figure 2 applies external interrupts to start incrementing the counter.

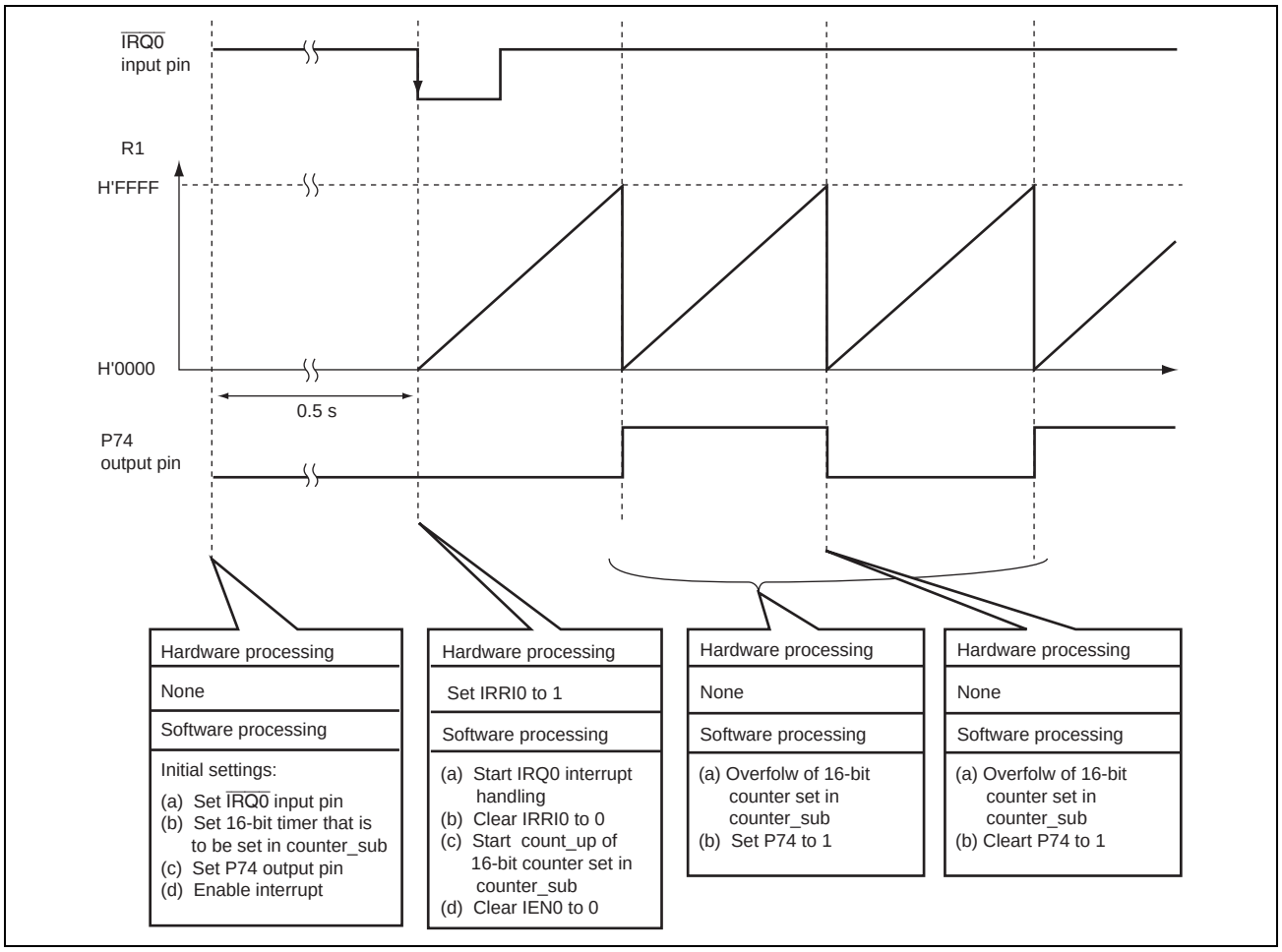



**Figure 2 Operation Principle: Using External Interrupts to Start Incrementing Counter**

# 4. Description of Software

## 4.1 Description of Modules

Table 2 describes the software used in this sample task.

**Table 2 Description of Modules**

| Module Name | Label Name | Function |
|---|---|---|
| Main routine | main | Sets the IRQ0 interrupt and LED output pin, enables interrupts, increments the 16-bit counter, and performs LED output. |
| Switch on | IRQ0 | During the IRQ0 interrupt handling routine, sets SWONF to 1. |

## 4.2 Description of Arguments

No arguments are used in this sample task.

## 4.3 Description of Internal Registers

Table 3 describes the internal registers used in this sample task.

**Table 3 Description of Internal Registers**

| Register Name | | Function | Address | Setting |
|---|---|---|---|---|
| PDR7 | P74 | Port data register 7 (port data register 74):<br>When P74 is cleared to 0, the P74 pin output level is low.<br>When P74 is set to 1, the P74 pin output level is high. | H'FFDA<br>Bit 4 | <br>0 |
| PCR7 | PCR74 | Port control register 7 (port control register 74):<br>When PCR74 is set to 1, the P74 pin functions as an output pin. | H'FFEA<br>Bit 4 | <br>1 |
| IEGR1 | IEG0 | Interrupt edge select register 1 (IRQ0 edge select):<br>When IEG0 is cleared to 0, the falling edge of the $\overline{\text{IRQ0}}$ pin input is detected.<br>When IEG0 is set to 1, the rising edge of the $\overline{\text{IRQ0}}$ pin input is detected. | H'FFF2<br>Bit 0 | <br>0 |
| IENR1 | IEN0 | Interrupt enable register 1 (IRQ0 interrupt enable):<br>When IEN0 is set to 1, interrupt requests from the $\overline{\text{IRQ0}}$ pin are enabled. | H'FFF4<br>Bit 0 | <br>1 |
| IRR1 | IRRI0 | Interrupt flag register 1 (IRQ0 interrupt request flag):<br>When IRRI0 is cleared to 0, no IRQ0 interrupt is requested.<br>When IRRI0 is set to 1, an IRQ0 interrupt is requested. | H'FFF6<br>Bit 0 | <br>0 |

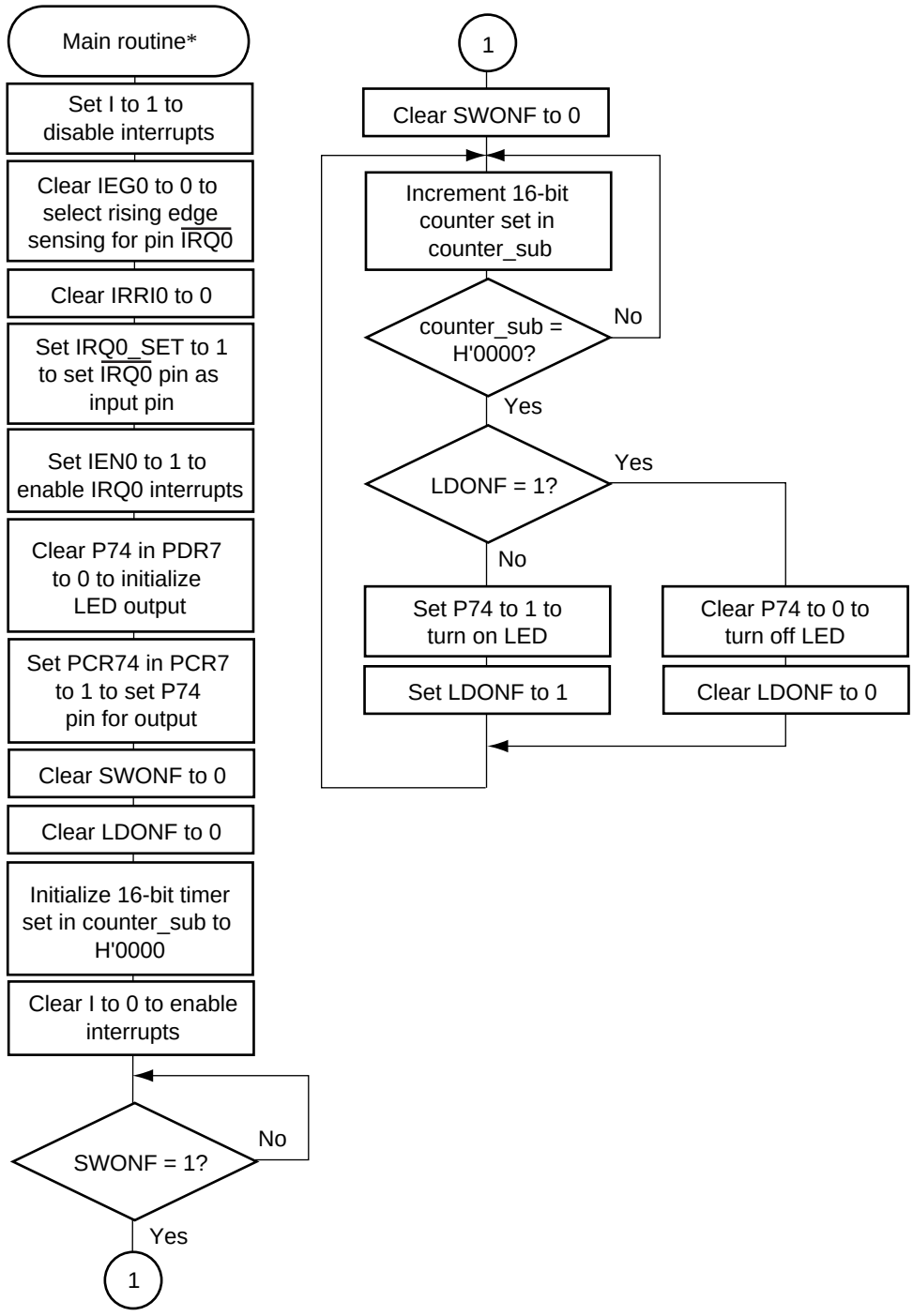
## 4.4 Description of RAM

Table 4 describes the RAM used in this sample task.

**Table 4 Description of RAM**

| Label Name | | Function | Address | Used in |
|---|---|---|---|---|
| counter_sub | | 16-bit up-counter that turns on or off the LED when it overflows | H'FB80 | Main routine |
| USRF | SWONF | Flag for judging on/off of the switch | H'FB82<br>Bit 0 | Main routine<br>Switch on |
| | LDONF | Flag for judging on/off of the LED | H'FB82<br>Bit 1 | Main routine |

## 5. Flowcharts




Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly).

**Figure 3 Flowchart for Main Routine**

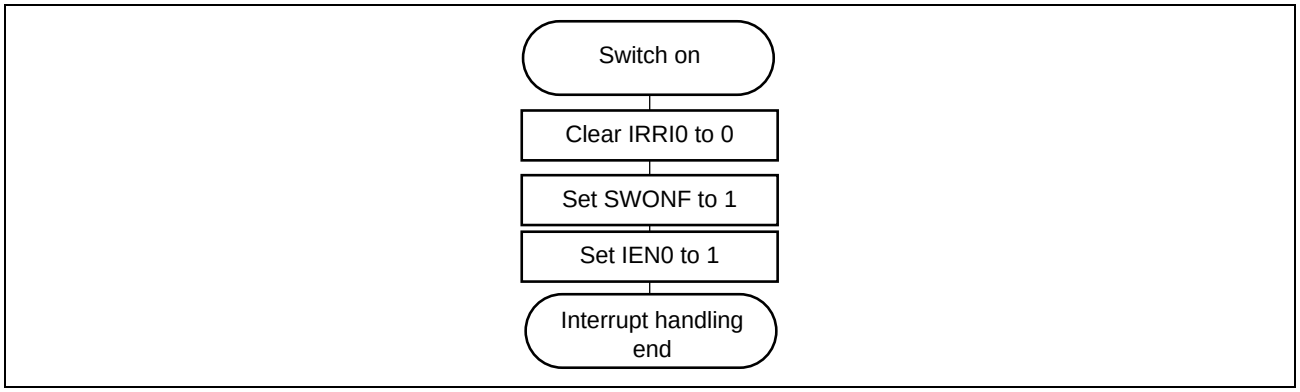



**Figure 4 Flowchart for IRQ0 Interrupt Handling Routine**

## 6. Program Listing

INIT.SRC (Program listing)

```
      .EXPORT  _INIT
      .IMPORT  _main
 ;
      .SECTION    P,CODE
 _INIT:
      MOV.W    #H'FF80,R7
      LDC.B    #B'10000000,CCR
      JMP      @_main
 ;
      .END
```

```
/************************************************************/
/*                                                          */
/*    H8/300H Tiny Series -H8/3664-                         */
/*    Application Note                                      */
/*                                                          */
/*    'Count Start by External Interrupt'                   */
/*                                                          */
/*    Function                                              */
/*    : External Interrupt                                  */
/*                                                          */
/*    External Clock : 16MHz                                */
/*    Internal Clock : 16MHz                                */
/*    Sub Clock      : 32.768kHz                            */
/*                                                          */
/************************************************************/

#include    <machine.h>
```

```
/************************************************************/
/*    Symbol Definition                                     */
/************************************************************/
struct BIT {
    unsigned char    b7:1;      /* bit7 */
    unsigned char    b6:1;      /* bit6 */
    unsigned char    b5:1;      /* bit5 */
    unsigned char    b4:1;      /* bit4 */
    unsigned char    b3:1;      /* bit3 */
    unsigned char    b2:1;      /* bit2 */
    unsigned char    b1:1;      /* bit1 */
    unsigned char    b0:1;      /* bit0 */
};

#define        PDR7_BIT    (*(struct BIT *)0xFFDA)     /* Port Data Register 7             */
#define        P74         PDR7_BIT.b4                 /* Port Data Register 7 bit4        */
#define        PCR7_BIT    (*(struct BIT *)0xFFEA)     /* Port Control Register 7          */
#define        PCR74       PCR7_BIT.b4                 /* Port Control Register bit4       */
#define        IEGR1_BIT   (*(struct BIT *)0xFFF2)     /* Interrupt Edge Select Register 1 */
#define        IEG0        IEGR1_BIT.b0                /* IRQ0 Edge Select                 */
#define        IENR1_BIT   (*(struct BIT *)0xFFF4)     /* Interrupt Enable Register 1      */
#define        IEN0        IENR1_BIT.b0                /* IRQ0 Interrupt Enable            */
#define        IRR1_BIT    (*(struct BIT *)0xFFF6)     /* Interrupt Request Register 1     */
#define        IRRI0       IRR1_BIT.b0                 /* IRQ0 Interrupt Request Flag      */
#define        PMR1_BIT    (*(struct BIT *)0xFFE0)     /* Port Mode Register 1             */
#define        IRQ0_SET    PMR1_BIT.b4                 /* Port Mode Register 1 bit4        */

#pragma        interrupt    (IRQ0)
/************************************************************/
/*     Function Definition                                  */
/************************************************************/
extern    void    INIT ( void );                     /* SP Set                           */
void      main   ( void );
void      IRQ0   ( void );
void      wait   ( void );
```

```
/************************************************************/
/*    RAM define                                            */
/************************************************************/

unsigned int     counter_sub;
    unsigned char    USRF;              /* User Flag Erea                          */

#define        USRF_BIT    (*(struct BIT *)&USRF)
#define        SWONF        USRF_BIT.b0 /* Switch On Flag                          */
#define        LDONF        USRF_BIT.b1 /* LED On Flag                             */

/************************************************************/
/*    Vector Address                                        */
/************************************************************/
#pragma    section        V1            /* VECTOR SECTOIN SET                      */
void (*const VEC_TBL1[])(void) = {
    INIT                                /* 00 Reset                                */
};
#pragma    section        V2            /* VECTOR SECTOIN SET                      */
void (*const VEC_TBL2[])(void) = {
    IRQ0                                /* IRQ0  Interrupt                         */
};
#pragma    section                       /* P                                       */
/************************************************************/
/*    Main Program                                          */
/************************************************************/
void    main ( void )
{

    set_imask_ccr(1);                   /* Interrupt Disable                       */

    IEG0 = 1;                           /* Initialize IRQ0 Terminal Input Edge     */

    IRRI0 = 0;                          /* Initialize IRRI0                        */

    IRQ0_SET = 1;                       /* Initialize Input TerminalIRQ0           */

    IEN0 = 1;                           /* IRQ0 Interrupt Request Enable           */

    P74 = 0;                            /* Initialzie LED Output                   */
```

```
    PCR74 = 1;                          /* Initialize P74 Input-Output Terminal Function */

    SWONF = 0;                          /* Initialize SWONF                              */
    LDONF = 0;                          /* Initialize LDONF                              */

    counter_sub = 0x0000;               /* Initialize 16bit Counter                      */

    set_imask_ccr(0);                   /* Interrupt Enable                              */

    while(SWONF != 1){                  /* SWONF = 0 ?                                   */
        ;
    }

    SWONF = 0;                          /* Clear SWONF                                   */

    while(1){
        do{
            counter_sub++;              /* Increment 16bit Counter                       */
        }while(counter_sub != 0x0000);  /* 16bit Counter = H'0000 ?                      */

        if(LDONF == 1){                 /* LDONF = 1 ?                                   */
            P74 = 0;                    /* Turn Off LED                                  */
            LDONF = 0;                  /* Clear LDONF                                   */
        }
            else{
                P74 = 1;                /* Turn On LED                                   */
                LDONF = 1;              /* Set LDONF                                     */
            }
    }

}
```

```
/************************************************************/
/*    IRQ0 Interrupt                                        */
/************************************************************/
void    IRQ0 ( void )
{

    IRRI0 = 0;                          /* Clear    IRRI0                          */

    SWONF = 1;                          /* Set SWONF                               */

    IEN0 = 0;                           /* IRQ0 Interrupt Disable                  */

}
```

**Link Address Setting:**

| Section Name | Address |
|---|---|
| CV1 | H'0000 |
| CV2 | H'001C |
| P | H'0100 |
| B | H'FB80 |

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| 2.00 | Sep.01.06 | All pages | Format has been changed from Hitachi version to Renesas version. |
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