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M32C/80 Series

Using DMACII (Multiple Transfer)

1. Abstract

This application note describes how to use DMACII in multiple transfer mode.

2. Introduction

The explanation of this issue is applied to the following condition:

Applicable MCU: M32C/80 Series

This program can also be used when operating other microcomputers within the M16C family, provided they have DMACII function. However, some functions may have been modified.

Refer to the User's Manual for details. Use functions covered in this Application Note only after careful evaluation.

3. Detailed description

The following explains an example use of DMACII transfer for the case where when an interrupt request which has had its priority level set to 7 by the interrupt control register occurs, data is transferred from multiple memory locations to multiple memory locations by a DMACII transfer.

In multiple transfer mode, a DMACII transfer is performed a multiple number of times (as set by CNT2–CNT0 bits) for one transfer request generated.

Figure 1 shows a typical operation of a multiple transfer mode.

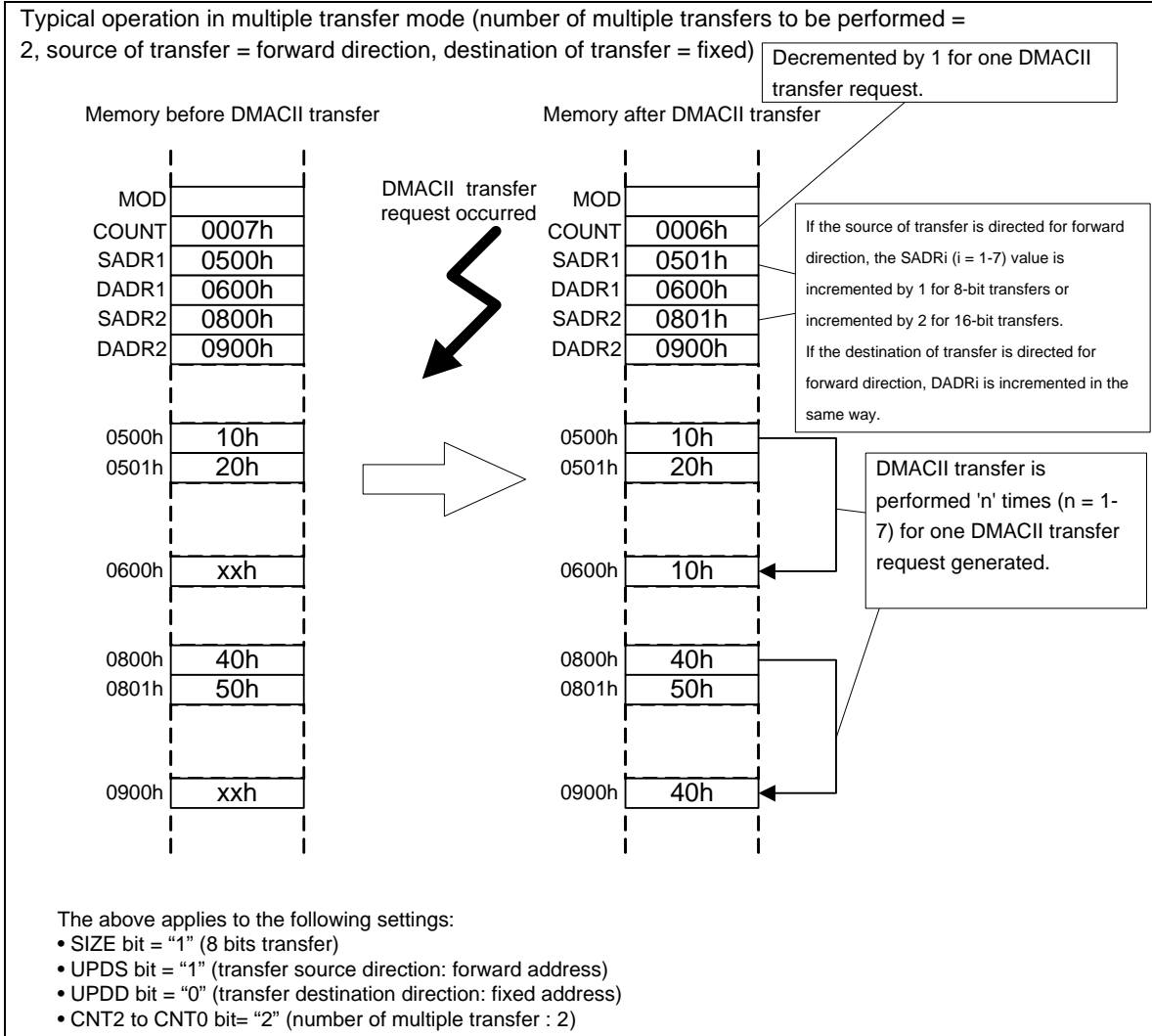


Figure 1. Typical Operation of a DMACII Multiple Transfer Mode

3.1 DMAC II Transfer Mode

This application note example offers functions of multiple transfer mode shown in Table 1.

Table 1. Selectable Functions in Multiple Transfer Mode

Item	Definition	Selection
Transfer Block	8 bits	Yes
	16 bits	
Source Direction	Fixed address	
	Forward address	Yes
Destination Direction	Fixed address	Yes
	Forward address	

3.2 DMAC II Index

During multiple transfer mode, the DMACII index is comprised of $4 + 4 \times n$ bytes (n = number of multiple transfers performed). The source of transfer and the destination of transfer addresses for a number of multiple transfers to be performed are located alternately at the addresses following MOD and COUNT. The DMAC II index must be located on the RAM area.

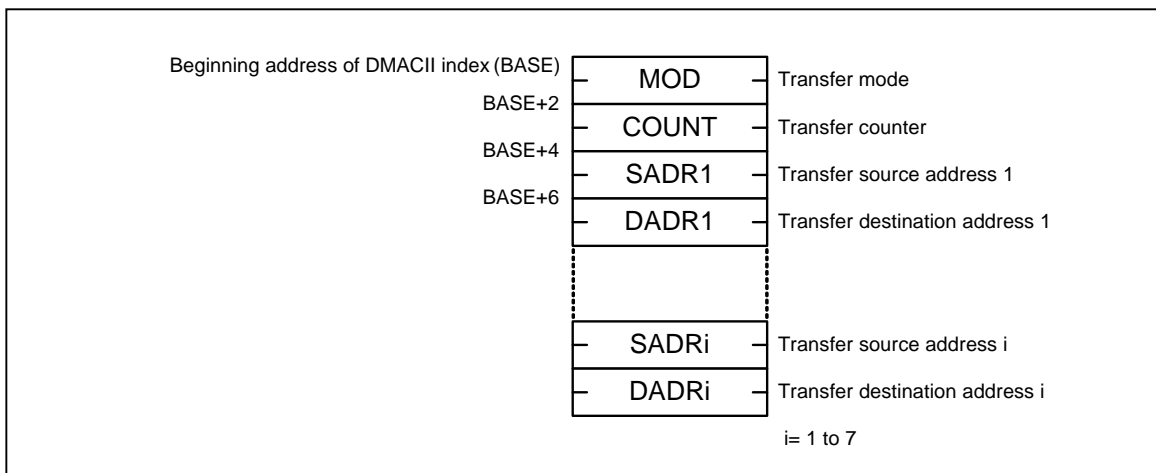


Figure 2. DMAC II Index

3.3 DMAC II Transfer

The interrupt requests from all peripheral functions whose ILVL2–ILVL0 bits in the interrupt control register have been set to “111b” constitute the cause of requests to DMAC II. In this application note, the INT0 interrupt is used for the cause of DMAC II request.

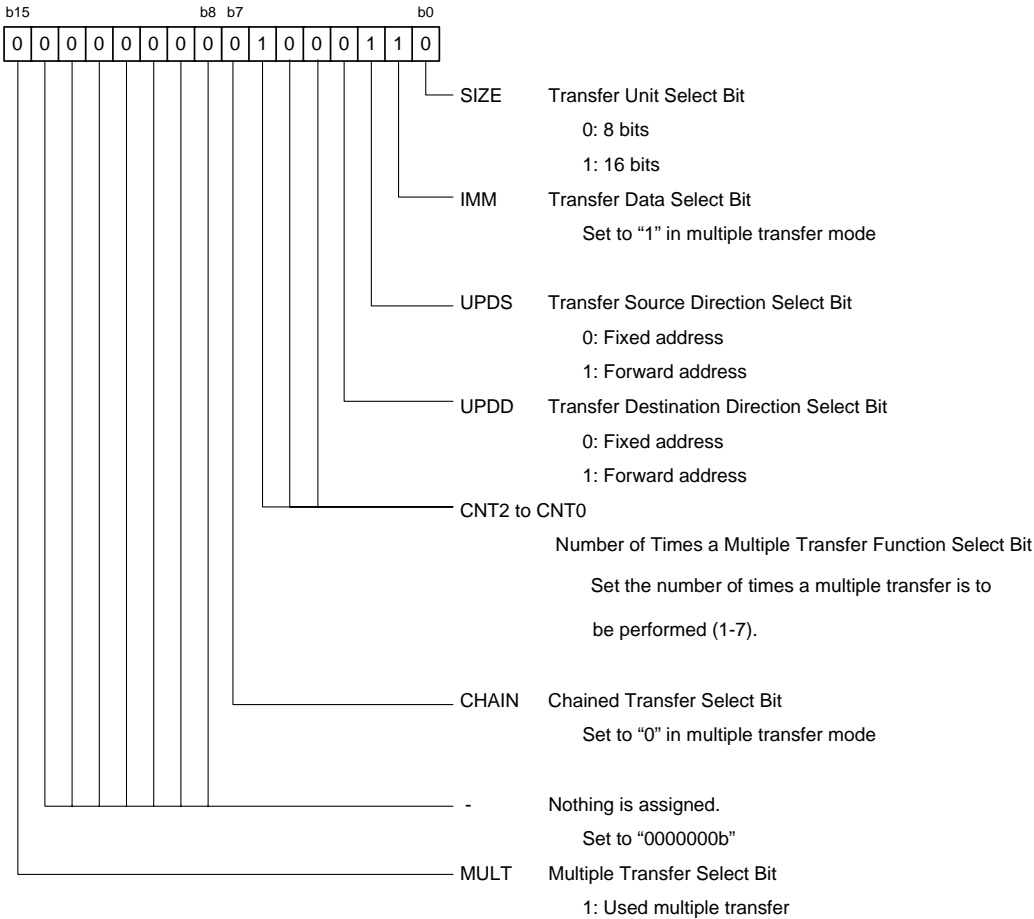
3.4 Setting Up the Relocatable Vector Table

Set the starting address of the DMAC II index in the interrupt vector for the peripheral function interrupt activating DMAC II.

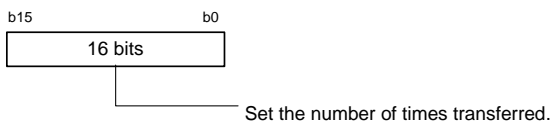
3.5 Register Setting

To enable the operation defined in "Section 3. Detailed description", the following register settings must be taken place step by step. For detail configuration of each register, please refer to M32C/80 Series HARDWARE MANUAL.

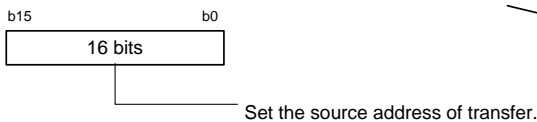
(1) Transfer mode (MOD)



(2) Transfer count (COUNT)

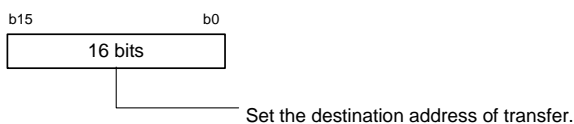


(3) Transfer source address (SADR)

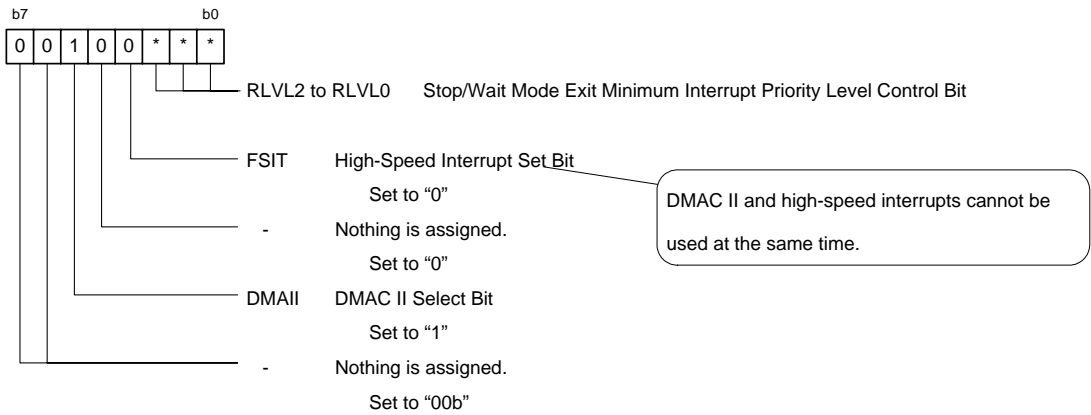


For (3) and (4), set the addresses alternately for a number of multiple transfers to be performed.

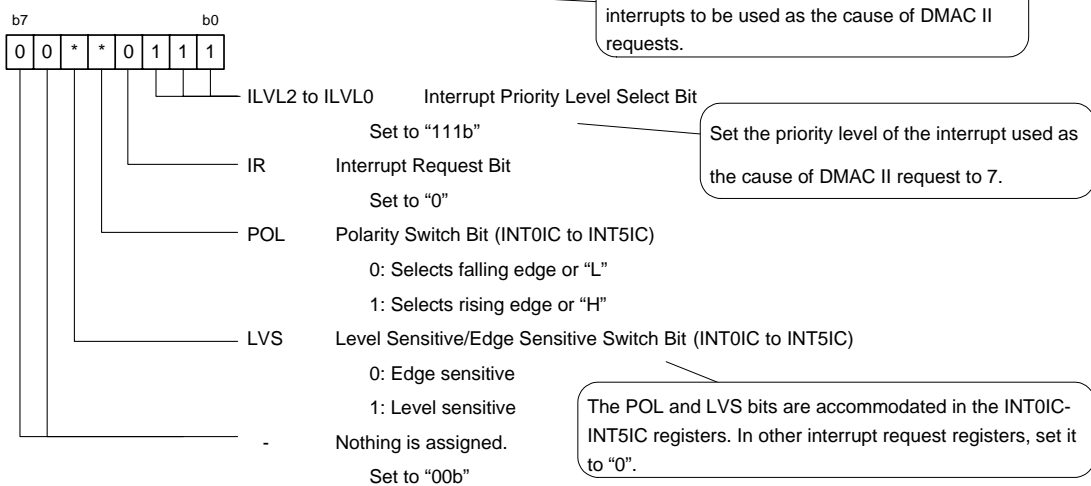
(4) Transfer destination address (DADR)



(5) RLVL register



(6) Interrupt Control Register



4. Example of a Sample Program

4.1 C language source

```

/*****
/* FILENAME: rej05b0641_src.c
/* Ver : 1.00
/* FUNCTION: DMACII(Multiple Transfer)
/*****
/*****
/* include file
/*****
#include <stdio.h>
#include "sfr32c83.h"

/*****
/* DMACII
/*****
struct{
    union{
        struct{
            char size:1; /* Transfer Unit Select Bit */
            char imm:1; /* Transfer Data Select Bit */
            char upds:1; /* Transfer Source Direction Select Bit */
            char updd:1; /* Transfer Destination Direction Select Bit */
            char cnt:3; /* Number of Times a Multiple Transfer Function Select Bit */
            char chain:1; /* Chained Transfer Select Bit */
            char reserve:7;
            char mult:1; /* Multiple Transfer Select Bit */
        }bit;
        unsigned short all;
    }mod;
    unsigned short count; /* Transfer count */
    struct{
        unsigned char near *sadr; /* Transfer source address */
        unsigned char near *dadr; /* Transfer destination address */
    }address[4]; /* Transfer source and destination addresses of transfer number */
}dm_index;

/* Transfer data array */
static unsigned char near data0[5] = {0x11,0x22,0x33,0x44,0x55};
static unsigned char near data1[5] = {0x66,0x77,0x88,0x99,0xaa};
static unsigned char near data2[5] = {0xbb,0xcc,0xdd,0xee,0xff};
static unsigned char near data3[5] = {0x5a,0xa5,0x69,0x96,0x87};

/* Transfer destination memory */
static unsigned char near dest0;
static unsigned char near dest1;
static unsigned char near dest2;
static unsigned char near dest3;
/*****
/* main
/*****
void main(void){
    asm(" fclr i "); /* Interrupt disable */
    /* DMACII setting */
    dm_index.mod.all = 0x8046; /* Transfer Unit: 8bit */
                                /* Transfer Data: Memory */
                                /* Transfer Source: Forward */
                                /* Transfer Destination: Fixed */
                                /* Number of multiple transfer:4 */
                                /* Chained Transfer: None */
                                /* Multiple Transfer: Have */

    dm_index.count = 5; /* number of transfer = 5 */
    dm_index.address[0].sadr = data0; /* Source of transfer = beginning address of the data array */
    dm_index.address[0].dadr = &dest0; /* Destination of transfer*/
    dm_index.address[1].sadr = data1; /* Source of transfer = beginning address of the data array */
    dm_index.address[1].dadr = &dest1; /* Destination of transfer*/
    dm_index.address[2].sadr = data2; /* Source of transfer = beginning address of the data array */
    dm_index.address[2].dadr = &dest2; /* Destination of transfer*/
    dm_index.address[3].sadr = data3; /* Source of transfer = beginning address of the data array */
    dm_index.address[3].dadr = &dest3; /* Destination of transfer*/

    /* Set the interrupt used for DMAC II */

```



```

rlvl = 0x20;          /* Interrupt priority level 7 is used for DMAC II transfers */
int0ic = 0x07;       /* INTO interrupt level 7 (used for DMACII) */

while(1);
}

```

4.2 Relocatable Vector Tables

```

;-----
; variable vector section
;-----
        .section vector,ROMDATA          ; variable vector table
        .org      VECTOR_ADR

        .lword   dummy_int              ; BRK (software int 0)
        .lword   dummy_int              ;
        .lword   dummy_int              ;
        .lword   dummy_int              ;
        .lword   dummy_int              ;
        .lword   dummy_int              ;
        .lword   dummy_int              ;
        .lword   dummy_int              ;
        .lword   dummy_int              ; DMA0 (software int 8)

;
;
;          (Omission)
;
        .lword   dummy_int              ; INT5 (software int 26)
        .lword   dummy_int              ; INT4 (software int 27)
        .lword   dummy_int              ; INT3 (software int 28)
        .lword   dummy_int              ; INT2 (software int 29)
        .lword   dummy_int              ; INT1 (software int 30)
        .glb     _dm_index
        .lword   _dm_index              ; INT0 (software int 31)
        .lword   dummy_int              ; TIMER B5 (software int 32)

;
;
;          (Omission)
;
;

```

5. Reference

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M32C/80 Group Hardware Manual

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