Abstract

This document describes the method for performing single transfer by activating DMAC II in the R32C/100 Series.

Products

MCUs: R32C/116 Group, R32C/117 Group, and R32C/118 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.
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1. Specifications

When an INT0 interrupt request is generated, DMAC II is activated, and data is transferred from memory to memory.

Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows a Usage Example.

<table>
<thead>
<tr>
<th>Peripheral Function</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMAC II</td>
<td>Memory-to-memory transfer</td>
</tr>
<tr>
<td>INT0 interrupt</td>
<td>Trigger for DMAC II</td>
</tr>
<tr>
<td>Timer A (timer A1)</td>
<td>Wait for PLL oscillation to stabilize</td>
</tr>
</tbody>
</table>

![Figure 1.1 Usage Example](image-url)
2. **Operation Confirmation Conditions**

The sample code accompanying this application note has been run and confirmed under the conditions below.

<table>
<thead>
<tr>
<th>Item</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU used</td>
<td>R5F64189DFD (R32C/118 Group)</td>
</tr>
<tr>
<td>Operating frequencies</td>
<td>Main clock: 16 MHz&lt;br&gt;PLL clock: 100 MHz&lt;br&gt;Base clock: 50 MHz&lt;br&gt;CPU clock: 50 MHz&lt;br&gt;Peripheral bus clock: 25 MHz&lt;br&gt;Peripheral function clock source: 25 MHz</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>5 V</td>
</tr>
<tr>
<td>Integrated development</td>
<td>Renesas Electronics Corporation&lt;br&gt;High-performance Embedded Workshop Version 4.07</td>
</tr>
<tr>
<td>environment</td>
<td>R32C/100 Series C Compiler V.1.02 Release 01</td>
</tr>
</tbody>
</table>
| C compiler                | Compile options<br>-D__STACKSIZE__ =0X300<br>-D__ISTACKSIZE__ =0X300<br>-DVECTOR_ADR=0xFFFFFBDC -c -finfo -dir "$(CONFIGDIR)"
| (Default setting is used in the integrated development environment.) |                             |
| Operating mode            | Single-chip mode                                                          |
| Sample code version       | Version 1.00                                                              |
| Board used                | Renesas Starter Kit for R32C/118 (product name: R0K564189S000BE)          |

3. **Reference Application Note**

The application note associated with this application note is listed below. Refer to the following application note for additional information.

- R32C/100 Series Configuring PLL Mode (REJ05B1221-0100)

4. **Hardware**

4.1 **Pin Used**

Table 4.1 lists the Pin Used and Its Function.

<table>
<thead>
<tr>
<th>Table 4.1 Pin Used and Its Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin Name</td>
</tr>
<tr>
<td>P8_2/INT0</td>
</tr>
</tbody>
</table>
5. Software

5.1 Operation Overview

When an interrupt request is generated with interrupt request level 7, DMAC II is activated to perform memory-to-memory transfer. In this application note, the INT0 interrupt is set to interrupt request level 7.

(1) DMAC II initial settings

Set the DMAC II index and a trigger for DMAC II. Also set the INT0 pin and INT0 interrupt control register to use the INT0 interrupt as a trigger for DMAC II.

Settings for the DMAC II index are as follows:
- Transfer size: 8 bits
- Transfer types: Memory
- Source addressing: Increment
- Destination addressing: Fixed
- Calculation transfer: Not used
- Transfer mode: Single transfer
- Transfer complete interrupt: Not used
- Chained transfer: Not used
- Number of transfers (COUNT): Five times
- Source address (SADR): Start address of source data (400h)
- Destination address (DADR): Destination address (1000h)

(2) When the INT0 interrupt is generated

When the INT0 interrupt is generated, data set in the DMAC II index is transferred from the source address (SADR) to the destination address (DADR). After the data is transferred, 1 is subtracted from the transfer count (COUNT) and 1 is added to SADR. (1)

When COUNT becomes 0, even if the INT0 interrupt is generated, DMA II transfer is not performed.

Note:
- 1. When the transfer size is 8 bits. When the transfer size is 16 bits, 2 is added.

Figure 5.1 shows a DMA II Transfer Operation Example.
Figure 5.1 DMA II Transfer Operation Example
5.2 Invariable Table

Table 5.1 lists the Invariables Used in the Sample Code.

<table>
<thead>
<tr>
<th>Invariable Name</th>
<th>Setting Value</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEST_ADDRESS</td>
<td>1000h</td>
<td>DMA II destination address</td>
</tr>
<tr>
<td>TRANS_COUNT</td>
<td>5</td>
<td>Number of DMA II transfers</td>
</tr>
</tbody>
</table>

5.3 Structure/Union List

Figure 5.2 shows the Structure/Union Used in the Sample Code.

```c
// DMAC II index
struct{
    union {
        struct{
            char    size:1;                             // Transfer size select bit
            char    imm:1;                             // Transfer source select bit
            char    upds:1;                            // Source addressing select bit
            char    updd:1;                            // Destination addressing select bit
            char    oper:1;                             // Calculation transfer select bit
            char    brst:1;                              // Burst transfer select bit
            char    inte:1;                              // Transfer complete interrupt select bit
            char    chain:1;                           // Chained transfer select bit
            char    reserve:7;                        //
            char    mult:1;                             // Multiple transfer select bit
        }mod_bit;
        unsigned short mod_word;
    }mod;
    unsigned short count;                         // transfer counter
    unsigned char far *sadr;                     // source address
    unsigned char far *dadr;                     // destination address
}dm_index;
```

Figure 5.2 Structure/Union Used in the Sample Code

Set the starting address of the DMAC II index to the interrupt vector for the DMAC II triggerable peripheral interrupt source.

In this application note, the INT0 interrupt is used as a trigger for DMAC II.

Figure 5.3 shows a setting example of the asm function in a C language program.

```c
asm( " .rvector 31, _dm_index" ); // Define DMAC II Index (Software Interrupt Number 31)
```

Figure 5.3 Setting Example for the Starting Address of the DMAC II Index to the Interrupt Vector
5.4 Variable Table
Table 5.2 lists the Global Variables.

<table>
<thead>
<tr>
<th>Type</th>
<th>Variable Name</th>
<th>Contents</th>
<th>Function Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char</td>
<td>data[]</td>
<td>DMA II source data (11h, 22h, 33h, 44h, and 55h)</td>
<td>DMACII_init</td>
</tr>
<tr>
<td>struct</td>
<td>dm_index</td>
<td>DMAC II index</td>
<td>DMACII_init</td>
</tr>
</tbody>
</table>

5.5 Function Table
Table 5.3 lists the Functions.

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>SetPLLClock</td>
<td>PLL clock setting</td>
</tr>
<tr>
<td>DMACII_init</td>
<td>DMAC II initialization</td>
</tr>
</tbody>
</table>

5.6 Function Specifications
The following tables list the sample code function specifications.

SetPLLClock
Outline: PLL clock setting
Header: None
Declaration: void SetPLLClock (void)
Explanation: Set each clock frequency in PLL mode.
Argument: None
Returned value: None
Remark:

DMACII_init
Outline: DMAC II initial setting
Header: None
Declaration: void DMACII_init (void)
Explanation: Initialize DMAC II.
Argument: None
Returned value: None
Remark:
5.7 Flowcharts

5.7.1 Main Processing

Figure 5.4 shows the Main Processing.

![Flowchart of Main Processing]

Figure 5.4 Main Processing

1. Disable maskable interrupts
   - I flag ← 0
   - PLL clock setting
     - SetPLLClk()

2. P8_2/INT0 pin setting
   - P8_2S register ← 00h
     - Bits PSEL2 to PSEL0 = 000b
     - NOD bit = 0
     - I/O port P8_2
     - Push-pull output
   - PD8 register
     - PD8_2 bit ← 0
     - Input port

3. DMAC II initial setting
   - DMACII_init()

4. Set input polarity of INT0 interrupt and interrupt request level
   - IFSR0 register ← 00h
     - IFSR00 bit = 0
     - One edge
   - INTOIC register ← 07h
     - Bits ILVL2 to ILVL0 = 111b
     - Level 7
     - IR bit = 0
     - No interrupt requested
     - POL bit = 0
     - Select the falling edge or a low.
     - LVS bit = 0
     - Edge sensitive
### 5.7.2 PLL Clock Setting

Figure 5.5 shows the PLL Clock Setting.

#### Set PLL Clock

1. **Set timer to wait for PLL stabilization time of 1 ms**
   - PRCR register
   - PRC2 bit ← 1
   - PLC0 register
   - Bits MCV4 to MCV0 = 00100b
   - Bits SCV2 to SCV0 = 000b
   - SEO bit = 0

2. **Set PLL clock to 100 MHz**
   - PRCR register
   - PRC2 bit ← 1
   - PLC1 register ← 03h
   - Bits RCV3 to RCV0 = 0011b
   - SEO bit = 0

3. **Wait for oscillation of the PLL clock to be stabilized (1 ms)**
   - PRR register ← AAh
   - PBC register
   - Bits PRD4 to PRD0 ← 00100b
   - Bits PWR4 to PWR0 ← 00101b
   - CCR register ← 1Fh
   - Bits BCD1 to BCD0 = 11b
   - Bits CCD1 to CCD0 = 11b
   - Bits PCD1 to PCD0 = 01b
   - BCS bit = 0

4. **Set peripheral bus timing**
   - PRR register ← 00h
   - PBC register
   - Bits PRD4 to PRD0 ← 00100b
   - Bits PWR4 to PWR0 ← 00101b

5. **Set base clock, CPU clock and peripheral bus clock**
   - PRR register ← 00h
   - PBC register
   - Bits PRD4 to PRD0 ← 00100b
   - Bits PWR4 to PWR0 ← 00101b

6. **Set peripheral clock source divide ratio**
   - PRR register ← 00h
   - PM3 register ← 10h
   - PM3 register ← 0

#### Notes:

1. Refer to the hardware user’s manual for details of setting value.
2. The value in the PRR register should be left as AAh (write enabled) until the register protected by the PRR register is set in process box number 5.

---

**Figure 5.5 PLL Clock Setting**
### 5.7.3 DMAC II Initial Setting

Figure 5.6 shows the DMAC II Initial Setting.

<table>
<thead>
<tr>
<th>DMACII_init</th>
<th>RIPL1 register ← 20h</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RIPL2 register ← 20h</td>
</tr>
<tr>
<td></td>
<td>FSIT bit = 0</td>
</tr>
<tr>
<td></td>
<td>DMAII bit = 1</td>
</tr>
</tbody>
</table>

: Interrupt request level 7 is used for DMA II transfer. \(^{(1, 2)}\)

![Diagram](image)

#### Notes:
1. The DMA II transfer is not affected by the I flag or the IPL.
2. Simultaneous use of the fast interrupt and DMAC II is not available.
6. Sample Code
Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents
R32C/118 Group User's Manual: Hardware Rev.1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02
C Compiler User’s Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

8. Website and Support
Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
## Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Dec. 28, 2010</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.
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