R32C/100 Series

Using DMAC II in Single Transfer Mode

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Abstract

This document describes the method for performing single transfer by activating DMAC II in the R32C/100 Series.

Products

MCUs: R32C/116 Group, R32C/117 Group, and R32C/118 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

When an INT0 interrupt request is generated, DMAC II is activated, and data is transferred from memory to memory.
Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows a Usage Example.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
DMAC II	Memory-to-memory transfer
INT0 interrupt	Trigger for DMAC II
Timer A (timer A1)	Wait for PLL oscillation to stabilize

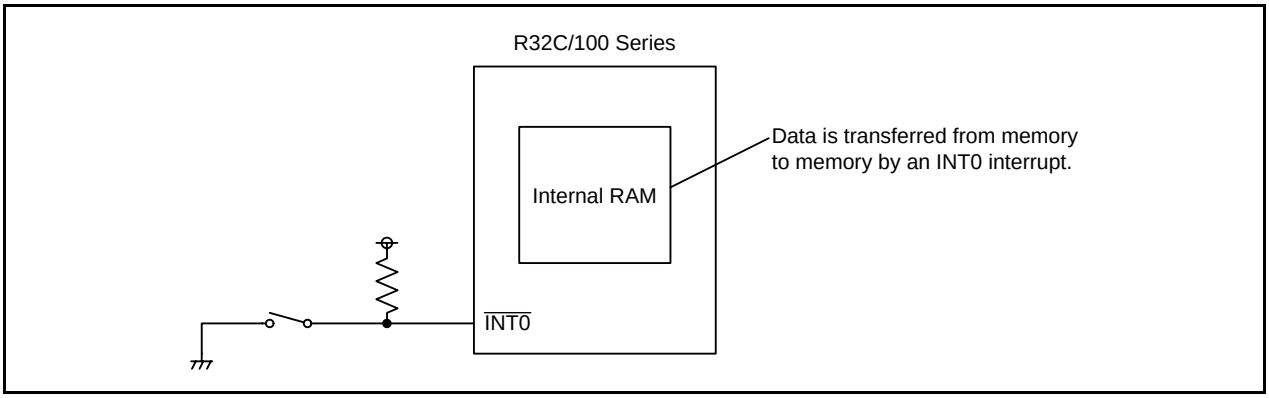


Figure 1.1 Usage Example

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F64189DFD (R32C/118 Group)
Operating frequencies	Main clock: 16 MHz PLL clock: 100 MHz Base clock: 50 MHz CPU clock: 50 MHz Peripheral bus clock: 25 MHz Peripheral function clock source: 25 MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.07
C compiler	Renesas Electronics Corporation R32C/100 Series C Compiler V.1.02 Release 01
	Compile options -D__STACKSIZE__=0X300 -D__ISTACKSIZE__=0X300 -DVECTOR_ADR=0x0FFFFFBDC -c -finfo -dir "$(CONFIGDIR)" (Default setting is used in the integrated development environment.)
Operating mode	Single-chip mode
Sample code version	Version 1.00
Board used	Renesas Starter Kit for R32C/118 (product name: R0K564189S000BE)

3. Reference Application Note

The application note associated with this application note is listed below. Refer to the following application note for additional information.

- R32C/100 Series Configuring PLL Mode (REJ05B1221-0100)

4. Hardware

4.1 Pin Used

Table 4.1 lists the Pin Used and Its Function.

Table 4.1 Pin Used and Its Function

Pin Name	I/O	Function
P8_2/$\overline{\text{INT0}}$	Input	DMAC II trigger (INT0 interrupt) input

5. Software

5.1 Operation Overview

When an interrupt request is generated with interrupt request level 7, DMAC II is activated to perform memory-to-memory transfer. In this application note, the INT0 interrupt is set to interrupt request level 7.

(1) DMAC II initial settings

Set the DMAC II index and a trigger for DMAC II. Also set the $\overline{\text{INT0}}$ pin and INT0 interrupt control register to use the INT0 interrupt as a trigger for DMAC II.

Settings for the DMAC II index are as follows:

- Transfer size: 8 bits
- Transfer types: Memory
- Source addressing: Increment
- Destination addressing: Fixed
- Calculation transfer: Not used
- Transfer mode: Single transfer
- Transfer complete interrupt: Not used
- Chained transfer: Not used
- Number of transfers (COUNT): Five times
- Source address (SADR): Start address of source data (400h)
- Destination address (DADR): Destination address (1000h)

(2) When the INT0 interrupt is generated

When the INT0 interrupt is generated, data set in the DMAC II index is transferred from the source address (SADR) to the destination address (DADR). After the data is transferred, 1 is subtracted from the transfer count (COUNT) and 1 is added to SADR. (1)

When COUNT becomes 0, even if the INT0 interrupt is generated, DMA II transfer is not performed.

Note:

1. When the transfer size is 8 bits. When the transfer size is 16 bits, 2 is added.

Figure 5.1 shows a DMA II Transfer Operation Example.

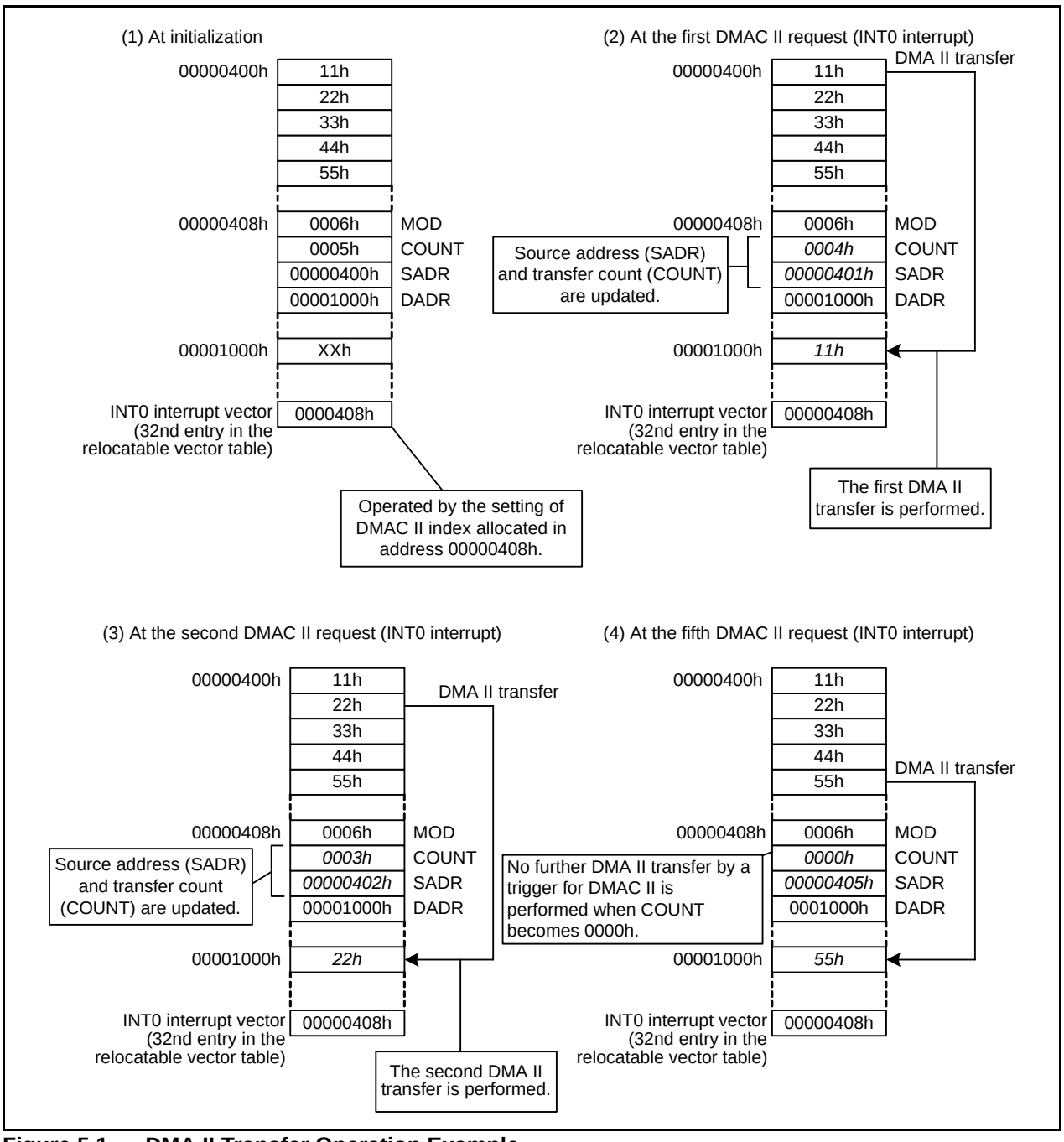


Figure 5.1 DMA II Transfer Operation Example

5.2 Invariable Table

Table 5.1 lists the Invariables Used in the Sample Code.

Table 5.1 Invariables Used in the Sample Code

Invariable Name	Setting Value	Contents
DEST_ADDRESS	1000h	DMA II destination address
TRANS_COUNT	5	Number of DMA II transfers

5.3 Structure/Union List

Figure 5.2 shows the Structure/Union Used in the Sample Code.

```
// DMAC II index

struct{
    union {
        struct{
            char    size:1;             // Transfer size select bit
            char    imm:1;              // Transfer source select bit
            char    upds:1;             // Source addressing select bit
            char    updd:1;             // Destination addressing select bit
            char    oper:1;             // Calculation transfer select bit
            char    brst:1;             // Burst transfer select bit
            char    inte:1;             // Transfer complete interrupt select bit
            char    chain:1;            // Chained transfer select bit
            char    reserve:7;          //
            char    mult:1;             // Multiple transfer select bit
        }mod_bit;
        unsigned short mod_word;
    }mod;
    unsigned short count;               // transfer counter
    unsigned char far *sadr;            // source address
    unsigned char far *dadr;            // destination address
}dm_index;
```

Figure 5.2 Structure/Union Used in the Sample Code

Set the starting address of the DMAC II index to the interrupt vector for the DMAC II triggerable peripheral interrupt source.
In this application note, the INT0 interrupt is used as a trigger for DMAC II.
Figure 5.3 shows a setting example of the asm function in a C language program.

```
asm( "   .rvector 31, _dm_index" );     // Define DMAC II Index (Software Interrupt Number 31)
```

Figure 5.3 Setting Example for the Starting Address of the DMAC II Index to the Interrupt Vector

5.4 Variable Table

Table 5.2 lists the Global Variables.

Table 5.2 Global Variables

Type	Variable Name	Contents	Function Used
unsigned char	data[]	DMA II source data (11h, 22h, 33h, 44h, and 55h)	DMACII_init
struct	dm_index	DMAC II index	DMACII_init

5.5 Function Table

Table 5.3 lists the Functions.

Table 5.3 Functions

Function Name	Outline
SetPLLClock	PLL clock setting
DMACII_init	DMAC II initialization

5.6 Function Specifications

The following tables list the sample code function specifications.

SetPLLClock	
Outline	PLL clock setting
Header	None
Declaration	void SetPLLClock (void)
Explanation	Set each clock frequency in PLL mode.
Argument	None
Returned value	None
Remark	

DMACII_init	
Outline	DMAC II initial setting
Header	None
Declaration	void DMACII_init (void)
Explanation	Initialize DMAC II.
Argument	None
Returned value	None
Remark	

5.7 Flowcharts

5.7.1 Main Processing

Figure 5.4 shows the Main Processing.

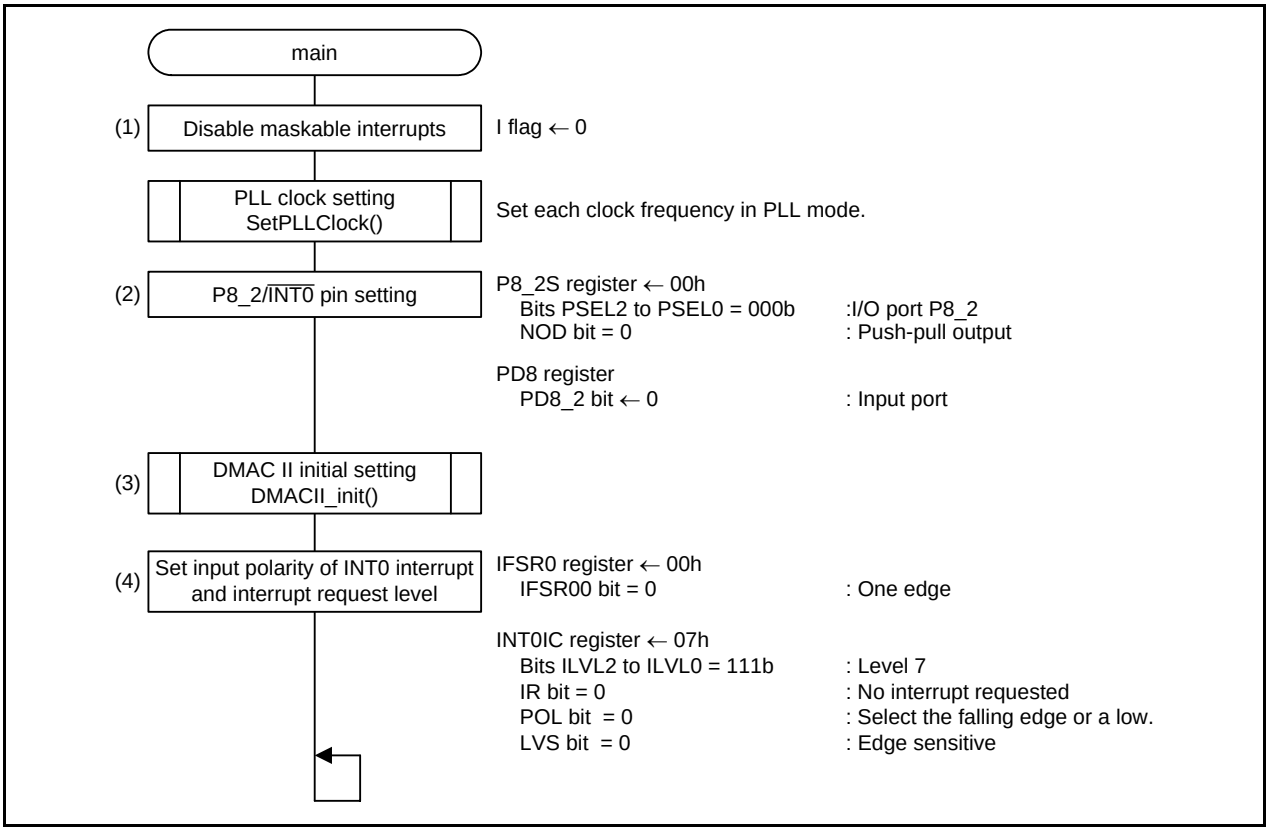
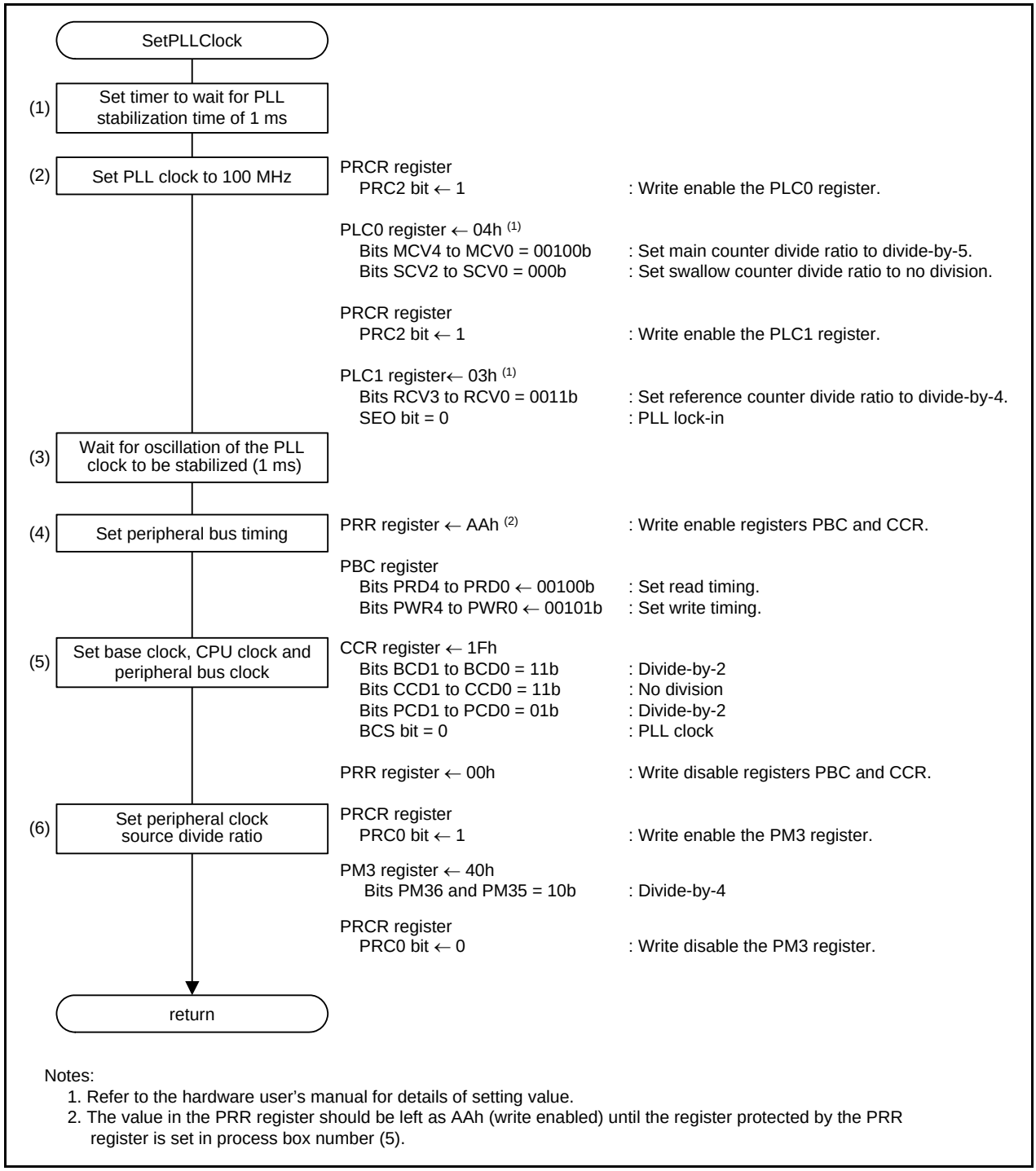


Figure 5.4 Main Processing

5.7.2 PLL Clock Setting

Figure 5.5 shows the PLL Clock Setting.



Notes:
1. Refer to the hardware user's manual for details of setting value.
2. The value in the PRR register should be left as AAh (write enabled) until the register protected by the PRR register is set in process box number (5).

Figure 5.5 PLL Clock Setting

5.7.3 DMAC II Initial Setting

Figure 5.6 shows the DMAC II Initial Setting.

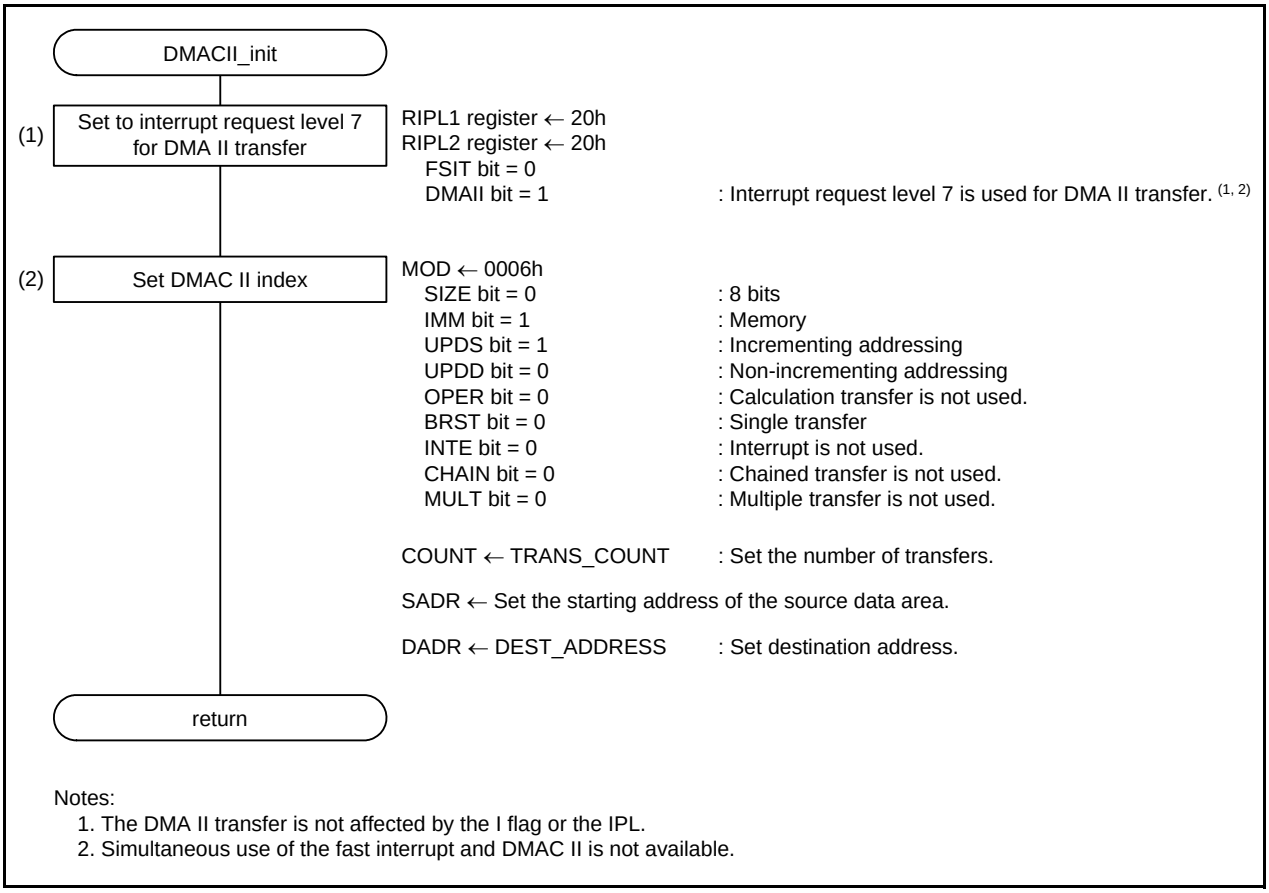


Figure 5.6 DMAC II Initial Setting

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

R32C/116 Group User's Manual: Hardware Rev.1.10
R32C/117 Group User's Manual: Hardware Rev.1.10
R32C/118 Group User's Manual: Hardware Rev.1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

8. Website and Support

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Revision History	R32C/100 Series Using DMAC II in Single Transfer Mode

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 28, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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