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H8S/20103, H8S/20203, and H8S/20223 Groups

Using a Compare-Match Signal from Timer RD to Activate the DTC

Introduction

The event link controller (ELC) in products of the H8S/20103, H8S/20203, and H8S/20223 Groups is used to set up activation of the data transfer controller (DTC) by the compare match signal for a match between the counter of timer RD_0, channel 0, and GRA_0. Activation proceeds without CPU intervention.

Target Devices

H8S/20103 (R4F20103)

H8S/20203 (R4F20203)

H8S/20223 (R4F20223)

Frequency Used in Confirming Operation

System clock $\phi = \phi osc = 20$ MHz

Contents

1. Specifications

Specifications of this sample task are as given below. Figure 1 gives an schematic view of how the event controller sets up DTC activation by compare matches of timer RD and figure 2 shows the output operation obtained by starting the DTC on compare matches of timer RD.

1. A table specifying the timing of the PWM waveforms to be output is created and placed in ROM.
2. The address where the DTC register information starts is stored in the address corresponding to the activation source within the DTC vector table.
3. Settings are made so that timer RD_0 channel 0 is placed in PWM mode and TRDCNT_0 is cleared on a compare match with GRA_0.
4. The period of the PWM waveforms is set in GRA_0, and settings to control the timing of the output of PWM signals on pins FTIOB0, FTIOC0 and FTIOD0 are made in GRB_0, GRC_0 and GRD_0, respectively.
5. The DTC is placed in block transfer mode with “word” as the unit of transfer.
6. The source address for data transfer is specified as the first address of the area containing the table to control the timing of PWM waveform output.
7. The destination address for data transfer is specified as the address of GRB_0.
8. The event selected in ELSR30 is set as the activation source for the DTC.
9. The compare match A signal from timer RD_0 channel 0 is selected as the event signal to be linked with DTC operation.
10. The event interrupt signal corresponding to ELSR30 is enabled.
11. Event linkage is enabled.
12. Output on pins FTIOB0, FTIOC0 and FTIOD0 is enabled.
13. Operation of timer RD1 channel 0 is started.
14. The I bit is cleared to enable interrupts.
15. Every time the compare match signal for a match between timer RD_0 channel 0 and GRA_0 is generated, the DTC is activated and the output timing of PWM waveforms is updated, and both operations proceed without CPU intervention.

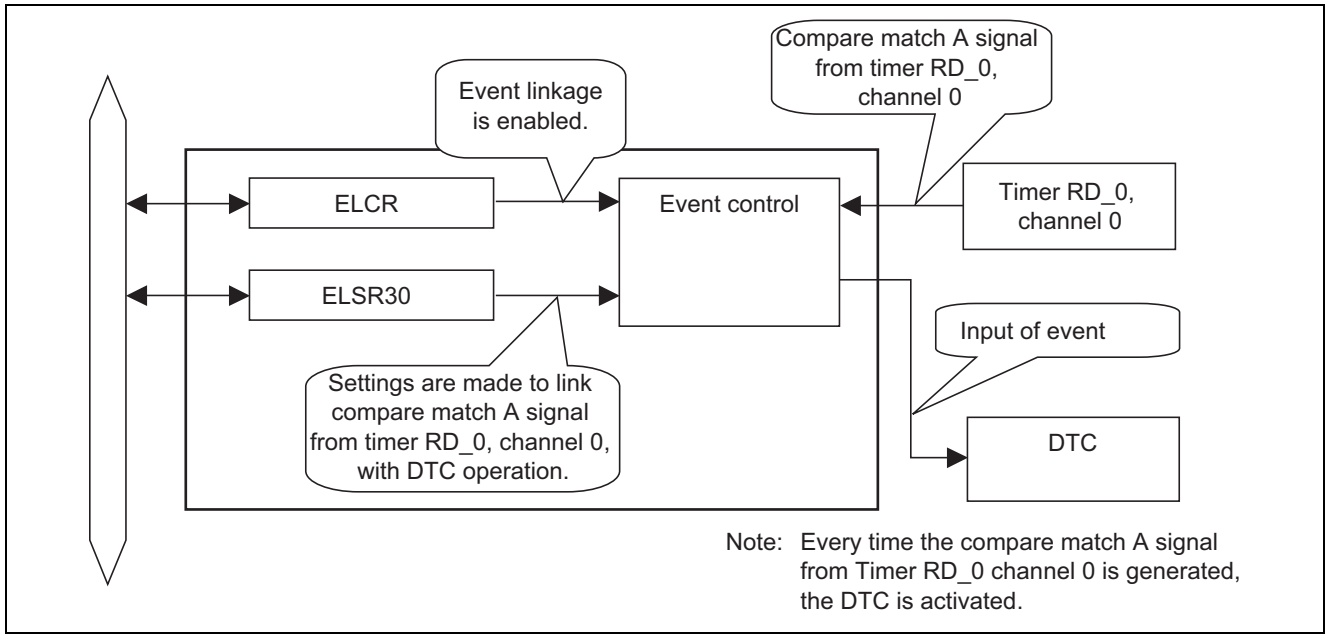


Figure 1 Schematic View of How a Compare Match of Timer RD Activates the DTC

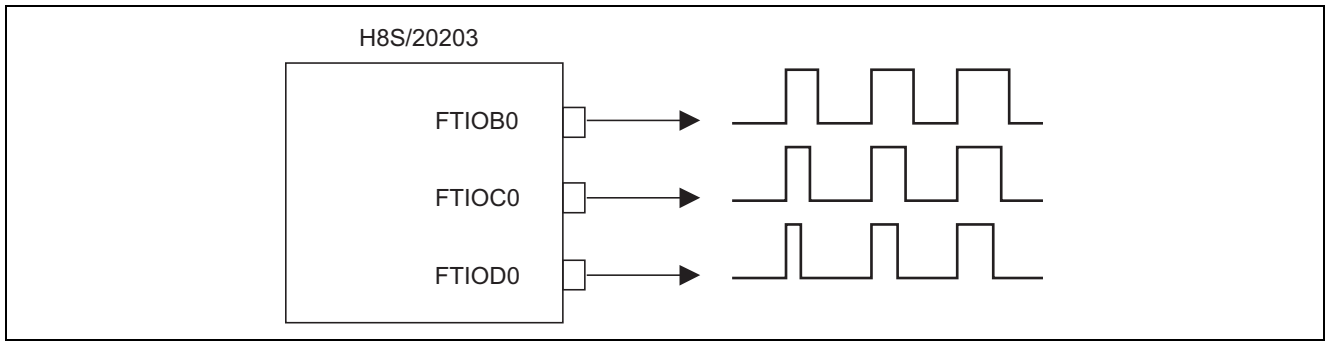


Figure 2 Pin Output Operation Obtained by Using Timer RD Compare Match for DTC Activation

2. Description of Modules Used

2.1 Event Link Controller (ELC)

The features of the ELC are described below. Figure 3 is a block diagram of the ELC.

The ELC connects events generated by the various peripheral modules to other modules. This function allows direct cooperation between modules, without CPU intervention.

- Fifty-nine event signals can be directly connected to modules.
- The operation of timer modules can be selected when an event is input to the timer module.
- Events can be connected to ports 3 and 6.
- Settings for ports enable the generation of events in the form of signals on port pins.
- A single bit or any grouping of several bits can be set up for event connection on the ports used for connecting events.
- The event generation timer can be used to set up the generation of signals on four channels as events with the desired intervals.

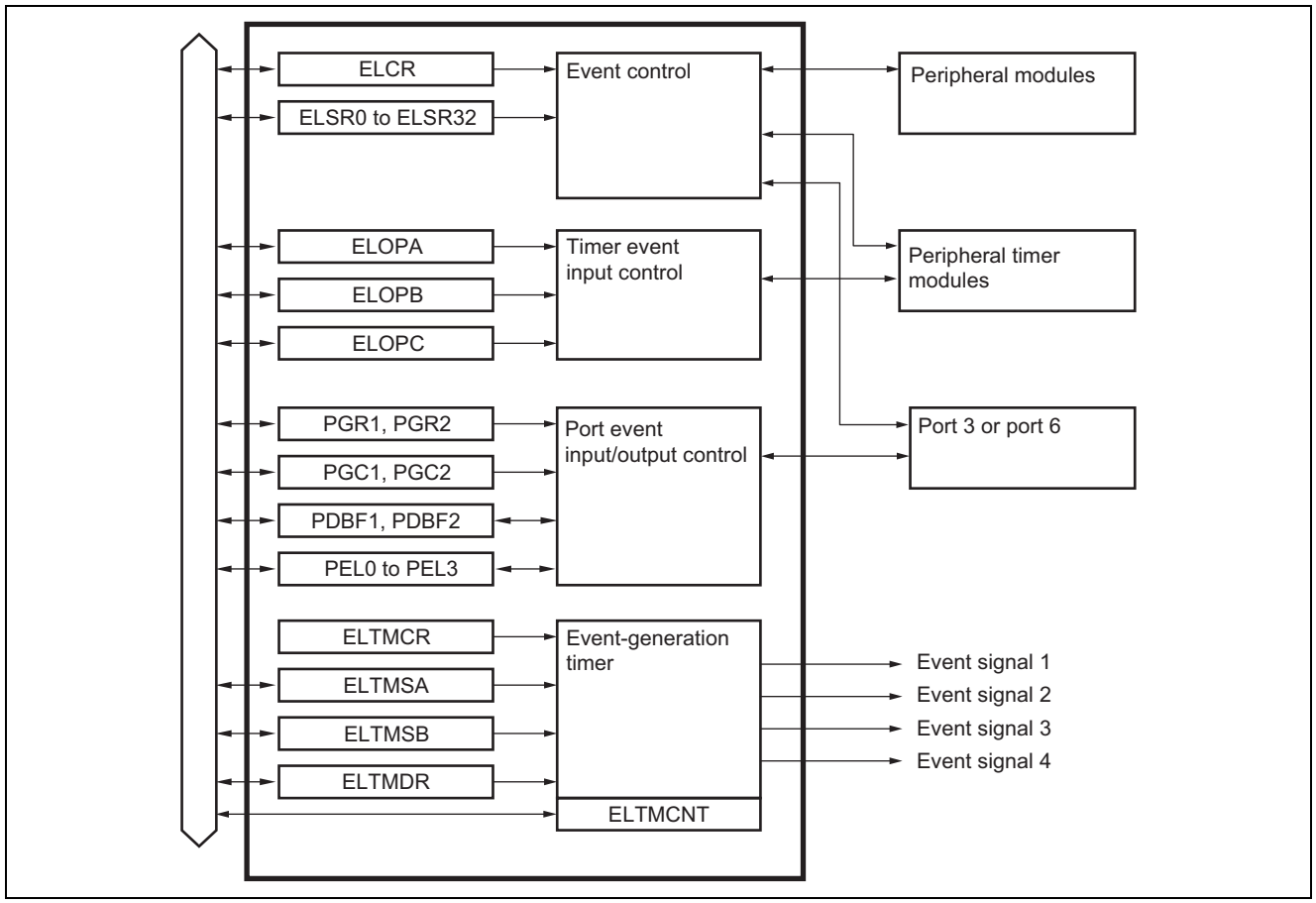


Figure 3 Block Diagram of Event Link Controller

2.2 Timer RD

The features of timer RD are described below.

This LSI has two units of 16-bit timers (timer RD_0 and timer RD_1), each of which has two channels. Table 1 lists the timer RD functions, table 2 lists the channel configuration of timer RD, and figure 4 is a block diagram of the entire timer RD. Block diagrams of channels 0 and 1 are shown in figures 5 and 6.

Timer RD_0 has the same features as timer RD_1. Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted (products of the H8S/20103 Group do not include timer RD_1).

- Capability to process up to eight inputs/outputs
- Eight general registers (GR): four registers for each channel
  Independently assignable output compare or input capture functions
- Selection of seven counter clock sources:
  Six internal clock signals (with the high-speed on-chip oscillator operating at 32 or 40 MHz: ϕ, ϕ/2, ϕ/4, ϕ/8, ϕ/32, and ϕ/40) and an external clock
- Seven selectable operating modes
  - Timer mode
    Output compare function (Selection of 0 output, 1 output, or toggled output)
    Input capture function (Rising edge, falling edge, or both edges)
  - Synchronous operation
    Timer counters_0 and _1 (TRDCNT_0 and TRDCNT_1) can be written simultaneously.
    Simultaneous clearing by compare match or input capture is possible.
  - PWM mode
    Up to six-phase PWM output can be provided with desired duty ratio.
  - PWM3 mode
    One-phase PWM output for non-overlapped normal and counter phases
  - Reset-synchronized PWM mode
    Three-phase PWM output for normal and counter phases
  - Complementary PWM mode
    Three-phase PWM output for non-overlapped normal and counter phases
    The A/D conversion start trigger can be set for PWM cycles.
  - Buffered operation
    The input capture registers can be configured for buffered operation.
    The output compare register can automatically be modified.
- High-speed access by the internal 16-bit bus
  16-bit TRDCNT and GR registers can be accessed in high speed by a 16-bit bus interface.
- Any initial timer output value can be set.
- Output of the timer can be disabled by an external trigger.
- Eleven interrupt sources
  Four compare match/input capture interrupts and an overflow interrupt are available for each channel. An underflow interrupt can be set for channel 1.

Table 1 Functions of Timer RD (One Unit)

Item		Channel 0	Channel 1
Count clock		Internal clocks: ϕ, ϕ/2, ϕ/4, ϕ/8, ϕ/32, ϕ/40 External clock: FTIOA0 (TCLK)	
General registers (output compare/input capture registers)		GRA_0, GRB_0, GRC_0, GRD_0	GRA_1, GRB_1, GRC_1, GRD_1
Buffer registers		GRC_0, GRD_0	GRC_1, GRD_1
I/O pins		FTIOA0, FTIOB0, FTIOC0, FTIOD0	FTIOA1, FTIOB1, FTIOC1, FTIOD1
Counter clearing function		Compare match/input capture of GRA_0, GRB_0, GRC_0, or GRD_0	Compare match/input capture of GRA_1, GRB_1, GRC_1, or GRD_1
Compare match output	0 output	Yes	Yes
	1 output	Yes	Yes
	Toggled output	Yes	Yes
Input capture function		Yes	Yes
Synchronous operation		Yes	Yes
PWM mode		Yes	Yes
PWM3 mode		Yes	Yes
Reset-synchronized PWM mode		Yes	Yes
Complementary PWM mode		Yes	Yes
Buffer function		Yes	Yes
Interrupt sources		Compare match/ input capture A0 to D0 Overflow	Compare match/ input capture A1 to D1 Overflow Underflow

Table 2 Configuration of Timer RD Channels

Unit	Channel	Pin
Timer RD_0 (Unit 0)	0	FTIOA0
		FTIOB0
		FTIOC0
		FTIOD0
	1	FTIOA1
		FTIOB1
		FTIOC1
		FTIOD1
	Shared by channels 0 and 1	$\overline{\text{TRDOI\_0}}$
Timer RD_1 (Unit 1)	2	FTIOA2
		FTIOB2
		FTIOC2
		FTIOD2
	3	FTIOA3
		FTIOB3
		FTIOC3
		FTIOD3
	Shared by channels 2 and 3	$\overline{\text{TRDOI\_1}}$

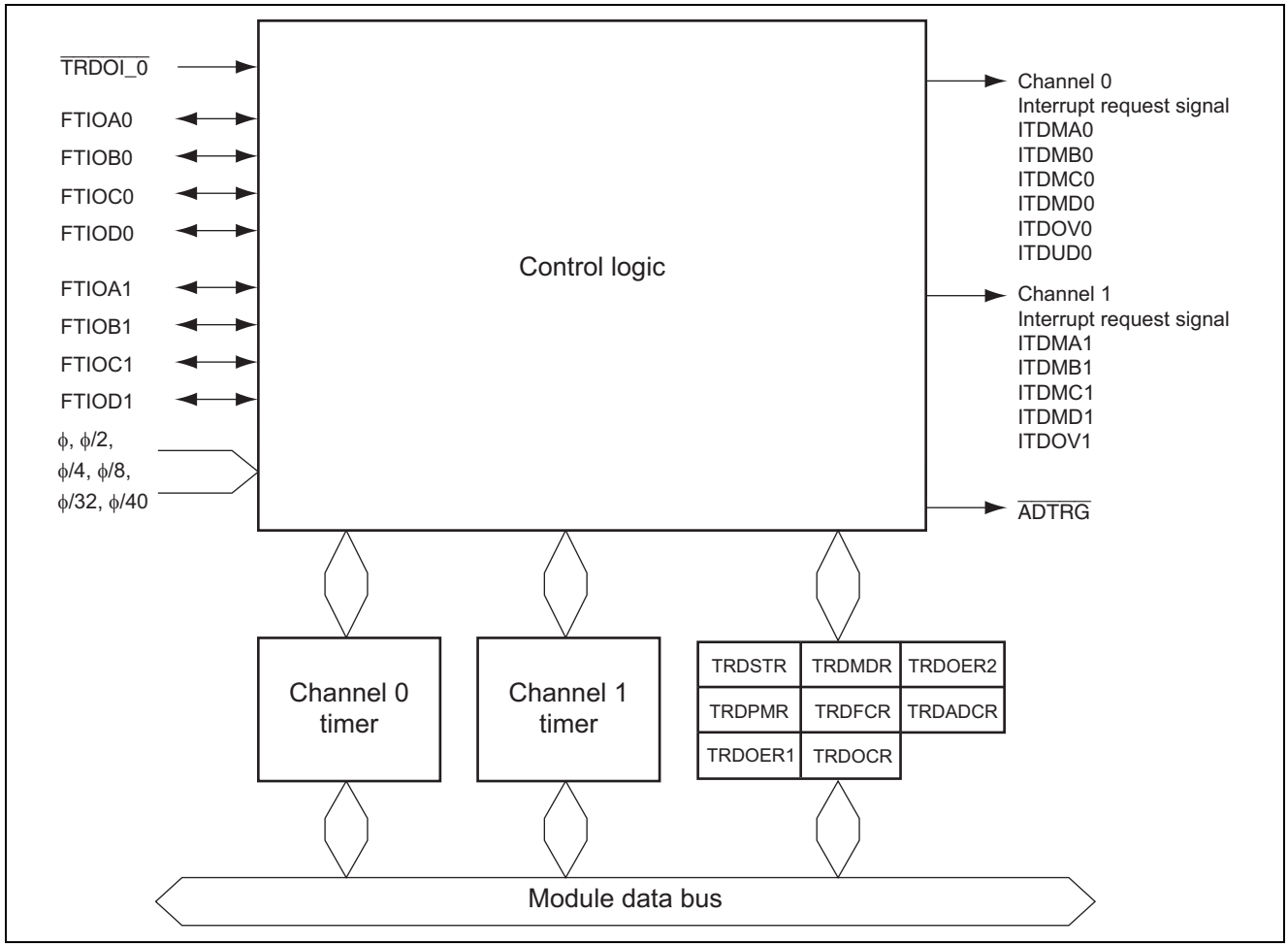


Figure 4 Block Diagram of Timer RD (One Unit)

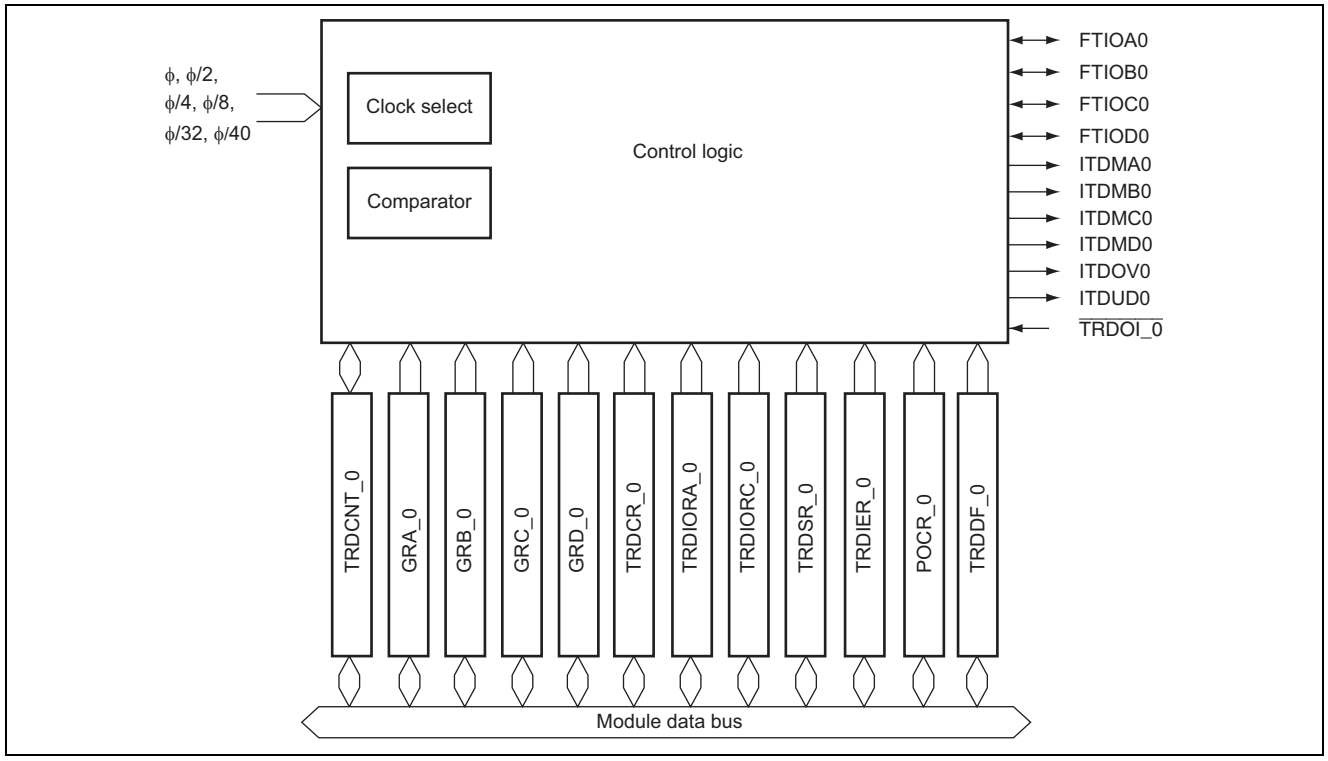


Figure 5 Block Diagram of Timer RD (Channel 0)

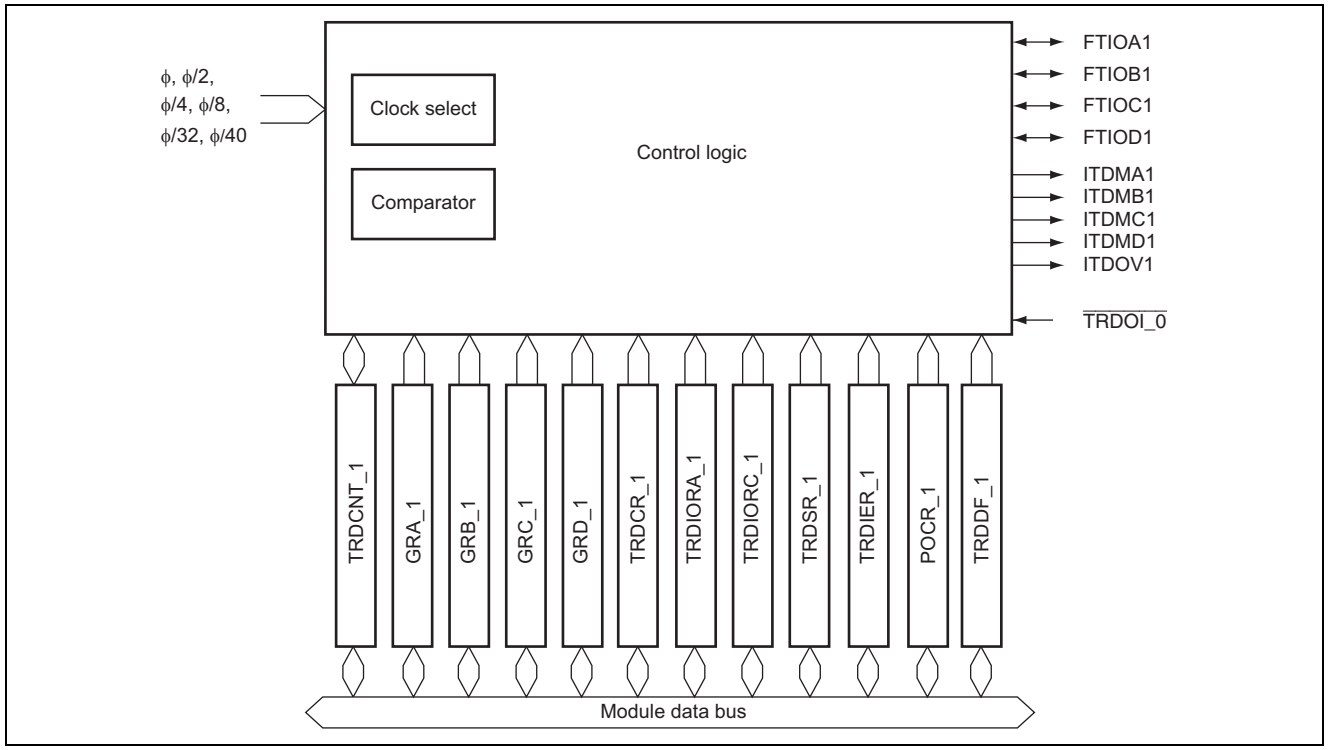


Figure 6 Block Diagram of Timer RD (Channel 1)

2.3 Data Transfer Controller (DTC)

The features of the DTC are described below.

This LSI includes a data transfer controller (DTC). The DTC can be activated by an interrupt or software to transfer data.

Figure 7 is a block diagram of the DTC.

- Transfer possible over any number of channels
- Three transfer modes
  1. Normal mode
     One operation transfers one byte or one word of data.
     Memory address is incremented or decremented by 1 or 2.
     From 1 to 65,536 transfers can be specified.
  2. Repeat mode
     One operation transfers one byte or one word of data.
     Memory address is incremented or decremented by 1 or 2.
     Once the specified number of transfers (1 to 256) has ended, the initial state is restored, and transfer is repeated.
  3. Block transfer mode
     One operation transfers specified one block of data.
     The block size is 1 to 256 bytes or words.
     From 1 to 65,536 transfers can be specified.
     Either the transfer source or the transfer destination is designated as a block area.
- One activation source can trigger a number of data transfers (chained transfer).
- Direct specification of 16-Mbyte address space possible.
- Activation by software is possible.
- Transfer can be set in byte or word units.
- A CPU interrupt can be requested for the interrupt that activated the DTC.
- Module standby mode can be set.

The DTC's register information is stored in the on-chip RAM. A 32-bit bus connects the DTC to the on-chip RAM, enabling 32-bit/1-state reading and writing of the DTC register information.

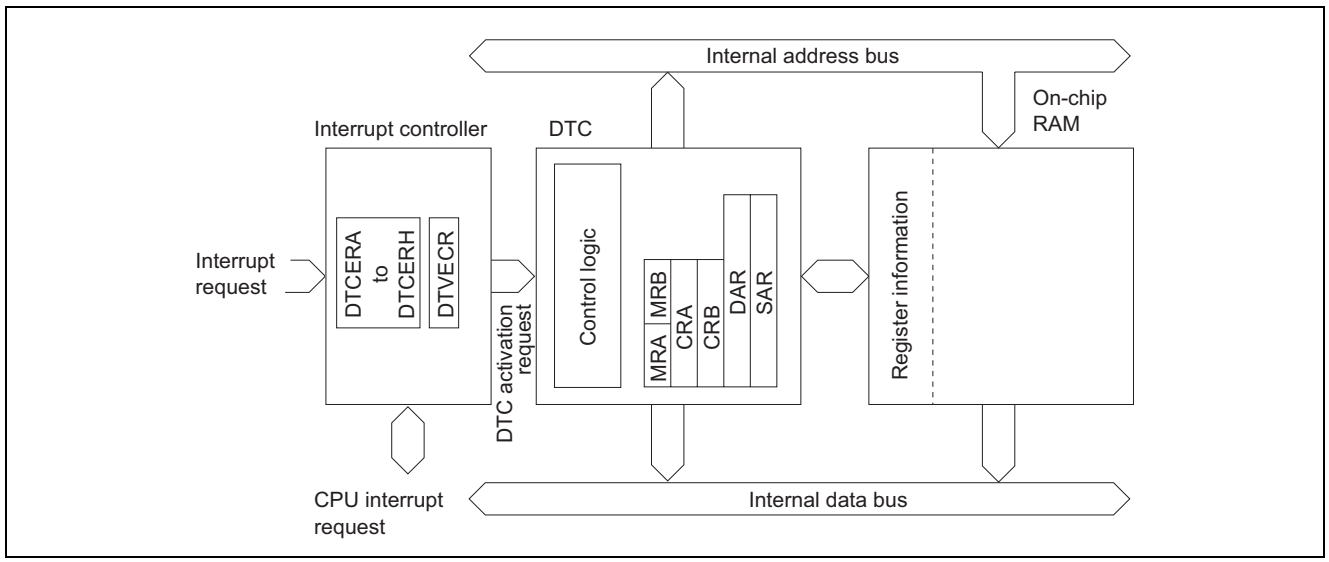


Figure 7 Block Diagram of DTC

2.3.1 Activation Sources

The DTC operates when activated by an interrupt request or by writing to DTVECR by software. An interrupt request can be designated by the DTCER bit. At the end of a data transfer (or the last consecutive transfer in the case of chained transfer), the activation source flag is the RDRF flag of SCI3_1.

When an interrupt has been designated a DTC activation source, existing CPU mask level and interrupt controller priorities have no effect. If there is more than one activation source at the same time, the DTC operates in accordance with the default priorities for the interrupt sources. Table 2 shows a relationship between activation sources and DTCER clear conditions. Figure 8 is a block diagram of DTC activation source control. For details, see the section on the interrupt controller of the *H8S/20103, H8S/20203, H8S/20223 Group Hardware Manual* (REJ09B0465).

Table 3 Relationship between Activation Sources and DTCER Clearing

Activation Source	DISEL = 0 and Specified Number of Transfers Has Not Ended	DISEL = 1 or Specified Number of Transfers Has Ended
Activation by software	The SWDTE bit is cleared to 0	• The SWDTE bit retains the value 1. • Interrupt request to the CPU
Activation by an interrupt	• The corresponding bit of DTCER retains the value 1. • Activation source flag is cleared to 0.	• The corresponding bit of the DTCER bit is cleared to 0. • Activation source flag retains the value 1. • The interrupt that had been the source for activation is issued as an interrupt request for the CPU.

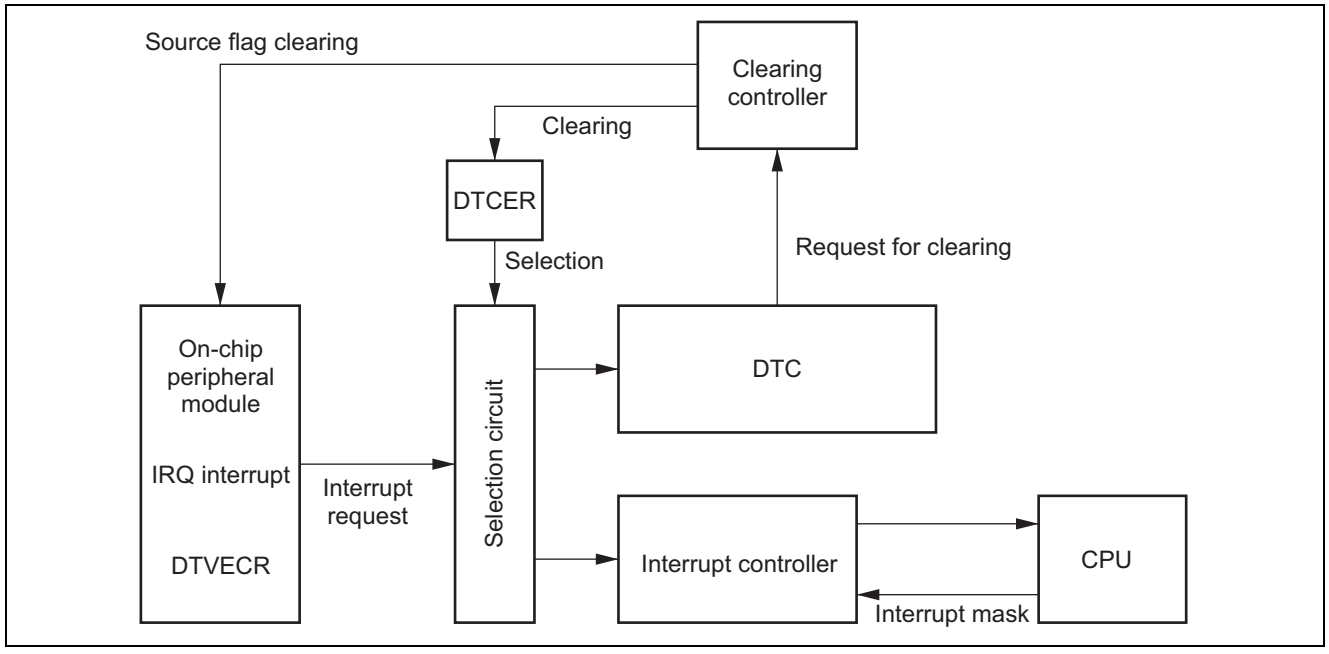


Figure 8 Block Diagram of DTC Activation Source Control

2.3.2 Location of Register Information and DTC Vector Table

Locate the register information in the on-chip RAM. Register information should be located at the address that is multiple of four. Locating the register information in address space is shown in figure 9. Locate the MRA, SAR, MRB, DAR, CRA, and CRB registers, in that order, from the start address of the register information. In the case of chained transfer, register information should be located in consecutive areas as shown in figure 9 and the register information start address should be located at the corresponding vector address to the activation source. Figure 10 shows correspondences between the DTC vector address and register information. The DTC reads the start address of the register information from the vector address set for each activation source, and then reads the register information from that start address.

Table 4 gives a list of interrupt sources capable of DTC activation, addresses in the vector table, and the corresponding DTCE bits.

When the DTC is activated by software, the vector address is obtained from: H'0400 + (DTVECR[6:0] × 2). For example, if VOFR and DTVECR are H'0000 and H'18 respectively, the vector address is H'0430.

The configuration of the vector address is a 2-byte unit. These two bytes specify the lower bits of the start address. Variable vector addresses can be used by setting VOFR. For details on VOFR settings, see the section on the interrupt controller of the *H8S/20103, H8S/20203, H8S/20223 Group Hardware Manual* (REJ09B0465).

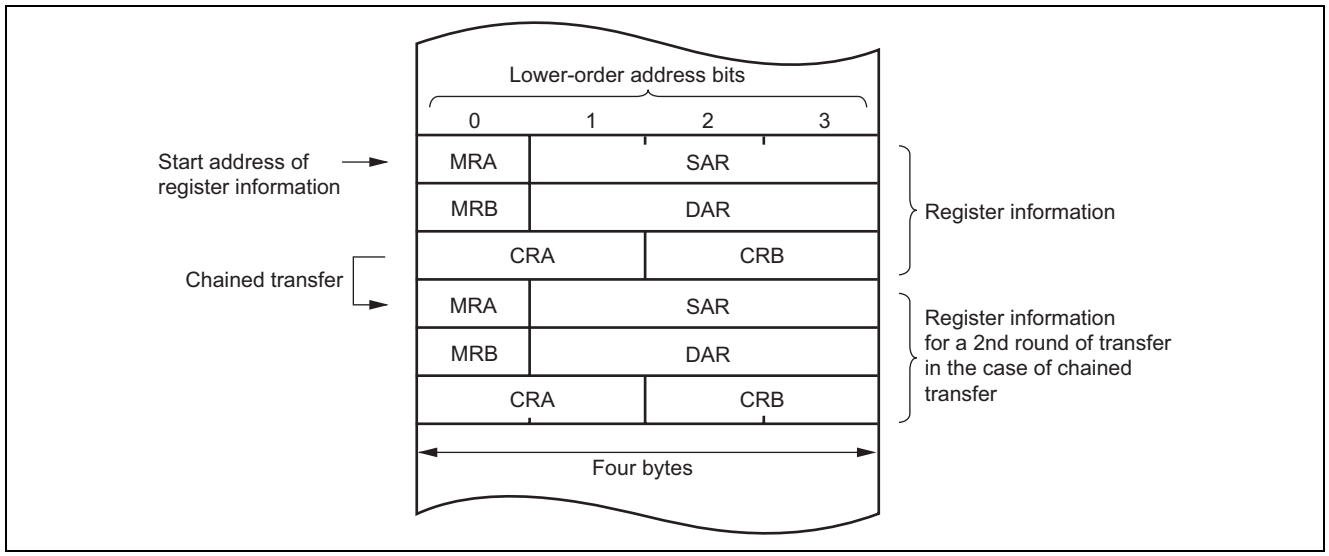


Figure 9 Locating DTC Register Information in Address Space

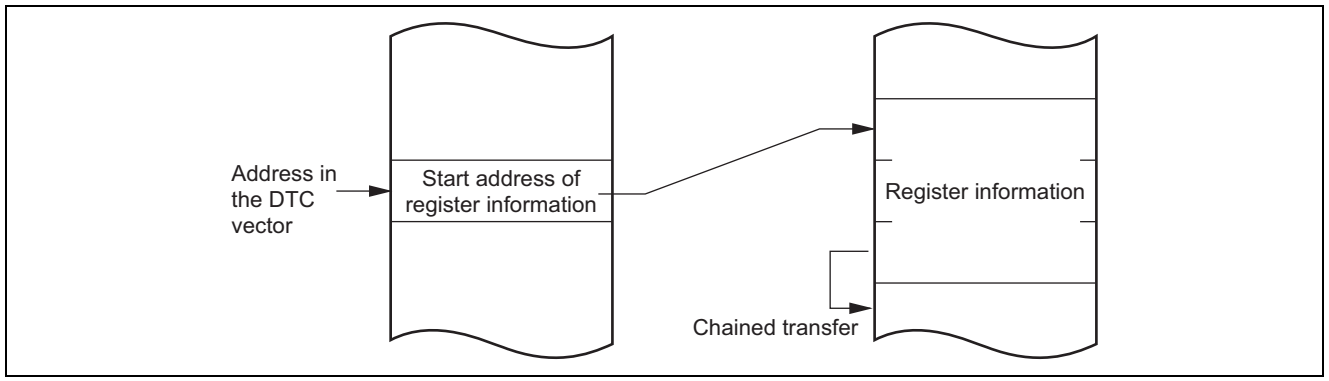


Figure 10 Correspondence between the Address in a DTC Vector and Register Information

Table 4 Interrupt Sources, Addresses of DTC Vectors, and Corresponding DTCE Bits

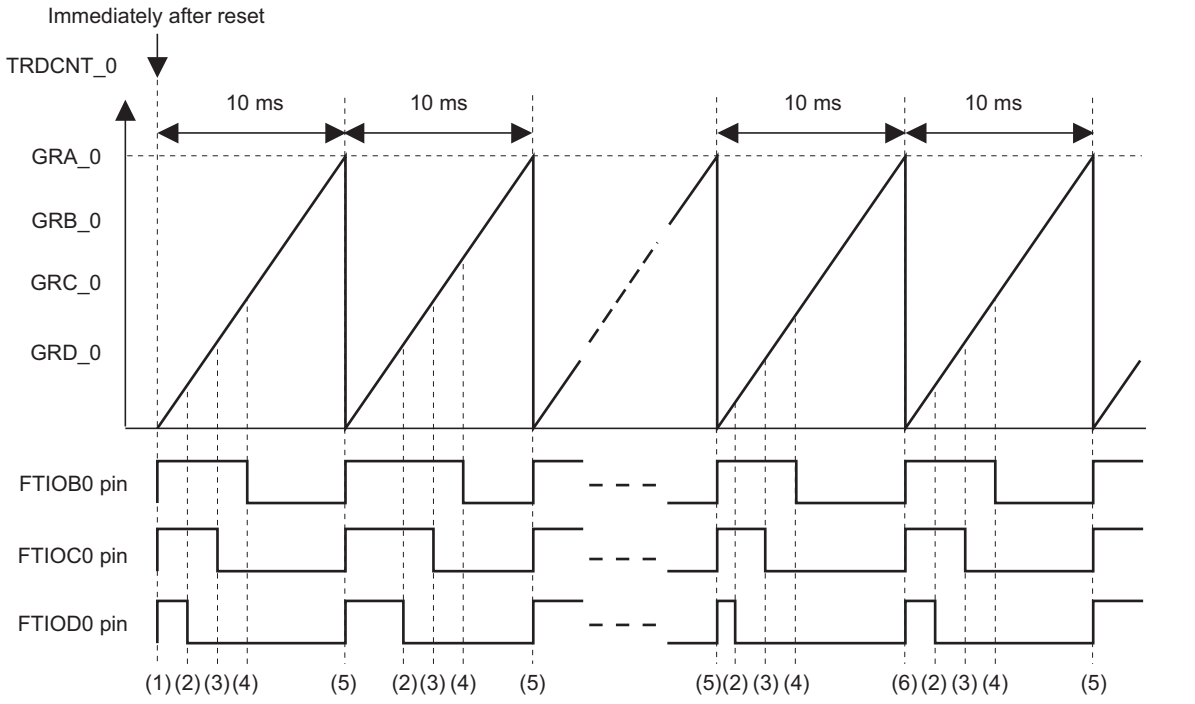
Origin of Activation Source	Activation Source	Vector Number	Address in Vector Table*[1]	DTCE*[5]	Priority
Software	Write to DTVECR	DTVECR	H'0400 + (DTVECR[6:0] × 2)	—	High
External pin	IRQ0	22	H'42C to H'42D	DTCEA7	
	IRQ1	23	H'42E to H'42F	DTCEA6	
	IRQ2	24	H'430 to H'431	DTCEA5	
	IRQ3	25	H'432 to H'433	DTCEA4	
	IRQ4	26	H'434 to H'435	DTCEA3	
	IRQ5	27	H'436 to H'437	DTCEA2	
	IRQ6	28	H'438 to H'439	DTCEA1	
	IRQ7	29	H'43A to H'43B	DTCEA0	
A/D converter unit 1	IADEND_1 (conversion completion)	30	H'43C to H'43D	DTCEB7	
	IADCMP_1 (compare condition match)	31	H'43E to H'43F	DTCEB6	
A/D converter unit 2	IADEND_2 (conversion completion)	32	H'442 to H'443	DTCEB5	
	IADCMP_2 (compare condition match)	33	H'444 to H'445	DTCEB4	
ELC	ELC1FP (ELSR12 event occurrence)	35	H'446 to H'447	DTCEB3	
	ELC2FP (ELSR30 event occurrence)	36	H'448 to H'449	DTCEB2	
SCI3 channel 1	SCI3_1 RXI	38	H'44C to H'44D	DTCEB1	
	SCI3_1 TXI	39	H'44E to H'44F	DTCEB0	
SCI3 channel 2	SCI3_2 RXI	42	H'454 to H'455	DTCEC7	
	SCI3_2 TXI	43	H'456 to H'457	DTCEC6	
SCI3 channel 3	SCI3_3 RXI	46	H'45C to H'45D	DTCEC5	
	SCI3_3 TXI	47	H'45E to H'45F	DTCEC4	
IIC2/SSU	IIC2/SSU_RXI	60	H'478 to H'479	DTCED7	
	IIC3/SSU_TXI	61	H'47A to H'47B	DTCED6	
Timer RC*[3]	ITCMA Input capture A/compare match A	71	H'48E to H'48F	DTCED3	
	ITCMB Input capture B/compare match B	72	H'490 to H'491	DTCED2	
	ITCMC Input capture C/compare match C	73	H'492 to H'493	DTCED1	
	ITCMD Input capture D/compare match D	74	H'494 to H'495	DTCED0	
Timer RD unit 0 channel 0	ITDMA0_0 Input capture A/compare match A	76	H'498 to H'499	DTCEE7	
	ITDMB0_0 Input capture B/compare match B	77	H'49A to H'49B	DTCEE6	
	ITDMC0_0 Input capture C/compare match C	78	H'49C to H'49D	DTCEE5	
	ITDMD0_0 Input capture D/compare match D	79	H'49E to H'49F	DTCEE4	Low

Origin of Activation Source	Activation Source	Vector Number	Address in Vector Table*[1]	DTCE*[5]	Priority
Timer RD unit 0 channel 1*[4]	ITDMA0_1 Input capture A/compare match A	82	H'4A4 to H'4A5	DTCEE3	High
	ITDMB0_1 Input capture B/compare match B	83	H'4A6 to H'4A7	DTCEE2	
	ITDMC0_1 Input capture C/compare match C	84	H'4A8 to H'4A9	DTCEE1	
	ITDMD0_1 Input capture D/compare match D	85	H'4AA to H'4AB	DTCEE0	
Timer RD unit 1 channel 2*[4]	ITDMA1_2 Input capture A/compare match A	87	H'4AE to H'4AF	DTCEF7	
	ITDMB1_2 Input capture B/compare match B	88	H'4B0 to H'4B1	DTCEF6	
	ITDMC1_2 Input capture C/compare match C	89	H'4B2 to H'4B3	DTCEF5	
	ITDMD1_2 Input capture D/compare match D	90	H'4B4 to H'4B5	DTCEF4	
Timer RD unit 1 channel 3*[4]	ITDMA1_3 Input capture A/compare match A	93	H'4BA to H'4BB	DTCEF3	
	ITDMB1_3 Input capture B/compare match B	94	H'4BC to H'4BD	DTCEF2	
	ITDMC1_3 Input capture C/compare match C	95	H'4BE to H'4BF	DTCEF1	
	ITDMD1_3 Input capture D/compare match D	96	H'4C0 to H'4C1	DTCEF0	
Timer RE	ITESC	100	H'4C8 to H'4C9	DTCEG4	
	ITEMI	101	H'4CA to H'4CB	DTCEG3	
	ITEHR	102	H'4CC to H'4CD	DTCEG2	
	ITEDY	103	H'4CE to H'4CF	DTCEG1	
	ITEWK	104	H'4D0 to H'4D1	DTCEG0	
Timer RG	ITGMA Input capture A/compare match A	109	H'4DA to H'4DB	DTCEH3	
	ITGMB Input capture B/compare match B	110	H'4DC to H'4DD	DTCEH2	Low

Notes: 1. "Address in vector table" indicates the 11 lower-order bits of the address in the vector table when VOFR = H'0000.
2. Supported only in the H8S/20223 Group and reserved in other products.
3. Supported only in the H8S/20103 Group and reserved in other products.
4. Not supported in the H8S/20103 Group and reserved in other products.
5. The DTCE bits with no corresponding interrupt are reserved. The write value should always be 0.

3. Principle of Operation

Figure 11 shows the principle of operation in this sample task. The DTC is activated on compare-matches of timer RD by means of the hardware and software processing described in figure 11. Every time the compare match A signal from timer RD_0 channel 0 is generated, GRB_0, GRC_0, and GRD_0 are updated to change the timing for the output of PWM waveforms on pins FTIOB0, FTIOC0, and FTIOD0. Figure 12 shows how the DTC operates in this sample task.



(1)
Hardware processing
(a) Starts counting up by TRDCNT_0
Software processing
Initial settings (a) Timer RD_0, channel 0 (b) DTC (c) Event linkage (d) Setting to start TRDCNT_0 (e) Setting to enable interrupts

(2)
Hardware processing
(a) Outputs the low level on the FTIOD0 pin on a match between TRDCNT_0 and GRD_0

(3)
Hardware processing
(a) Outputs the low level on the FTIOC0 pin on a match between TRDCNT_0 and GRC_0

(5)
Hardware processing
(a) Clears TRDCNT_0 to H'0000 on a match between TRDCNT_0 and GRA_0 (b) Outputs the high level on pins FTIOB0, FTIOC0 and FTIOD0 (c) Activates the DTC to update GRB_0, GRC_0, and GRD_0

(4)
Hardware processing
(a) Outputs the low level on the FTIOB0 pin on a match between TRDCNT_0 and GRB_0

(6)
Hardware processing
(a) Clears TRDCNT_0 to H'0000 on a match between TRDCNT_0 and GRA_0 (b) Outputs the high level on pins FTIOB0, FTIOC0 and FTIOD0 (c) Updates GRB_0, GRC_0 and GRD_0 by DTC activation
Software processing
Handler for the transfer end interrupt for the specified data (a) Resetting of DTC

Figure 11 Principle of Operation in the Sample Task

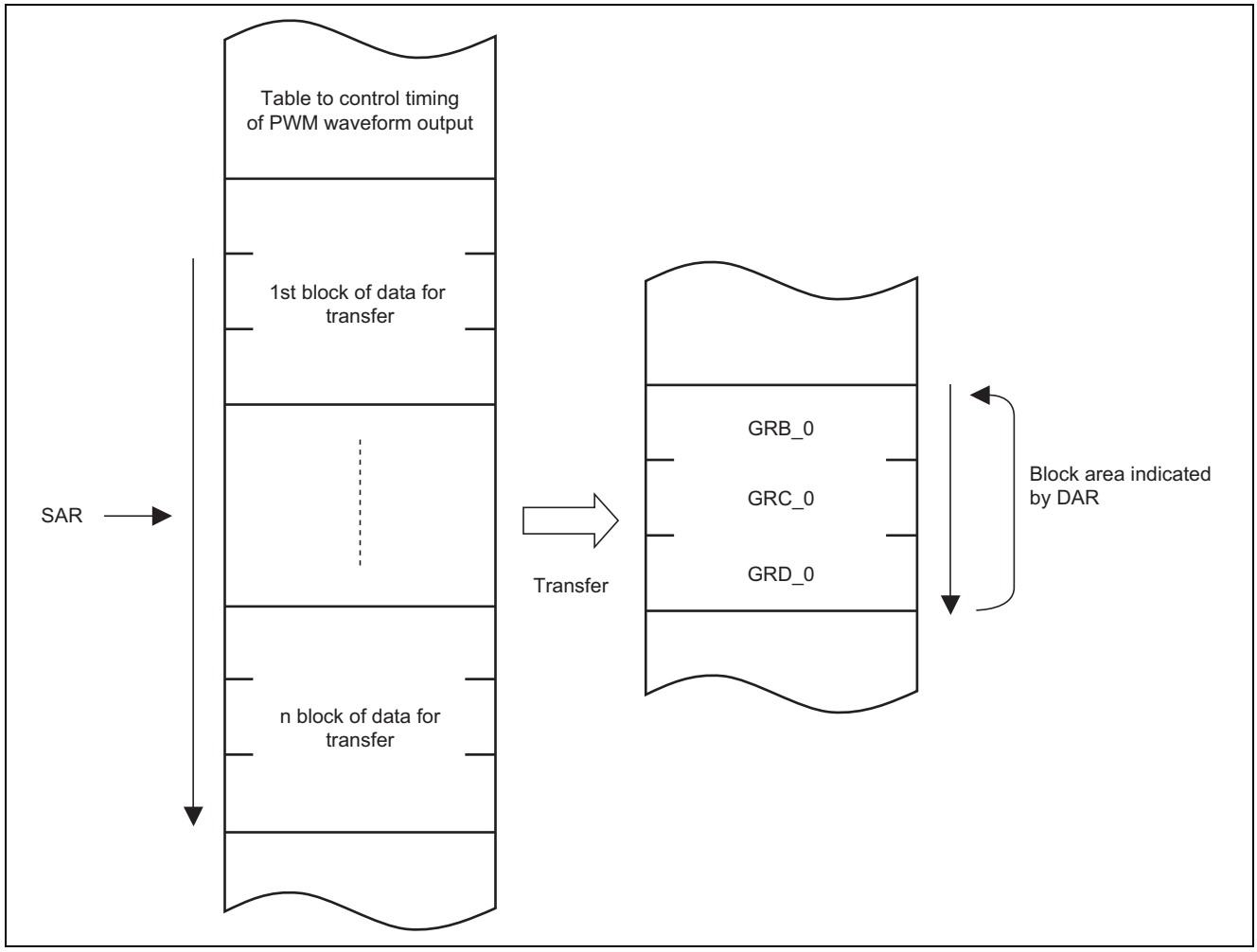


Figure 12 DTC Operation in the Sample Task

4. Description of Software

4.1 Description of Functions

The functions in this sample task are listed and described in table 5.

Table 5 Description of Functions

Function Name	Label Name	Description
Main routine	main	Calls various other functions, starts counting by timer RD_0 channel 0, and enables interrupts and output on pins FTIOD0 to FTIOB0.
System initialization routine	h8s_sysinit	Makes settings for module standby, system clock and bus-master operating clock, and halts the WDT.
Timer RD setting routine	init_tmrd	Makes settings for timer RD_0 and channel 0.
DTC setting routine	init_dtc	Makes DTC and ELC settings.
ELSR30 event interrupt routine	INT_ELC2FP_ELC	Clears interrupt request flags and resets the DTC.

4.2 Description of Argument

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 6 gives descriptions of how internal registers are used in this sample task.

Table 6 Description of Internal Registers

Register Name	Symbol	Description	Address	Setting
PMR6	PMR63	The P63 pin is set to operate as the FTIOD0 pin.	H'FF0005	1
	PMR62	The P62 pin is set to operate as the FTIOC0 pin.		1
	PMR61	The P61 pin is set to operate as the FTIOB0 pin.		1
PMRJ	PMRJ[1:0]	The OSC1 and OSC2 functions are selected for pins PJ0/OSC1 and PJ1/OSC2.	H'FF000C	B'11
ELCSR	ELIE2	The ELF2 interrupt is enabled.	H'FF0528	1
	ELF2	The ELSR30 event flag is cleared.		0
DTCERB	ELC2FP	The ELSR30 event interrupt source is selected as the source for DTC activation.	H'FF0535	1
DTVECR	DTVEC6 to DTVEC0	DTC activation vector numbers are specified.	H'FF053D	B'0000000
ELSR30		Settings are made to link DTC activation with the compare match A signal from channel 0 of timer RD_0.	H'FF069E	H'09
ELCR	ELCON	Linkage of all the events are enabled.	H'FF06BC	1
SYSCCR	PHIHSEL	ϕosc is selected for clock source ϕhigh.	H'FF06D0	1
LPCR1	PSCSTP	PSC divider runs.	H'FF06D1	0
	PHIBSEL	ϕhigh is selected for clock source ϕbase.		1
LPCR2	PHI[2:0]	ϕbase is selected for system clock ϕ.	H'FF06D2	B'000
LPCR3	PHIS[2:0]	ϕ is selected for bus master operation clock ϕs.	H'FF06D3	B'000
OSCCSR		Setting is made for period of timer ϕosc oscillation settling time.	H'FF06D5	H'0E
TMWD		Clock input to WDT is prohibited.	H'FFFF99	H'F7
TCSRWD		Writing to TMWD is controlled.	H'FFFF9A	H'A3
TRDCNT_0		TRDCNT_0 is initialized.	H'FFFFB0	H'0000
GRA_0		The period of timer RD_0, channel 0, (PWM cycle) is specified.	H'FFFFB2	H'C34F
GRB_0		Output timing of waveforms on the FTIOB0 pin is specified.	H'FFFFB4	H'3A97
GRC_0		Output timing of waveforms on the FTIOC0 pin is specified.	H'FFFFB6	H'270F
GRD_0		Output timing of waveforms on the FTIOD0 pin is specified.	H'FFFFB8	H'1387
TRDCR	CCLR[2:0]	TRDCNT is cleared by compare match with GRA_0.	H'FFFFC4	B'001
	CKEG[1:0]	Counting of rising edges.		B'00
	TPSC[2:0]	Internal clock: count by ϕ/4.		B'010
POCR	POLD	Active-low output is selected for the FTIOD0 pin. With the setting of the TOD0 bit in TRDOCR, "H" is selected as the initial output level on the FTIOD0 pin.	H'FFFFC9	0
	POLC	Active-low output is selected for the FTIOC0 pin. With the setting of the TOC0 bit in TRDOCR, "H" is selected as the initial output level on the FTIOC0 pin.		0

Register Name	Symbol	Description	Address	Setting
POCR	POLB	Active-low output is selected for the FTIOB0 pin. With the setting of the TOB0 bit in TRDOCR, "H" is selected as the initial output level on the FTIOB0 pin.	H'FFFFC9	0
TRDSTR	CSTPN0	Counting proceeds on a compare match of TRDCNT_0 and GRA_0.	H'FFFFD2	1
	STR0	Counting by TRDCNT_0 proceeds.		1
TRDPMR	PWMD0	FTIOD0 is in PWM mode.	H'FFFFD4	1
	PWMC0	FTIOC0 is in PWM mode.		1
	PWMB0	FTIOB0 is in PWM mode.		1
TRDOER1	ED0	Output on the FTIOD0 pin in accord with the settings of TRDPMR, TRDFCR and TRDIORC_0 is enabled.	H'FFFFD6	0
	EC0	Output on the FTIOC0 pin in accord with the settings of TRDPMR, TRDFCR and TRDIORC_0 is enabled.		0
	EB0	Output on the FTIOB0 pin in accord with the settings of TRDPMR, TRDFCR and TRDIORA_0 is enabled.		0
TRDOCR	TOD0	With the setting of the POLD bit in POCR, "H" is selected as the initial output level on the FTIOD0 pin.	H'FFFFD8	0
	TOC0	With the setting of the POLC bit in POCR, "H" is selected as the initial output level on the FTIOC0 pin.		0
	TOB0	With the setting of the POLB bit in POCR, "H" is selected as the initial output level on the FTIOB0 pin.		0
MSTCR1	MSTWDT	The WDT is released from module standby.	H'FFFFDC	0
	MSTDTC	The DTC is released from module standby.		0
MSTCR3	MSTTMRD1	Timer RD unit 0 is released from module standby.	H'FFFFDE	0
MRA*	SM[1:0]	The SAR is incremented after transfer.	H'FFDF80	B'10
	DM[1:0]	The DAR is incremented after transfer.		B'10
	MD[1:0]	The DTC is placed in block transfer mode.		B'10
	DTS	Destination side is specified as a block area.		0
	Sz	Word-size transfer		1
SAR*		Transfer source address is specified.	H'FFDF81	H'0009F6
MRB*	CHNE	Setting is made so that transfer is not chained.	H'FFDF84	0
	DISEL	Setting is made so that an interrupt request for the CPU is only generated when the specified data transfer is completed.		0
DAR*		Transfer destination address is specified.	H'FFDF85	H'FFFFB4
CRAH*		Number of unit transfers is specified.	H'FFDF88	3
CRAL*		Transfer counter	H'FFDF89	3
CRB*		Number of unit transfers of block data by the DTC is specified.	H'FFDF8A	12

Note: * Information for the DTC registers is located in RAM.

4.4 RAM Usage

No RAM is used in this sample task (information for the DTC registers is also located in RAM).

4.5 Description of Definitions in Use

Table 7 gives a description of the definitions used in this sample task.

Table 7 Description of Definition in Use

Label Name	Description	Constant
GR_10MS	With division by four at ϕ = 20 MHz, 10 ms	H'C34F
GR_9MS	With division by four at ϕ = 20 MHz, 9 ms	H'AFC7
GR_8MS	With division by four at ϕ = 20 MHz, 8 ms	H'9C3F
GR_7MS	With division by four at ϕ = 20 MHz, 7 ms	H'88B7
GR_6MS	With division by four at ϕ = 20 MHz, 6 ms	H'752F
GR_5MS	With division by four at ϕ = 20 MHz, 5 ms	H'61A7
GR_4MS	With division by four at ϕ = 20 MHz, 4 ms	H'4E1F
GR_3MS	With division by four at ϕ = 20 MHz, 3 ms	H'3A97
GR_2MS	With division by four at ϕ = 20 MHz, 2 ms	H'270F
GR_1MS	With division by four at ϕ = 20 MHz, 1 ms	H'1387
BLK_SIZE	Size of block for transfer (in word units)	3
BLK_SIZE_CNT	Number of blocks to be transferred (value for counting)	3
TRANSFER_CNT	Number of times blocks are to be transferred	12
PWM_CHANGE_NUM	Size in words of table for PWM output timing	36

4.6 Description of Constants

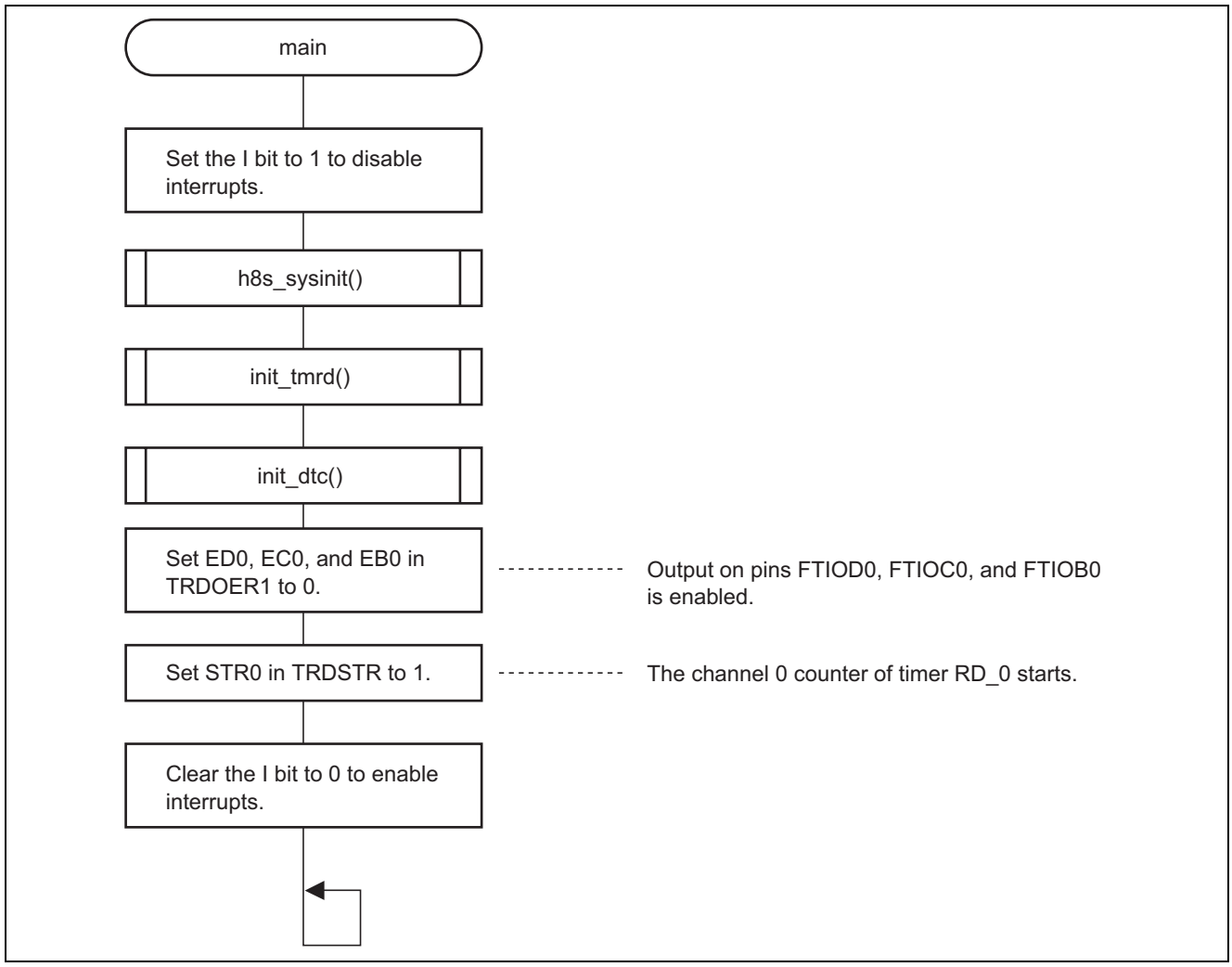
Table 8 gives description of the constants used in this sample task.

Table 8 Description of Constants

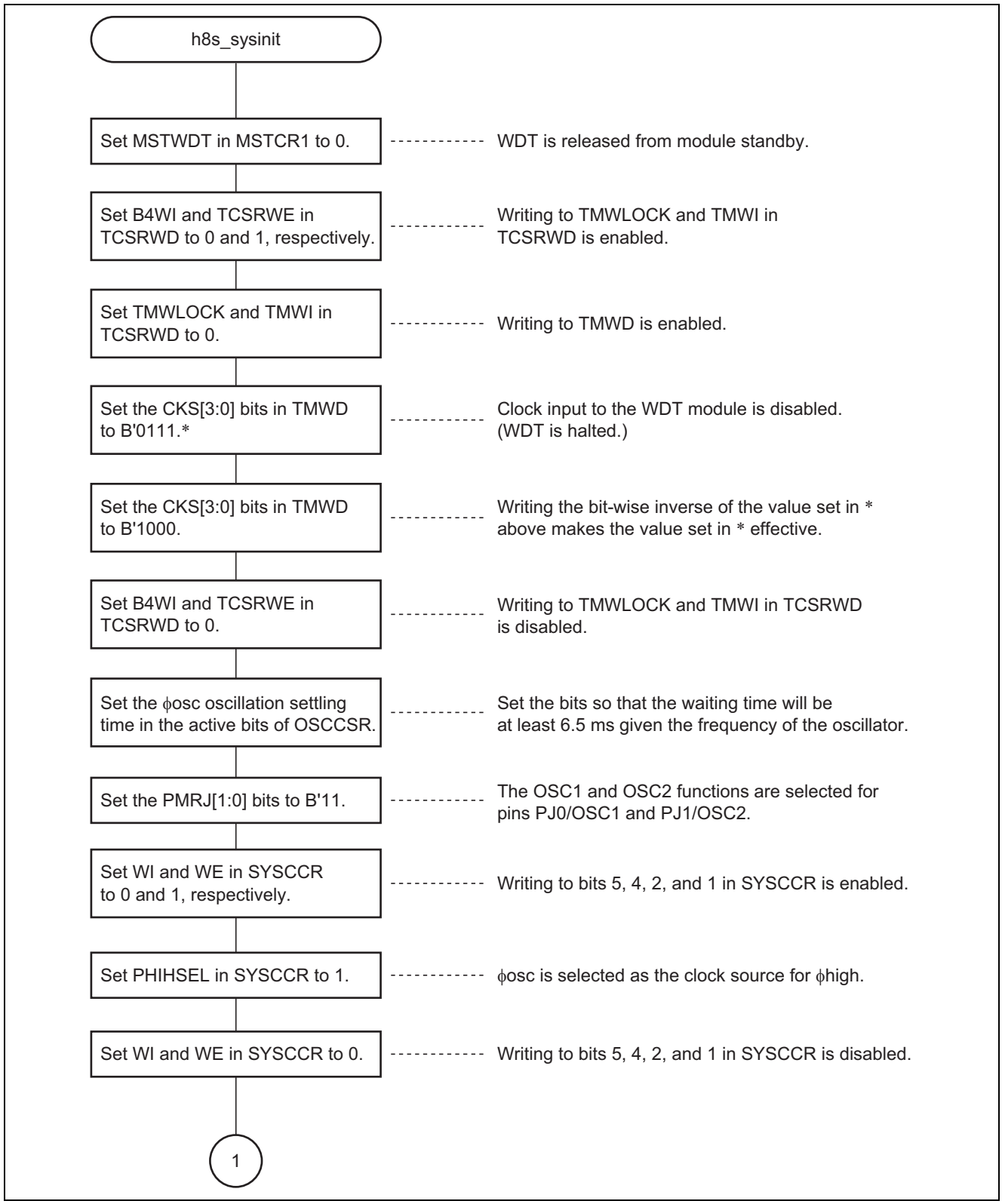
Label Name	Description	Address	Constant
dtcvect_tbl[ ]	The address where the DTC register information starts is specified as the address corresponding to the activation source within the DTC vector table.	H'000448	H'DF80
TMRD_PWM_TBL[0] to TMRD_PWM_TBL[35]	Table of output timing for pins FTIOB0, FTIOC0, and FTIOD0	H'0009FA	(FTIOB) (FTIOC) (FTIOD) GR_4MS, GR_3MS, GR_2MS
		H'000A00	GR_5MS, GR_4MS, GR_3MS
		H'000A06	GR_6MS, GR_5MS, GR_4MS
		H'000A0C	GR_7MS, GR_6MS, GR_5MS
		H'000A12	GR_8MS, GR_7MS, GR_6MS
		H'000A18	GR_9MS, GR_8MS, GR_7MS
		H'000A1E	GR_8MS, GR_7MS, GR_6MS
		H'000A24	GR_7MS, GR_6MS, GR_5MS
		H'000A2A	GR_6MS, GR_5MS, GR_4MS
		H'000A30	GR_5MS, GR_4MS, GR_3MS
		H'000A36	GR_4MS, GR_3MS, GR_2MS
		H'000A3C	GR_3MS, GR_2MS, GR_1MS

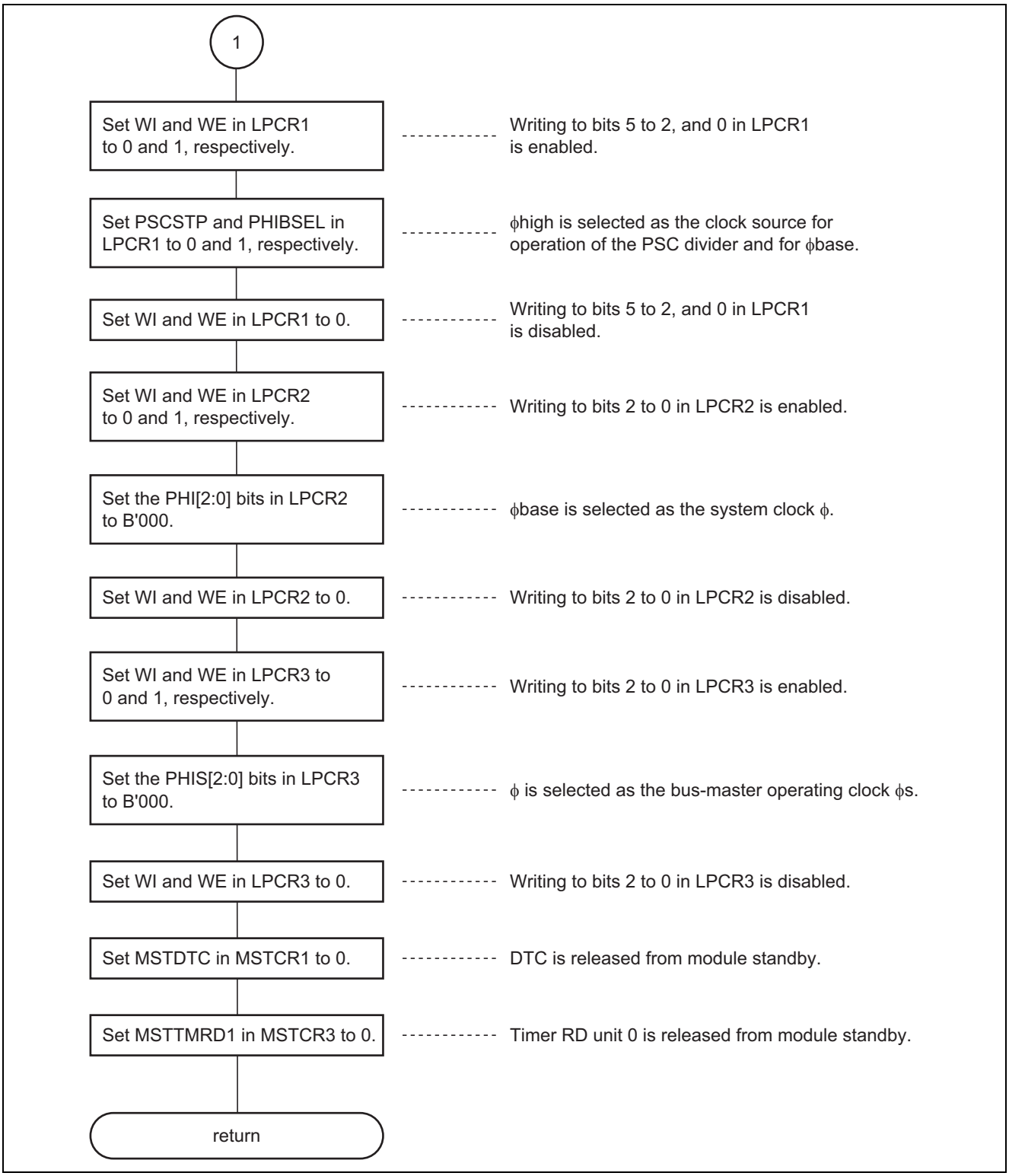
5. Flowcharts

5.1 Main Routine

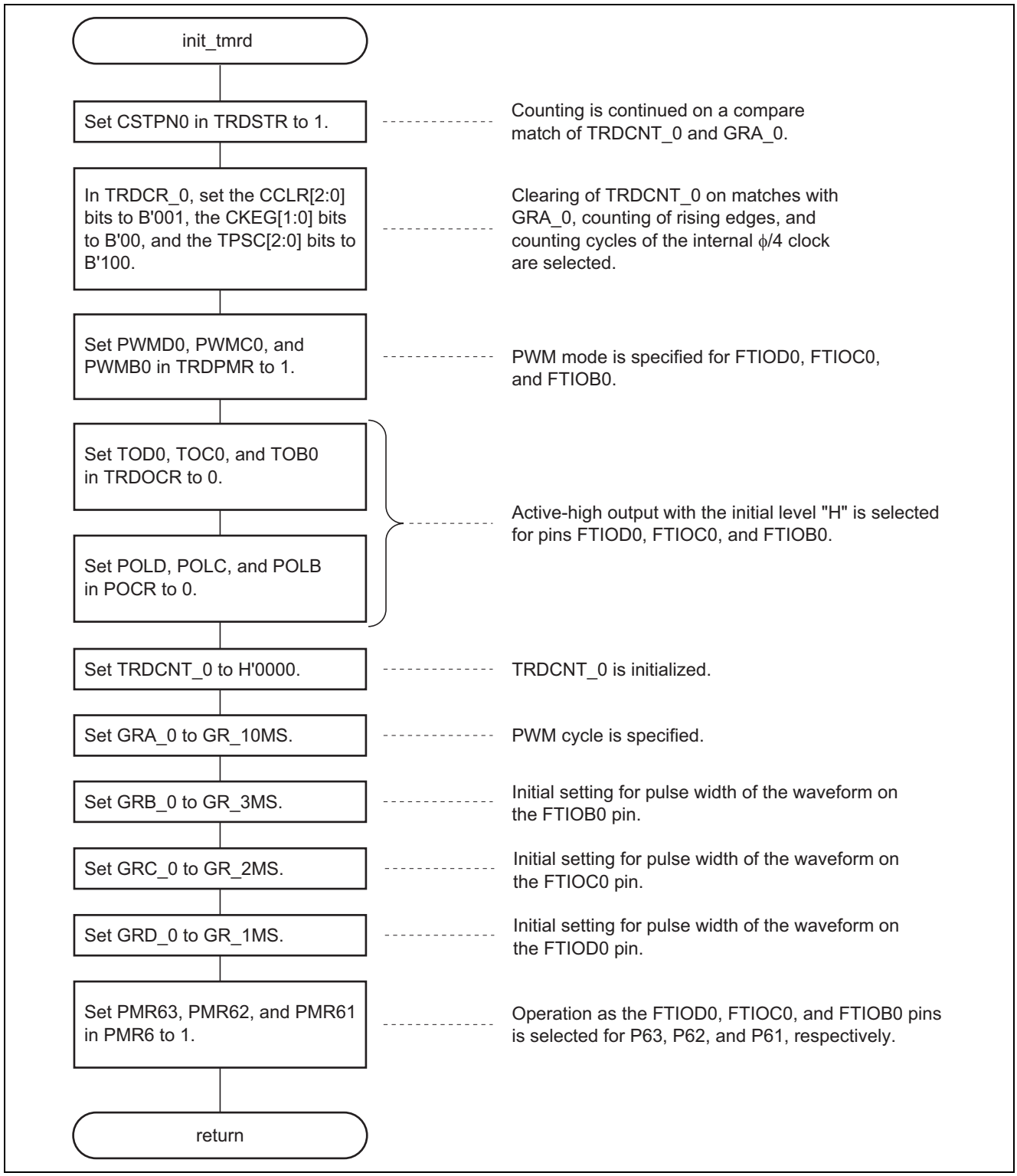


5.2 System Initialization Routine

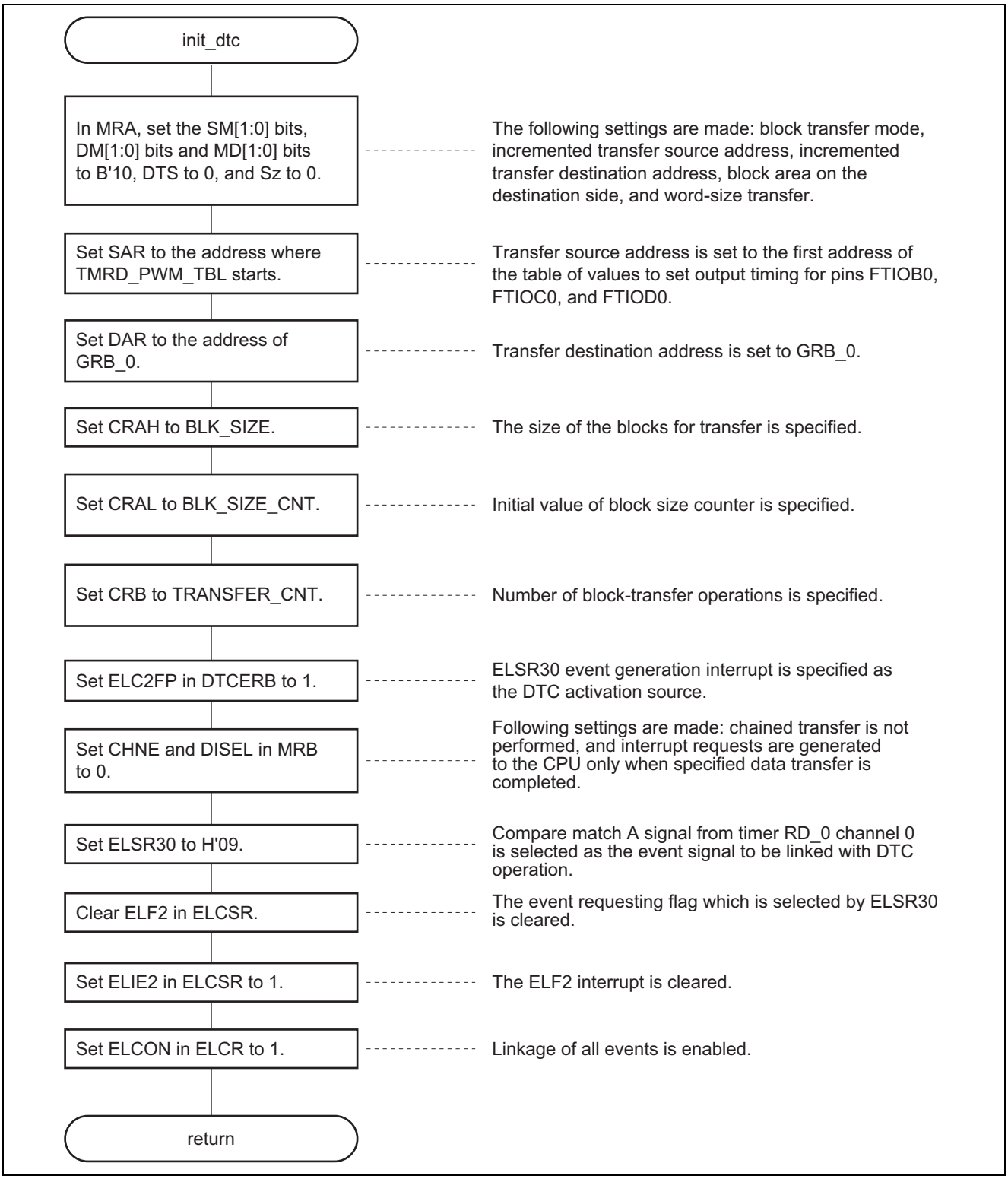



1
Set WI and WE in LPCR1 to 0 and 1, respectively.
Writing to bits 5 to 2, and 0 in LPCR1 is enabled.
Set PSCSTP and PHIBSEL in LPCR1 to 0 and 1, respectively.
ϕhigh is selected as the clock source for operation of the PSC divider and for ϕbase.
Set WI and WE in LPCR1 to 0.
Writing to bits 5 to 2, and 0 in LPCR1 is disabled.
Set WI and WE in LPCR2 to 0 and 1, respectively.
Writing to bits 2 to 0 in LPCR2 is enabled.
Set the PHI[2:0] bits in LPCR2 to B'000.
ϕbase is selected as the system clock ϕ.
Set WI and WE in LPCR2 to 0.
Writing to bits 2 to 0 in LPCR2 is disabled.
Set WI and WE in LPCR3 to 0 and 1, respectively.
Writing to bits 2 to 0 in LPCR3 is enabled.
Set the PHIS[2:0] bits in LPCR3 to B'000.
ϕ is selected as the bus-master operating clock ϕs.
Set WI and WE in LPCR3 to 0.
Writing to bits 2 to 0 in LPCR3 is disabled.
Set MSTDTC in MSTCR1 to 0.
DTC is released from module standby.
Set MSTTMRD1 in MSTCR3 to 0.
Timer RD unit 0 is released from module standby.
return

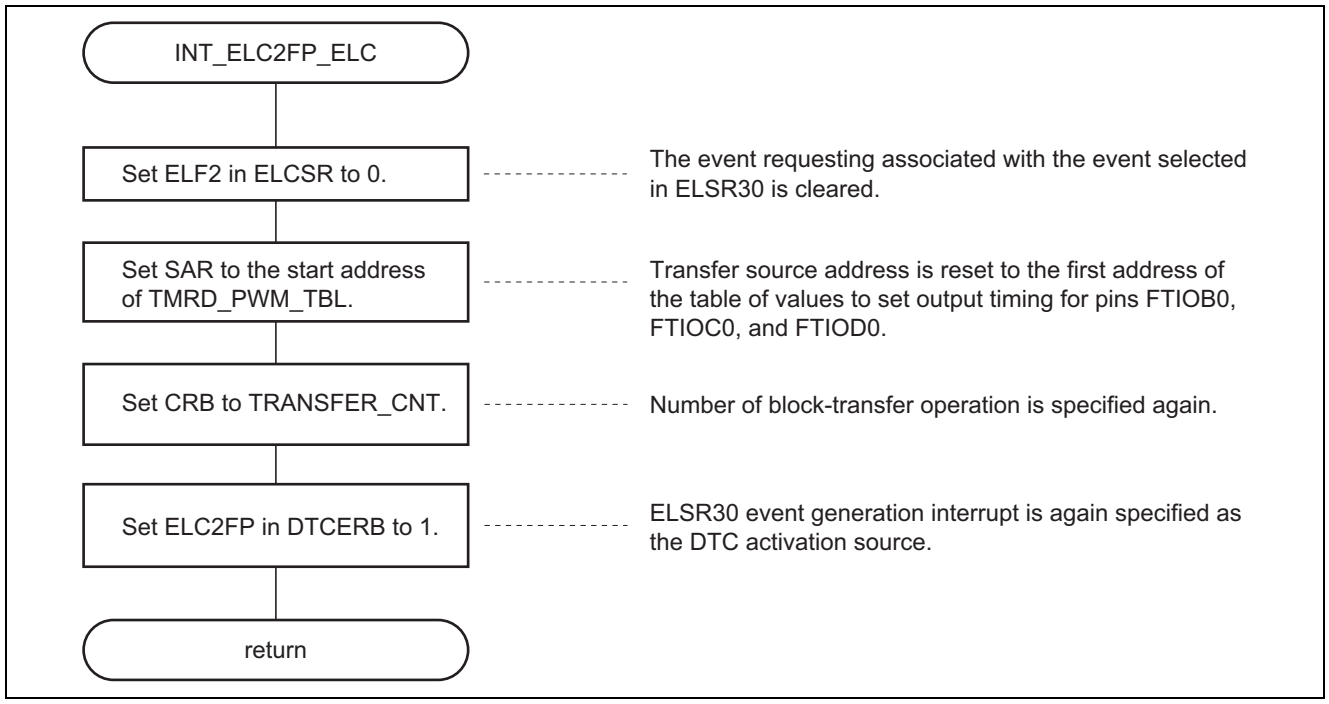
5.3 Timer RD Setting Routine



5.4 DTC Setting Routine



5.5 ELSR30 Event Generation Interrupt Routine



6. Program Listing

```
<trd_dtc.c>
/************************************************************************/
/*  H8S/2000 Tiny Series -H8S/20203-                                    */
/*  Application Note                                                    */
/*                                                                      */
/* start DTC by Timer RD unit0 channel 0                                */
/*                                                                      */
/*  Function                                                            */
/*  : start DTC by Timer RD unit0 channel 0 compare match A             */
/*  Event Link DTC and Timer RD unit0 channel 0                         */
/*                                                                      */
/*  External Clock : 20 MHz                                             */
/*  Internal Clock : 20 MHz                                             */
/************************************************************************/
#include <machine.h>
#include "iodefine.h"

typedef struct
{
    union{
            unsigned char          MRA;                    /* DTC mode register A */
            struct{
                    unsigned long          dummy1:8;       /* dummy1 data (MRA address) */
                    unsigned long          SAR:24;         /* DTC source address register */
            }SAR;
    }UN_MRA_SAR;
    union{
            unsigned char          MRB;                    /* DTC mode register B */
            struct{
                    unsigned long          dummy2:8;       /* dummy2 data (DAR address) */
                    unsigned long          DAR:24;         /* DTC destination address register */
            }DAR;
    }UN_MRB_DAR;
    union{
            unsigned short         CRA;                    /* DTC transfer count register A */
            struct{
                    unsigned char          CRAH;           /* DTC transfer count register BH */
                    unsigned char          CRAL;           /* DTC transfer count register BL */
            }CHAR;
    }UN_CRA;
    union{
            unsigned short         CRB;                    /* DTC transfer count register B */
            struct{
                    unsigned char          CRBH;           /* DTC transfer count register BH */
                    unsigned char          CRBL;           /* DTC transfer count register BL */
            }CHAR;
    }UN_CRB;
} st_dtc_reg;
```

```
/******************************************************/
/* Definition of const data                           */
/******************************************************/
/* Timer RD */
/* unit1 (Phi = 20 MHz, divide 4) */
#define GR_10MS            0xC34F         /* Set 10 ms */
#define GR_9MS             0xAFC7         /* Set 9 ms */
#define GR_8MS             0x9C3F         /* Set 8 ms */
#define GR_7MS             0x88B7         /* Set 7 ms */
#define GR_6MS             0x752F         /* Set 6 ms */
#define GR_5MS             0x61A7         /* Set 5 ms */
#define GR_4MS             0x4E1F         /* Set 4 ms */
#define GR_3MS             0x3A97         /* Set 3 ms */
#define GR_2MS             0x270F         /* Set 2 ms */
#define GR_1MS             0x1387         /* Set 1 ms */

/* DTC */
#define BLK_SIZE              3           /* block transfer size */
#define BLK_SIZE_CNT          3           /* block size counter */
#define TRANSFER_CNT          12          /* transfer counter */

#define PWM_CHANGE_NUM        36          /* number of pwm change timing */

#pragma section
/******************************************************/
/* Declaration of function prototype                  */
/******************************************************/
void main(void);
void init_dtc(void);
void init_tmrd(void);
void h8s_sysinit(void);

/******************************************************/
/* Definition of Const area                           */
/******************************************************/
const unsigned short TMRD_PWM_TBL[PWM_CHANGE_NUM]={
    GR_4MS, GR_3MS, GR_2MS,           /* GRB_0, GRC_0, GRD_0 */
    GR_5MS, GR_4MS, GR_3MS,           /* GRB_0, GRC_0, GRD_0 */
    GR_6MS, GR_5MS, GR_4MS,           /* GRB_0, GRC_0, GRD_0 */
    GR_7MS, GR_6MS, GR_5MS,           /* GRB_0, GRC_0, GRD_0 */
    GR_8MS, GR_7MS, GR_6MS,           /* GRB_0, GRC_0, GRD_0 */
    GR_9MS, GR_8MS, GR_7MS,           /* GRB_0, GRC_0, GRD_0 */
    GR_8MS, GR_7MS, GR_6MS,           /* GRB_0, GRC_0, GRD_0 */
    GR_7MS, GR_6MS, GR_5MS,           /* GRB_0, GRC_0, GRD_0 */
    GR_6MS, GR_5MS, GR_4MS,           /* GRB_0, GRC_0, GRD_0 */
    GR_5MS, GR_4MS, GR_3MS,           /* GRB_0, GRC_0, GRD_0 */
    GR_4MS, GR_3MS, GR_2MS,           /* GRB_0, GRC_0, GRD_0 */
    GR_3MS, GR_2MS, GR_1MS            /* GRB_0, GRC_0, GRD_0 */
};
```

```
/******************************************************/
/* Definition of RAM area                             */
/******************************************************/
#pragma section DTC
st_dtc_reg DTC_REG;                  /* DTC register */

#pragma section
/******************************************************/
/* Name:        main                                  */
/* Parameters:  None                                  */
/* Returns:     None                                  */
/* Description: User main                             */
/******************************************************/
void main(void)
{
    set_ccr(0x80);                /* set CCR-Ibit */

    h8s_sysinit();                /* initialize system */

    init_tmrd();                  /* initialize timer RD */

    init_dtc();                   /* initialize DTC */

    TRD01.TRDOER1.BYTE = 0xF1;    /* FTIOD0-FTIOB0 output enable */
    TRD01.TRDSTR.BYTE = 0xFD;     /* start timer RD unit0 channel 0 */

    set_imask_ccr(0);             /* interrupt enable */

    while(1);
}

/******************************************************/
/* Name:        init_tmrd                             */
/* Parameters:  None                                  */
/* Returns:     None                                  */
/* Description: initialize timer RD                  */
/******************************************************/
void init_tmrd(void)
{
    /* unit 1 */
    TRD01.TRDSTR.BYTE = 0xFC;     /* continue count when TRDCNT_0 compare match GRA_0, TRDCNT_0 stop */
    TRD0.TRDCR.BYTE = 0x22;       /* clear TRDCNT_0 when compare match GRA_0 */
                                  /* select clock Phi/4 */
    TRD01.TRDPMR.BYTE = 0x8F;     /* PWM mode FTIOB0, FTIOC0, FTIOD0 */
    TRD01.TRDOCR.BYTE = 0x00;     /* FTIOB0, FTIOC0, FTIOD0 initialize output "L" */
    TRD0.POCR.BYTE = 0xF8;        /* FTIOB0, FTIOC0, FTIOD0 "L" active */

    TRD0.GRA = GR_10MS;           /* set GRA_0 */
    TRD0.GRB = GR_3MS;            /* set GRB_0 */
    TRD0.GRC = GR_2MS;            /* set GRC_0 */
    TRD0.GRD = GR_1MS;            /* set GRD_0 */
    TRD0.TRDCNT = 0x0000;         /* clear TRDCNT_0 */

    PMR6.BYTE |= 0x0E;            /* P63-P61=>FTIOD0-FTIOB0 */
}
```

```
/*****************************************************/
/* Name:        init_dtc                             */
/* Parameters:  None                                 */
/* Returns:     None                                 */
/* Description: initialize DTC                       */
/*****************************************************/
void init_dtc(void)
{
    DTC_REG.UN_MRA_SAR.MRA = 0xA9;    /* block transfer mode, SAR increment, DAR increment */
                                      /* transfer word size, block area -> destination address */

    DTC_REG.UN_MRA_SAR.SAR.SAR = (unsigned long)TMRD_PWM_TBL;     /* Forwarding former address */
    DTC_REG.UN_MRB_DAR.DAR.DAR = (unsigned long)&TRD0.GRB;        /* Address at forwarding destination */
    DTC_REG.UN_CRA.CHAR.CRAH = BLK_SIZE;              /* Set block transfer size */
    DTC_REG.UN_CRA.CHAR.CRAL = BLK_SIZE_CNT;          /* Set block size counter */
    DTC_REG.UN_CRB.CRB = TRANSFER_CNT;                /* Set transfer counter */

    DTC.DTCERB.BIT.ELC2FP = 1;                        /* DTC start by ELSR30 event */
    DTC_REG.UN_MRB_DAR.MRB = 0x00;                    /* disable chain, interrupt transfer end */

    /* Set event link, Timer RD unitr0 channel 0 compare match A */
    ELC.ELSR30.BYTE = 0x09;
    INTC.ELCSR.BYTE &= ~0xF2;                         /* clear ELF2 */
    INTC.ELCSR.BIT.ELIE2 = 1;                         /* ELF2 interrupt enable */
    ELC.ELCR.BIT.ELCON = 1;                           /* event link enable */
}

/*****************************************************/
/* Name:        h8s_sysinit                          */
/* Parameters:  None                                 */
/* Returns:     None                                 */
/* Description: initialize H8S/20203                 */
/*****************************************************/
void h8s_sysinit(void)
{
    MSTCR1.BIT.MSTWDT = 0;                                      /* WDT module standby off */

    /* stop WDT */
    WDT.TCSRWD.BYTE = 0x97;                                     /* write enable TMWLOCK, TMWI */
    WDT.TCSRWD.BYTE = 0xA3;                                     /* write enable TMWD */
    WDT.TMWD.BYTE = 0xF7;                                       /* Not select clock source */
    WDT.TMWD.BYTE = 0xF8;                                       /* write bit inversion */
    WDT.TCSRWD.BYTE = 0x87;                                     /* write disable TMWLOCK, TMWI */

    CPG.OSCCSR.BYTE = 0x0E;                                     /* wait over 6.5 ms, Phi_osc = 20 MHz */
    PMRJ.BYTE = 0x03;                                           /* select OSC1, OSC2 */

    CPG.SYSCCR.BYTE = (CPG.SYSCCR.BYTE & 0x7F)| 0x40;           /* WI = 0, WE = 1 */
    CPG.SYSCCR.BYTE = 0x60;                                     /* high = Phi_osc, Phi_low = Phi_loco */
    CPG.SYSCCR.BYTE = CPG.SYSCCR.BYTE & 0x3F;                   /* WI = 0, WE = 0 */
```

```
    CPG.LPCR1.BYTE = (CPG.LPCR1.BYTE & 0x7F) | 0x40;        /* WI = 0, WE = 1 */
    CPG.LPCR1.BYTE = 0x41;                                  /* PSC on, Phi_base = Phi_high */
    CPG.LPCR1.BYTE = CPG.LPCR1.BYTE & 0x3F;                 /* WI = 0, WE = 0 */

    CPG.LPCR2.BYTE = (CPG.LPCR2.BYTE & 0x7F) | 0x40;        /* WI = 0, WE = 1 */
    CPG.LPCR2.BYTE = 0x40;                                  /* select system clock */
    CPG.LPCR2.BYTE = CPG.LPCR2.BYTE & 0x3F;                 /* WI = 0, WE = 0 */

    CPG.LPCR3.BYTE = (CPG.LPCR3.BYTE & 0x7F) | 0x40;        /* WI = 0, WE = 1 */
    CPG.LPCR3.BYTE = 0x40;                                  /* select clock of bus master */
    CPG.LPCR3.BYTE = CPG.LPCR3.BYTE & 0x3F;                 /* WI = 0, WE = 0 */

    /* module standby off */
    MSTCR1.BIT.MSTDTC = 0;                                  /* DTC module standby off */
    MSTCR3.BIT.MSTTMRD1 = 0;                                /* Timer RD unit0 module standby off */
}
```

6.1 Designation of Linkage Addresses

Section Name	Address
CDTC_VECT	H'000400
PResetPRG, PIntPRG	H'000500
P, C, C$DSEC, C$BSEC, D	H'000800
BDTC, B, R	H'FFDF80
S	H'FFFD80

Website and Support

Renesas Technology Website
http://www.renesas.com/

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
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