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Renesas Electronics Corporation

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H8/300L Super Low Power Series

Using the Auto-Reload Timer Function to Set an Interrupt Period

Introduction

Using the Timer C auto-reload timer function, this function sets the interval of Timer C interrupts (in this example, the interval is 2.048 ms). This function turns on and off the LED connected to the pin for every 250 cycle of interrupts caused by Timer C

Target Device

H8/38024

Contents

1. Specifications

1. Using the Timer C auto-reload timer function, this function generates a Timer C interrupt every 2.048 ms.
2. This function turns on and off the LED connected to P92 for every 250 cycle of interrupts caused by Timer C interrupt handling.
3. The P92 pin is a large-current port.
4. Timer counter C (TCC) is set to down-counter by software control.

2. Description of Functions Used

1. In this sample task, a Timer C interrupt is generated every 2.048 ms using the Timer C auto-reload function.
   a. The block diagram of the Timer C auto-reload function is shown in Figure 1 and is described below.
      - The system clock (ϕ) is a 5-MHz clock obtained by dividing 10-MHz OSC clock by 2 and is a reference clock to operate the CPU and its peripheral functions.
      - The prescaler S (PSS) is a 13-bit counter using ϕ as input and counts up every cycle.
      - Timer Mode Register C (TMC) is an 8-bit read/write register and selects the auto-reload function and input clock, and perform Timer counter C (TCC) up/down-counter control. It can be selected whether TCC up/down control is performed by hardware using UD pin input, or whether TCC functions as an up-counter or a down-counter by software control.
      - Timer Counter C (TCC) is an 8-bit read-only counter. TCC is counted up/down by an internal clock/external event which is input. The input clock can be selected from a total of eight clocks, namely, clocks obtained by dividing the system clock by 8192, 2048, 512, 64, 16 and 4, and subclock/4, and an external clock. In this sample task, TCC is set to down-counter, and the system clock/64 is selected as the input clock of TCC.
      - Timer Load Register C (TLC) is an 8-bit write-only register and sets a reload value for TCC. In this sample task, TLC is set at H'A0 so that TCC underflows every 2.048 ms.
      - Timer C Interrupt Request Flag (IRRTC) is set to 1 when TCC underflows. A Timer C interrupt is accepted and Timer C interrupt handling is started when IRRTC is set to 1, Timer C interrupt enable (IENTC) in Interrupt Enable Register 2 (IENR2) is 1 and I Bit in Condition Code Register (CCR) is cleared to 0.

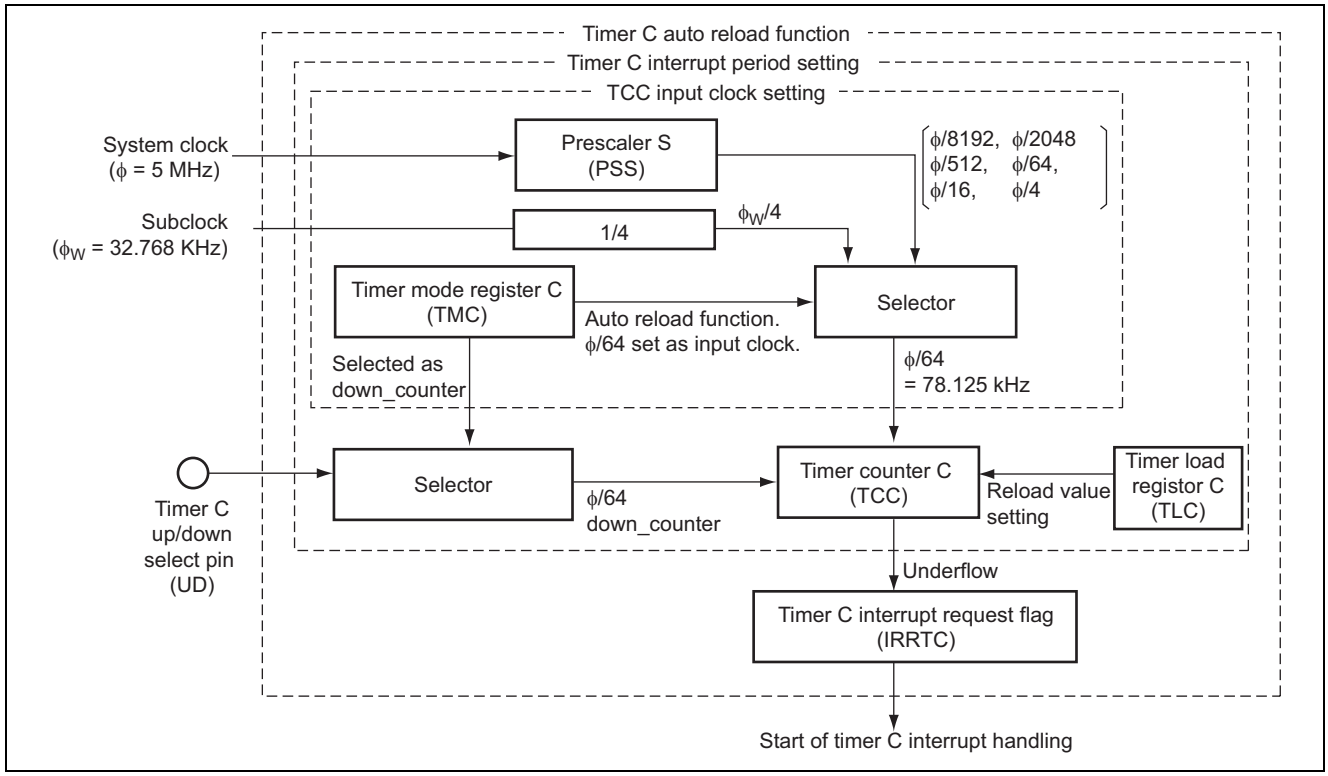


Figure 1 Block Diagram of Timer C Auto-Reload Function

b. The method to set an interrupt period by the Timer C auto-reload function is described below.
An interrupt period of the Timer C auto-reload function is set by the following calculation formula:
Timer C interrupt period (s) = (TCC input clock period (s)) × reload value
By setting the TCC input clock period to TMC and reload set value to TLC, the Timer C interrupt period is set.

2. Table 1 shows function assignment in this sample task. The functions are assigned as shown in table 1 and the interrupt period is set by the Timer C auto-reload function.

Table 1 Assignment of Functions

Function	Assignment
PSS	A 13-bit up-counter using the system clock (5 MHz) as input
TCC	An 8-bit counter using a clock obtained by dividing the system clock by 64 as input
TMC	Sets auto-reload function, sets TCC to down-counter by software control, and sets TCC input clock to ϕ/64
TLC	Sets TCC reload value.
IRRTC	Indicates whether or not a Timer C interrupt is requested.
IENTC	Enables Timer C interrupt requests
PDR9	Stores P92 output pin data
P92	LED output

3. Principle of Operation

1. Figure 2 illustrates the principle of operation of this sample task. As shown in figure 2, the interrupt period by the Timer C auto-reload function is set by hardware processing and software processing.

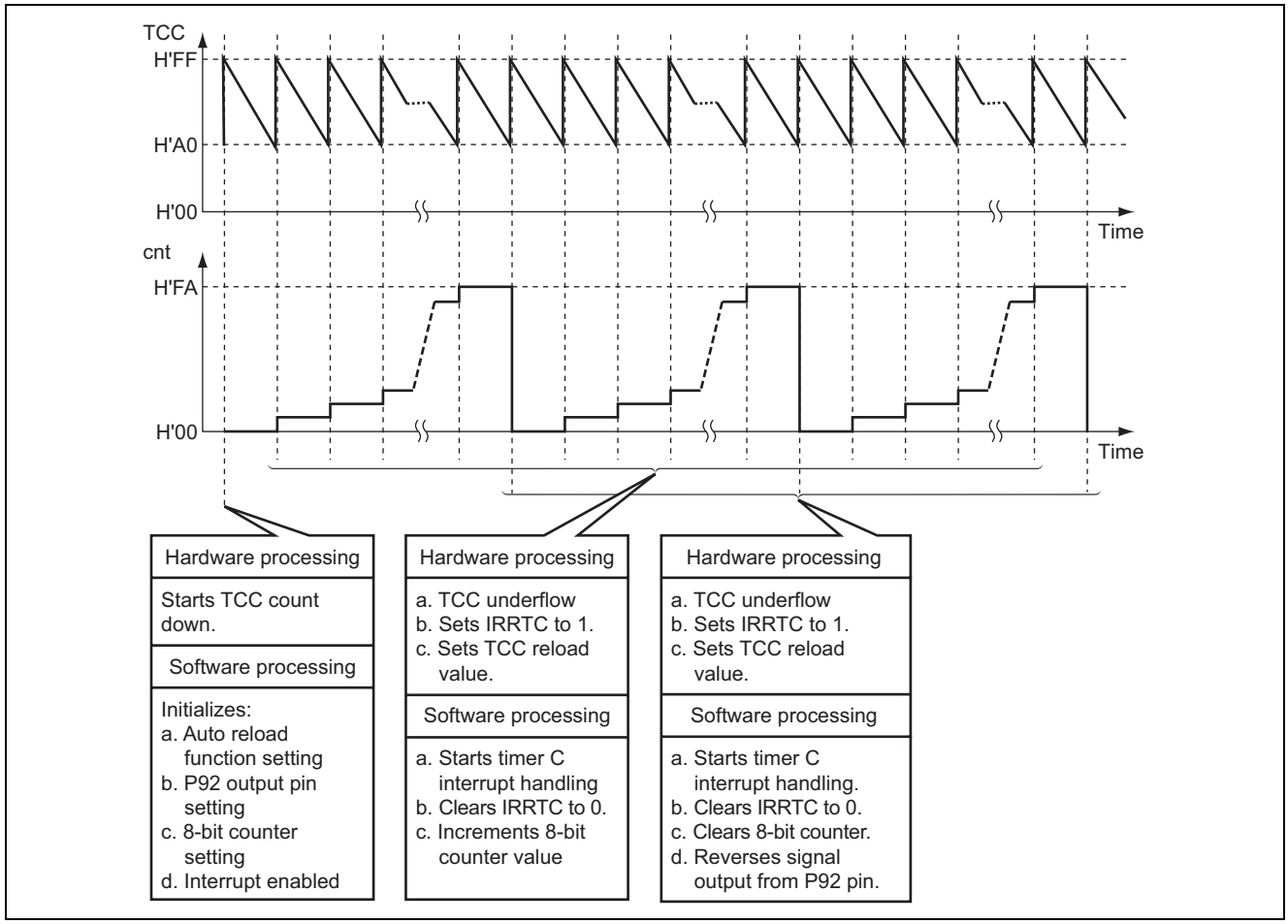


Figure 2 Operation Principle of Interrupt Period Setting by Timer C Auto-Reload Function

4. Description of Software

4.1 Modules

Table 2 describes the modules in this sample task.

Table 2 Description of Modules

Module	Label	Function
Main Routine	main	Sets the auto-reload function, sets Port 92, sets the 8-bit counter, enables interrupts
Count Up	tcint	Increments the 8-bit counter value and sets CTEDF to 1 when the counter value of the 8-bit counter becomes H'FA.

4.2 Arguments

Arguments are not used in this sample task.

4.3 Internal registers

Table 3 describes the internal registers in this sample task.

Table 3 Description of Internal Registers

Register		Function	Address	Setting
TMC	TMC7	Timer Mode Register C (Auto-Reload Function Select) When TMC7 = 0, Timer C function is set to Interval timer function. When TMC7 = 1, Timer C function is set to auto-reload function.	H'FFB4 Bit 7	1
	TMC6 TMC5	Timer Mode Register C (Counter Up/Down Control) When TMC6 = 0 and TMC5 = 0, TCC is an up-counter. When TMC6 = 0 and TMC5 = 1, TCC is a down-counter. When TMC6 = 1 and TMC5 = *, TCC is under hardware control by UD pin input. Note: *: Don't care	H'FFB4 Bit 6 Bit 5	TMC6 = 0 TMC5 = 1
	TMC2 TMC1 TMC0	Timer Mode Register C (Clock Select) When TMC2 = 0 and TMC1 = 1 and TMC0 = 1, TCC input clock is set to system clock/64.	H'FFB4 Bit 2 Bit 1 Bit 0	TMC2 = 0 TMC1 = 1 TMC0 = 1
TCC		Timer Counter C An 8-bit down-counter using the system clock/64 as input. When TCC underflows, the set value (H'A0) in TLC is loaded to TCC.	H'FFB5	H'00
TLC		Timer Load Register C When TLC = H'A0, TCC starts counting down from H'A0 and when TCC underflows, TLC set value (H'A0) is loaded to TCC.	H'FFB5	H'A0

Register		Function	Address	Setting
PDR9	P92	Port Data Register 9 (Port Data Register 92) When P92 = 0, the output level of P92 pin is "low". When P92 = 1, the output level of P92 pin is "high".	H'FFDC Bit 2	0
IENR2	IENTC	Interrupt Enable Register 2(Timer C Interrupt Enable) When IENTC = 0, Timer C interrupt request is disabled. If IENTC = 1, Timer C interrupt request is enabled.	H'FFF4 Bit 1	1
IRR2	IRRTC	Interrupt Request Register 2(Timer C Interrupt Request Flag) When IRRTC = 0, Timer C interrupt is not requested. When IRRTC = 1, Timer C interrupt is requested.	H'FFF7 Bit 1	0

4.4 RAM

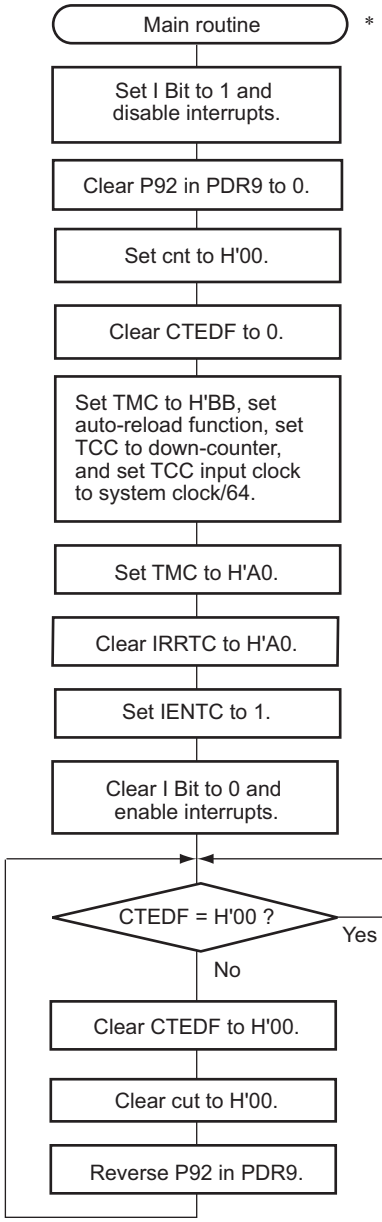
The RAMs used in this sample task are described in table 4.

Table 4 Description of RAM Used

Label	Function	Address	Used in
cnt	8-bit counter	H'FB80	Count up
CTEDF	Data that indicates whether or not the counter value of the 8-bit counter (cnt) has become H'FA When cnt < H'FA, CTEDF = H'00 When cnt == H'FA, CTEDF = H'01	H'FB81	Main Routine Count up

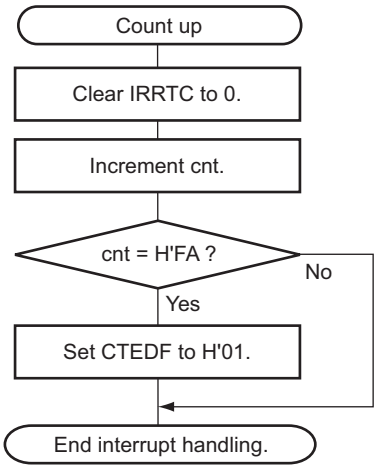
5. Flowchart

1. Main routine



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

2. Timer C interrupt handling routine



6. Program Listing

INIT.SRC (Program listing)

```
    .EXPORT     _INIT
    .IMPORT     _main
;
    .SECTION    P,CODE
_INIT:
    MOV.W       #H'FF80,R7
    LDC.B       #B'10000000,CCR
    JMP         @_main
;
    .END
```

```
/************************************************************************************************/
/*                                                                                              */
/*  H8/300L Super Low Power Series                                                              */
/*      -H8/38024 Series-                                                                       */
/*  Application Note                                                                            */
/*                                                                                              */
/*'8-bit Counter Count-Up by Interval Function'                                                 */
/*                                                                                              */
/*  Function                                                                                    */
/*  :Timer C Interval Timer                                                                     */
/*                                                                                              */
/*  External Clock :  10MHz                                                                     */
/*  Internal Clock :  5MHz                                                                      */
/*  Sub Clock:        32.768kHz                                                                 */
/*                                                                                              */
/************************************************************************************************/

#include     <machine.h>

/************************************************************************************************/
/*  Symbol Definition                                                                           */
/************************************************************************************************/
struct BIT {
    unsigned char    b7:1;      /* bit7 */
    unsigned char    b6:1;      /* bit6 */
    unsigned char    b5:1;      /* bit5 */
    unsigned char    b4:1;      /* bit4 */
    unsigned char    b3:1;      /* bit3 */
    unsigned char    b2:1;      /* bit2 */
    unsigned char    b1:1;      /* bit1 */
    unsigned char    b0:1;      /* bit0 */
};
```

```
#define      TMC           *(volatile unsigned char *)0xFFB4   /* Timer Mode Register C         */
#define      TCC           *(volatile unsigned char *)0xFFB5   /* Timer Counter C               */
#define      TLC           *(volatile unsigned char *)0xFFB5   /* Timer Load Register C         */
#define      PDR9_BIT      (*(struct BIT *)0xFFDC)             /* Port Data Register 9          */
#define      P92           PDR9_BIT.b2                         /* Port Data Register 92         */
#define      IRR2_BIT      (*(struct BIT *)0xFFF7)             /* Interrupt Request Register 2  */
#define      IRRTC         IRR2_BIT.b1                         /* Timer C Interrupt Request Flag*/
#define      IENR2_BIT     (*(struct BIT *)0xFFF4)             /* Interrupt Enable Register 2   */
#define      IENTC         IENR2_BIT.b1                        /* Timer C Interrupt Enable      */

#pragma interrupt   (tcint)
/************************************************************************************************/
/*  Function define                                                                             */
/************************************************************************************************/
extern void INIT ( void );                                    /* SP Set                        */
void         main ( void );
void         tcint ( void );

/************************************************************************************************/
/*  RAM define                                                                                  */
/************************************************************************************************/
unsigned char       cnt;                                      /* 8bit Counter                  */
unsigned char       CTEDF;                                    /* End  Data                     */

/************************************************************************************************/
/*  Vector Address                                                                              */
/************************************************************************************************/
#pragma section     V1                                    /* Vector Section Set              */
void (*const VEC_TBL1[])(void) = {                        /* 0x0000 - 0x000F                 */
    INIT                                                  /* 0x0000 Reset Vector             */
};
#pragma section     V2                                    /* Vector Section Set              */
void (*const VEC_TBL2[])(void) = {
    taint                                                 /* 0x001A Timer C Interrupt Vector */
};

#pragma section                                           /* P                               */
/************************************************************************************************/
/*  Main Program                                                                                */
/************************************************************************************************/
void main ( void )
{
    set_imask_ccr(1);                                     /* Interrupt Disable               */

    P92 = 0;                                              /* Clear P92                       */

    cnt = 0;                                              /* Initialize 8bit  Counter        */
    CTEDF = 0;

    TMC = 0xBB;
    TLC = 0xA0;

    IRRTC = 0;                                            /* Clear IRRTC                     */
    IENTC = 1;                                            /* Timer A Interrupt Enable        */
```

```
    set_imask_ccr(0);                                   /* Interrupt Enable              */
    while (1) {
        while (CTEDF == 0);

        CTEDF = 0;
        cnt = 0;

        P92 = ~P92;
    }
}

/*****************************************************************************************/
/*  Timer A Interrupt                                                                    */
/*****************************************************************************************/
void tcint ( void )
{
    IRRTC = 0;                                          /* Clear IRRTC                   */
    cnt++;

    if ( cnt == 0xFA ) {                                /* 8bit Counter = 0xff?          */
        CTEDF = 1;                                      /* Clear 8bit Counter            */
    }
}
```

Link address specifications

Section Name	Address
CV1	H'0000
CV2	H'001A
P	H'0100
B	H'FB80

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		Description	
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