Renesas Synergy™ Platform

Using ADC to Wake Up the MCU from Low Power Modes

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Introduction

This application note describes how to implement an application for reading analog inputs through a 14-bit ADC model during MCU sleeping/standby, and how to set up different ADC comparison functions for staying in low power mode (LPM), or returning to the normal running mode. The application program is created on DK-S124 (version 3.0) board, a Renesas Synergy development board, using the Renesas e^2 studio ISDE and the Renesas Synergy Software Package (SSP).

Goal and Objectives

The goal of this application note is to illustrate a general framework for reading analog signals during sleep/standby, and waking up the MCU, or keeping it in sleep state with different ADC conditions.

An example shows how to create an application using the 14-bit ADC, to read analog signals that are generated by adjusting the potentiometer when the Synergy S124 device is in the Snooze mode, and how to set different events on canceling the Snooze mode, such as either returning to the Software Standby mode, or returning to the Normal mode.

You can easily substitute the potentiometer with other analog sources, such as light sensors, motion sensors, and so forth, and re-define the ADC window functions for different waking up conditions, to create more complex applications.

Prerequisites

As the reader of this application note, you are assumed to have some experience with the Renesas e^2 studio ISDE and SSP. For example, before you perform the procedure in this application note, you should follow the procedure in your board's Quick Start Guide to build and run the Blinky project. By doing so, you will become familiar with e^2 studio ISDE and the SSP, and ensure that the debug connection to your board is functioning properly.

Required Resources

This example application targets Renesas Synergy S124 devices. To build and run the application, you will need:

- A Renesas Synergy DK-S124 board (version 3.0)
- A PC running Microsoft® Windows® 7 with the following Renesas software installed:
  - e^2 studio ISDE v5.4.0.023 or later
  - SSP v1.2.0 or later
  - IAR Embedded Workbench® for Renesas Synergy™ v7.71.2 or later
  - Synergy Standalone Configurator (SSC) v5.4.0.023 or later

You can download the required Renesas software from the Renesas Synergy Gallery: (https://synergygallery.renesas.com).

For instructions on importing the project into e^2 studio and building/running the project, see *Importing a Renesas Synergy Project* (Renesas, 2017), in the References section.

Contents

1. Overview

This design demonstrates how to make a typical IoT low power sensor hub, where the CPU is in a sleeping mode, and the environmental sensor such as a motion, temperature, or smoke sensor, is checked without waking up the CPU periodically, until a sensor value meets a predefined condition.

Hardware installation: The Micro USB J14 is connected to your PC host for debugging and programming through the JLink protocol.

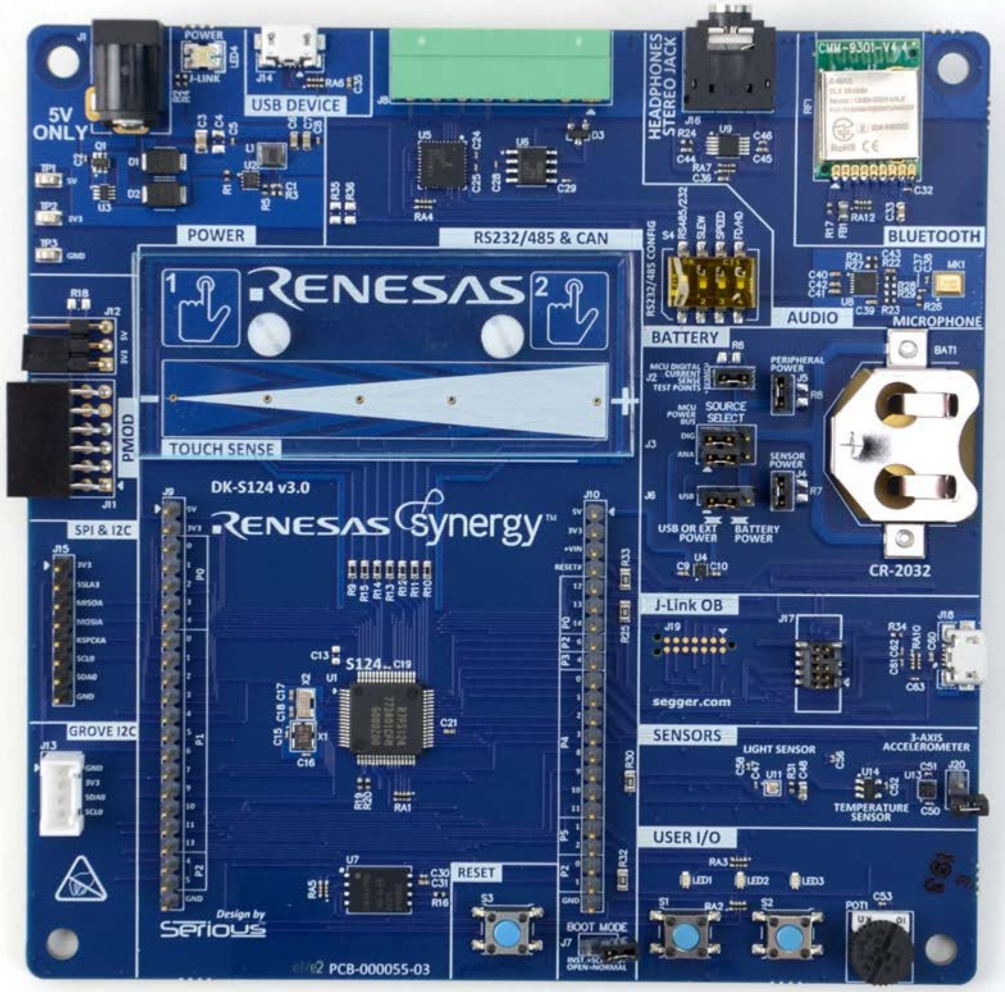


Figure 1.1 DK-S124 (version 3.0) board

Figure 1.2 Checking the environment sensor during sleep mode

The application uses the Low Power Mode (LPM) and the ADC module in the Synergy S124 MCU.

Using the Software Standby mode, which is one of the low power modes, the CPU is put in a sleep state, where the RTC timer at 32 kHz generates an interrupt periodically.

Each RTC PRD interrupt puts the MCU in Snooze mode, which is another low power mode, where the CPU is still in sleep state, but the 14-bit ADC is triggered.

Using the ADC compare function windows, different results or events can be set from predefined comparison conditions, which are used to decide if the CPU is still in sleep state, or is waking up to a running state.

A state diagram in Figure 1.3, shows the MCU states and LPM transitions used in this application.

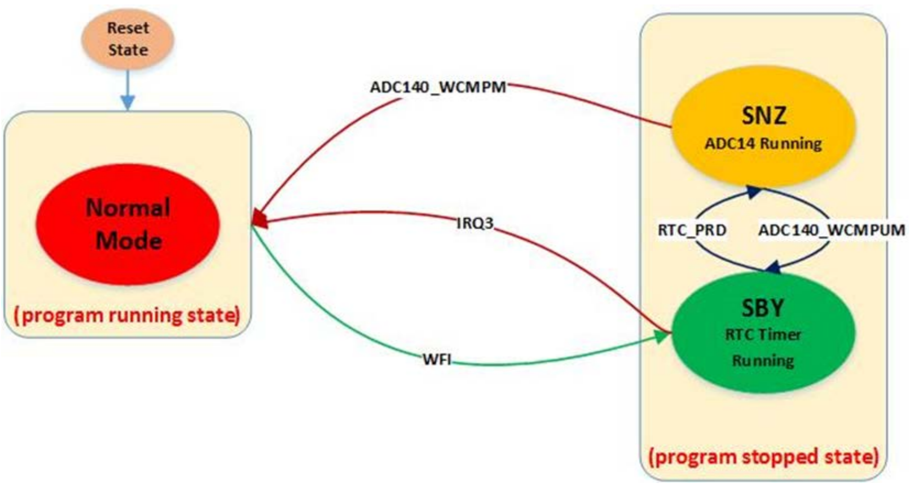


Figure 1.3 MCU states and LPM transitions used in this application

2. Peripheral Modules

This section describes the LPM, and the ELC, and ADC modules in the Synergy S124 MCU, and how to configure them for achieving the expected functionality.

2.1 LPMs for Configuring Different Sleep States

This application aims to show how to reduce the MCU power consumption, check analog sensors, and adjust the MCU states. The S124 device has three Low Power Modes (LPM), namely the Sleep mode (SLP), Software Standby mode (SBY), and Snooze mode (SNZ). Each mode has a differences in configuration for clock sources, available peripheral modes, and power consumption, among other things.

2.1.1 LPMs to be used

Table 10.2 in the *S124 User's Manual* specifies the operating conditions of each low power mode.

The low power modes to be used for reducing power consumption are as follows:

- Sleep mode (SLP): The CPU stops operating, however, the contents of the internal registers are retained. Other peripheral functions do not stop. Wake the CPU using any interrupt, RES pin reset, power-on reset, voltage monitor reset, SRAM parity error reset, or a reset caused by an IWDT or a WDT underflow.
- Software Standby mode (SBY): The CPU, and most of the on-chip peripheral functions and oscillators stop. However, the contents of the CPU internal registers and SRAM data, the states of on-chip peripheral functions and I/O ports are retained. This mode allows a significant reduction in power consumption because most of the oscillators stop in this mode. Only those interrupts specified in the Wake Up Interrupt Enable register (WUPEN) are capable of cancelling the Software Standby mode. According to the operating and standby currents specified in Table 41.12 in the *S124 User's Manual*, the SBY has the lowest power consumption among the three LPMs. So, this mode will be used in this application.
- Snooze mode (SNZ): Similar to the Sleep mode, some peripheral modules can operate without waking up the CPU. For example, the 14-bit ADC converter is able to read analog sensors and check if some predefined conditions, such as the ranges of ADC values, are satisfied or not, and then stay in the LPM, or wake up the CPU. The conditions to enter the Snooze mode, called Snooze requests are specified in Table 2.1, and the conditions to transition from the Snooze mode to the Standby mode are called Snooze end conditions, which are specified in Table 2.2.

Table 2.1 Events that cause a transition from SBY to SNZ mode

Snooze request	Control register	
	Register	Bit
PORT_IRQn (n = 0 to 7)	SNZREQCR	SNZREQENn (n = 0 to 7)
KEY_INTKR	SNZREQCR	SNZREQEN17
ACMP_LP0	SNZREQCR	SNZREQEN23
RTC_ALM	SNZREQCR	SNZREQEN24
RTC_PRD	SNZREQCR	SNZREQEN25
AGT1_AGTI	SNZREQCR	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR	SNZREQEN30
RXD0 falling edge	SNZCR	RXDREQEN[1]

Table 2.2 Events that end SNZ mode

<table>
<tr><th rowspan="2">Operating module when a Snooze end request occurs</th><th colspan="2">Snooze end request</th></tr>
<tr><th>AGT1 underflow</th><th>Other than AGT1 underflow</th></tr>
<tr><td>DTC</td><td rowspan="3">The MCU transfers to the Software Standby mode after all the modules listed to the left complete operation</td><td rowspan="4">The MCU transfers to the Software Standby mode after all the modules to the left complete operation</td></tr>
<tr><td>ADC140</td></tr>
<tr><td>CTSU</td></tr>
<tr><td>SCI0</td><td>The MCU transfers to the Software Standby mode immediately after a Snooze end request is generated</td></tr>
<tr><td>Other than above</td><td colspan="2">The MCU transfers to the Software Standby mode immediately after a Snooze end request is generated</td></tr>
</table>

Note: If the DTC is used to activate the ADC140, CTSU, or SCI, the MCU transitions to Software Standby mode after a Snooze end request is generated.

[1] RXDREQEN bit must not be set to 1 unless in asynchronous mode.

2.1.2 Possible power mode transitions

Available transitions between Normal mode and LPM mode are shown below. The conditions or interrupt sources for triggering such a transition are specified in the *S124 User's Manual*. Selecting different conditions create different applications. Figure 2.1 shows one such application for using the ADC140 for a Snooze end condition.

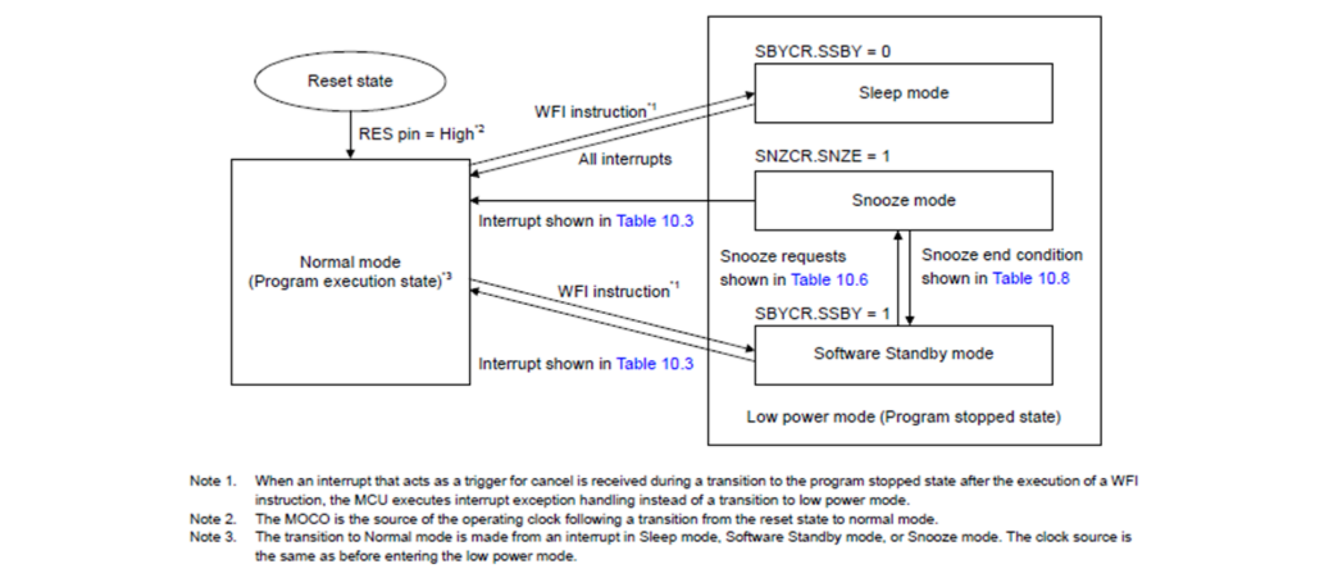


Figure 2.1 All possible LPM mode transitions for the S124 MCU

2.2 ELC for Running the ADC without Waking the CPU

To trigger the ADC in the Snooze mode without waking up the CPU, the Event Link Controller (ELC) is used to forward the event requests generated. Two sets of control registers, ELSEGR0, 1, and ELSRn should be set before entering the Standby mode. For example, to trigger an ADC operation in the Standby mode directly, set the SYSTEM_SNZREG event in the ELSR0, which is the entry for the ADC14 peripheral, as shown in Figure 2.2.

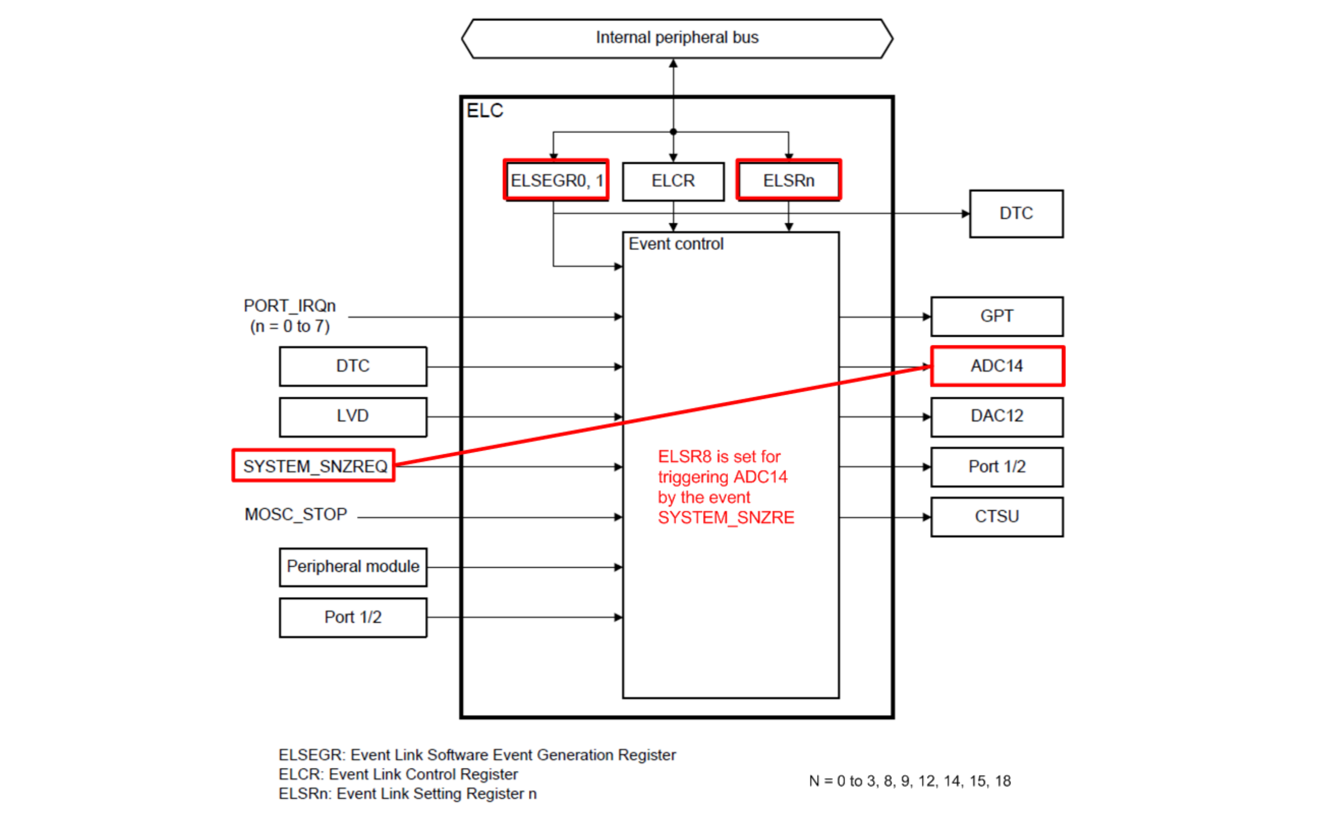


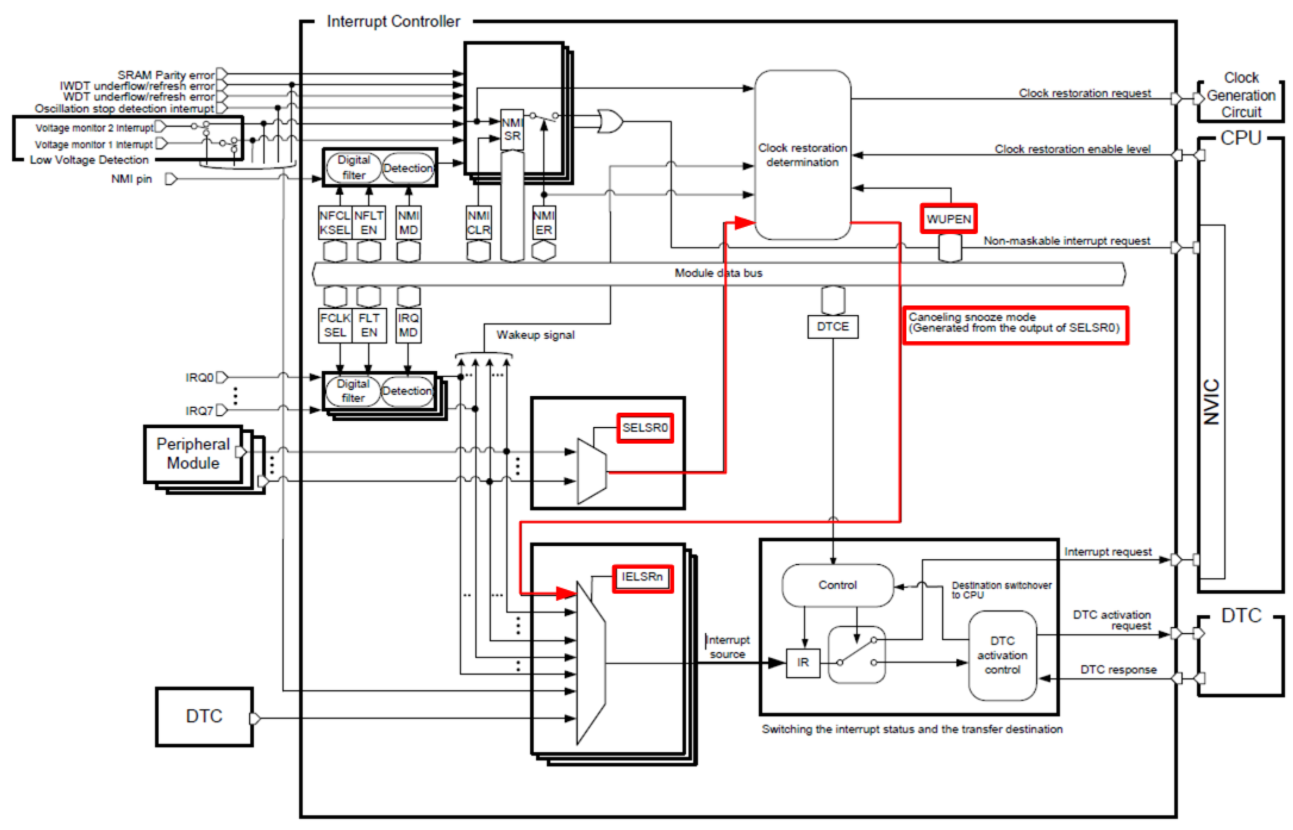
Figure 2.2 Selecting a proper source event to trigger a peripheral operation in ELC

Implement with the SSP ELC driver API as follows:

```
//set SYSTEM_SNZREQ to trigger ADC0
g_elc.p_api->linkSet(ELC_PERIPHERAL_ADC0, ELC_EVENT_LPM_SNOOZE_REQUEST);
```

2.3 ICU for Waking the CPU from LPM

The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller/ Data Transfer Control (NVIC/DTC) module. It is also required for waking up the CPU from different LPM modes, as shown in Figure 2.3.



NMISR: Non-Maskable Interrupt Status Register	FCLKSEL: IRQi Digital Filter Sampling Clock Select (IRQCRi.FCLKSEL (i = 0 to 7))
NMIER: Non-Maskable Interrupt Enable Register	FLTEN: IRQi Digital Filter Enable (IRQCRi.FLTEN (i = 0 to 7))
NMICLR: Non-Maskable Interrupt Status Clear Register	SELSR0: SYS Event Link Setting Register 0
NMIMD: NMI Detection Set (NMICR.NMIMD)	WUPEN: Wake Up Interrupt Enable Register
NFCLKSEL: NMI Digital Filter Sampling Clock Select (NMICR.NFCLKSEL)	IELSRn: ICU Event Link Setting Register (n = 0 to 31)
NFLTEN: NMI Digital Filter Enable (NMICR.NFLTEN)	IR: Interrupt Status Flag (IELSRn.IR)
IRQMD: IRQi Detection Sense Select (IRQCRi.IRQMD (i = 0 to 7))	DTCE: DTC Activation Enable (IELSRn.DTCE)

Figure 2.3 ICU functional blocks for waking up the LPM

Actions while waking up from different LPM modes are as follows:

- From Sleep mode, return is initiated by the non-maskable interrupts or any other interrupt source.
- From Standby mode, return is initiated by the non-maskable interrupts. Interrupts can be selected by the WUPEN register.
- From the Snooze mode, return is initiated by the non-maskable interrupts. Interrupt can be selected with the SELSR0 and WUPEN registers. The SELSR0 register selects the events that wake up the CPU from Snooze mode. Two registers are to be set:
  - Assign an event that is checked under Canceling Snooze, in Table 12.4, Event Table, in the *S124 User's Manual,* set in SELSR0.SELS[7:0]. For example, ADC140_WCMPM (0x20) is used here to wake up the CPU from the SNZ.
  - Assign the event ICU_SNZCANCEL (0x0B), set in IELSRn.IELS[7:0], to enable an SELSR0 event interrupt.

2.4 ADC for Setting Analog Conditions for an LPM Transition

The S124 MCU has a 14-bit A/D Converter (ADC14) unit, which can be used for reading up to 18 analog channels, and the on-chip temperature sensor/internal reference voltage. On the DK-S124 version 3.0 board, a potentiometer is already connected to the analog channel 7, enable this channel to the ADC14, and easily generate different values by turning the potentiometer wheel.

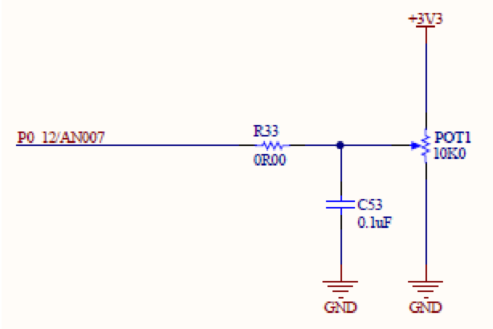


Figure 2.4 Potentiometer connection to the analog channel 7 on DK-S124 (version 3.0)

2.4.1 Scanning analog channels

The ADC14 module supports three different scanning modes:

- Single scan: goes through the enabled analog channels in ascending order of channel number
- Continuous scan: performs a single scan continuously
- Group scan: partitions the analog channels in two groups (group A and group B), then performs a single scan for each group.

  This design only reads the channel 7 once each time, and so the single scan mode is set for ADC14.

2.4.2 Starting an ADC operation

The ADC14 control logistics are shown in Figure 2.5, where there are two different kinds of triggers - a synchronous event from ELC, or an asynchronous event from an input pin (ADTRG0).

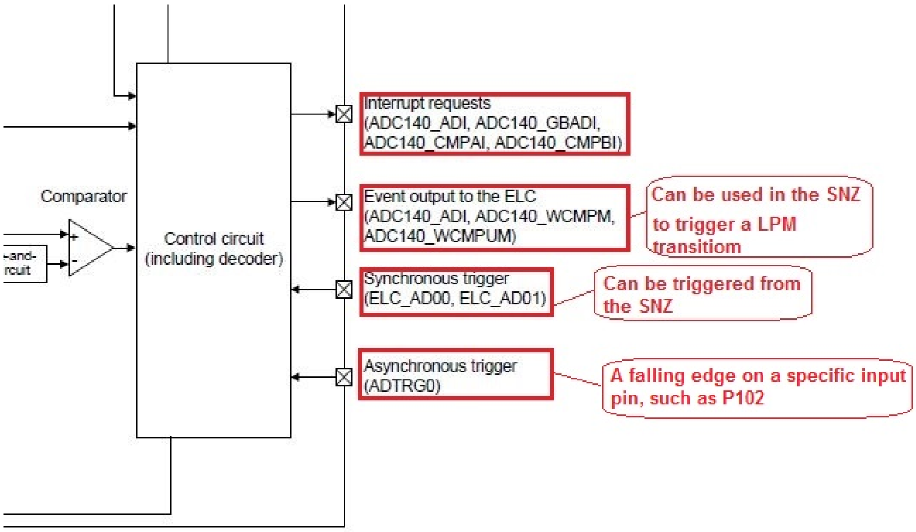


Figure 2.5 Input and output events for ADC14

As a synchronous trigger, ELC_AD00 can be considered an output from the ELC, and generated when an event SYSTEM_SNZREQ is provided. Such a relation is specified in the ELC.ELSR8 register. This is a critical link between the LPM and ADC module in this design.

2.4.3 Setting a compare function in the ADC

The ADC values can be compared with some predefined windows or ranges on each analog channel, and two different events are generated:

- ADC140_ADI: an interrupt for completing all selected channel conversion
- ADC_WCMPM: when the ADC value matches the comparison conditions on Window A/B
- ADC_WCMPUM: when the ADC value does not match the comparison conditions on Window A/B.

For example, for a compare function window A, there are 4 different comparison results by setting different values on two control register bits, as shown in .

Table 2.3 Four different compare conditions for ADC Windows A/B

Enable Window A Function (ADCMPCR.WCMPE)	Compare Conditions (ADCMPLR0.CMPLCHAn)	
Disabled (0)	Larger than the lower boundary (0)	ADCMPDR0 value > A/D-converted value
	Smaller than the lower boundary (1)	ADCMPDR0 value < A/D-converted value
Enabled (1)	Out of range (0)	A/D converted value < ADCMPDR0 value, or ADCMPDR1 value < A/D-converted value
	Within a range (1)	ADCMPDR0 value < A/D-converted value < ADCMPDR1 value

For example, a good range is selected for the potentiometer by setting the following ADC Compare Control register bits to check if the ADC value matches a condition, that is, within the range of 12,000 to 16,000.

```
//--- Set the Window_A ------
//Select a channel for Window_A Comparison
R_S14ADC->ADCMPANSR0_b.CMPCHA07 = 0x1;
//Set the Window_A Lower boundary
R_S14ADC->ADCMPDR0_b.ADCMPDR0 = POT_RD_LOW_A; //12,000
//Set the Window_A Upper boundary
R_S14ADC->ADCMPDR1_b.ADCMPDR1 = POT_RD_HIGH_A; //16,000
//Set the Window_A comparison condition
R_S14ADC->ADCMPLR0_b.CMPLCHA07 = 0x1;
//Enable Window_A operation
R_S14ADC->ADCMPCR_b.CMPAE = 0x1;
//Enable Window_A interrupt for meeting the condition, ADC140_CMPAI
R_S14ADC->ADCMPCR_b.CMPAIE = 0x1;
//Enable Window_A/B Comparison Function
R_S14ADC->ADCMPCR_b.WCMPE = 0x1;
```

Once the condition is matched, it generates an ADC140_WCMPM event, which is already set in the ICU as an event to wake up the CPU from Snooze mode.

```
//Enable Window_A/B composite condition
R_S14ADC->ADCMPCR_b.CMPAB = 0x0; //output ADC140_WCMPM
------------------------------------
//set ADC140_ADI as the event of ending SNZ
R_ICU->SELSR0_b.SELS = 0x20;        //ADC140_WCMPM to cancel SNZ
```

3. Application Implementation

This section summarizes those setup steps already described in previous sections in to a block diagram, with the algorithm used, and provides some usage information about the design on a SK-S124 version 3.0 board.

3.1 Algorithm

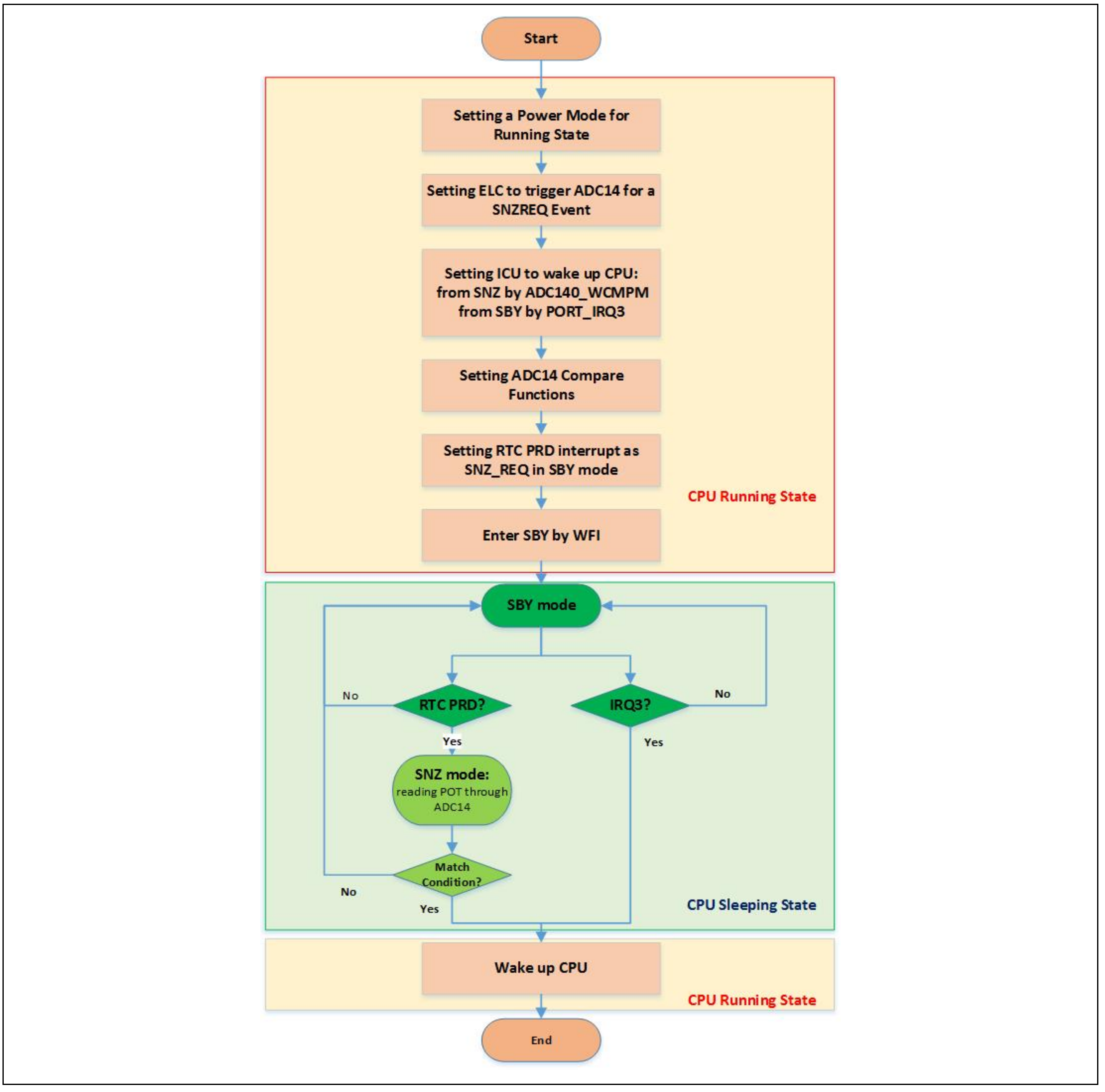


Figure 3.1 Algorithm used for checking ADC conditions in the Snooze mode

3.2 User interface

The user interface in this design on DK-S124 version 3.0 board is configured as follows:

- Switch function:
  - Press the switch S1 to enter Software Standby mode
  - Turn the POT1 to generate different analog values. This may wakeup the MCU from the Snooze mode if the value is within the predefined range of 12,000 to 16,000
  - Press the switch S2, to wake up the MCU from Standby mode
  - Press the switch S3, to reset the application for a new round of testing after waking up from the Standby or Snooze mode.

- LED function:
  - After powering on or pressing S3, LED1, LED2, and LED3 are on, indicating that the MCU is in the High-speed mode. You can modify the source code to enter other power modes such as Middle-speed, or Low-speed mode, and so forth, which have different LED on/off coding.
  - When the MCU is in a low power mode such as Standby or Snooze mode in this case, the LED1 is off. The LED1 is on when the MCU is in normal state. The LED1 will be blinking before the MCU changes state.

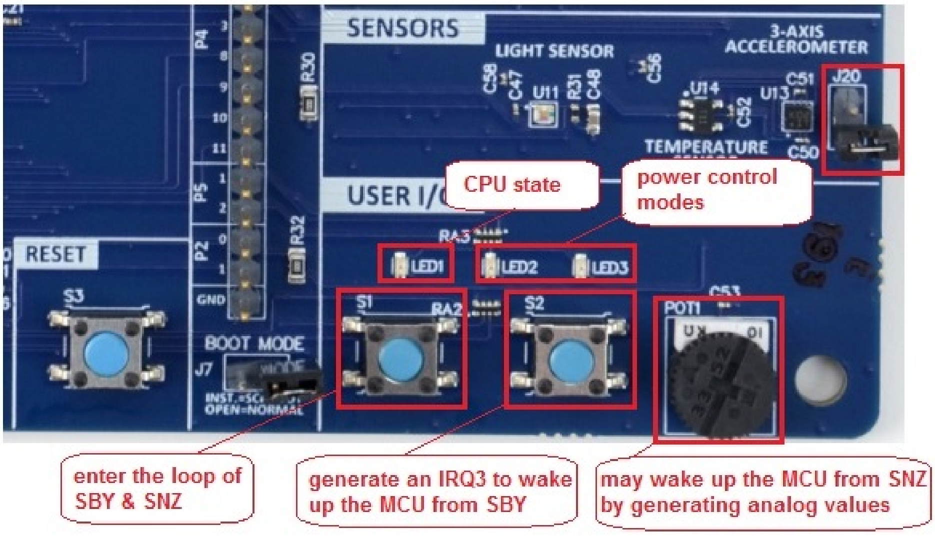


Figure 3.2 User interface of this design

4. Conclusion

In this document, a general platform of using a predefined logic condition on the ADC compare functions is demonstrated, including LPM transitions in Synergy S124 MCU, such as staying in the sleep state, or waking the CPU. As an example, the following configurations are selected:

- The potentiometer, POT1 on the DK-S124 board is selected to generate different analog values
- An ADC value range of 12,000 to 16,000 is set as the compare function on both the ADC windows A and B.A 2 second RTC periodic interrupt enables transitions from Standby mode to Snooze mode, where the ADC reads and checks the condition defined above, without activating the CPU. If the ADC value lies within the range, the CPU wakes up to execute high performance tasks.
- If the conditions do not match, that is, the potentiometer value is out of the defined range, the MCU is woken up and is ready for performing any high performance tasks. The ADC value range for the potentiometer is defined between 10000 and 16000. To verify the application is working, turn the potentiometer to one end and verify the results provided. If the CPU is waking up, reset the board and try the other end of the potentiometer to verify the results.

The example is implemented with the Synergy SSP API (v1.2.0 or later) and some bare-metal code, which is completely integrated with the next release of the SSP packages.

Further extensions can be made to other analog sensors on the DK-S124 board, such as temperature sensor TMP35, the light sensor APDS-9005, or other sensors through the external connectors. You can also replace the existing High-speed mode with other different power modes, such the Middle-speed mode, Low-speed, or Low-voltage modes, and experience complex power saving strategies supported by the Synergy MCUs.

Note: A full power-on reset cycle is required for operating the LPM, and so, it is impossible to debug an LPM application through the JTAG/LLink interface.

5. References

Renesas. (2017). *Importing a Renesas Synergy Project* (r11an0023eu0117-synergy-ssp-import-guide.pdf).

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug 30, 2016	-	Initial version
1.20	Feb 10, 2017	-	Migrated to SSP 1.2.0
1.21	Aug 4, 2017	-	Migrated to SSP 1.3.0
1.22	Sep 27, 2017	1, 11	Required resources of SSP version changed

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