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H8SX Family

Using the 32K Timer in Subclock Operation as a 24-hour Clock

Summary

In this example, we describe how to use the 32K timer in subclock operation to realize a 24-hour timer.

Target Device

H8SX/1663F

Introduction

Descriptions in this application note are in line with those in the hardware manual for the H8SX/1663 group, and the program is usable on the above device for which operation has been confirmed.

However, since some functions and the set of included functions will vary with the actual device in use, only apply the program after full evaluation with confirmation against the relevant hardware manual.

Contents

1. Specifications

In this example, the 32K timer is applied in subclock operation to realize a 24-hour clock.

With an overflow period of one second, the 32K timer generates interrupts every time it overflows. Counters set up in on-chip RAM for clocks are incremented within the processing routine for 32K timer interrupts. These counters consist of an 8-bit seconds counter, an 8-bit minutes counter, and an 8-bit hours counter. After counting has reached 23 hours, 59 minutes, and 59 seconds from 00 hours, 00 minutes, and 00 seconds, the counters are re-initialized to 00 hours, 00 minutes, and 00 seconds by the next incrementation, and counting up continues again in the same way.

Figure 1 is a diagram of the mode transitions in this sample application and is explained below.

1. Setting bit CK32K = 1 in the SUBCKR shifts the program-execution state from main-clock operation to subclock operation.
2. Executing a SLEEP instruction shifts subclock operation from the program-execution state to software-standby mode.
3. A 32K timer interrupt shifts subclock operation back to the program-execution state so that the 32K interrupt is accepted.
4. Within processing for the 32K-timer-interrupt, the clock counters are made to count up.
5. Operation continues with repetition of the above steps (2) to (4). In this sample application, all of these steps are handled in subclock operation.

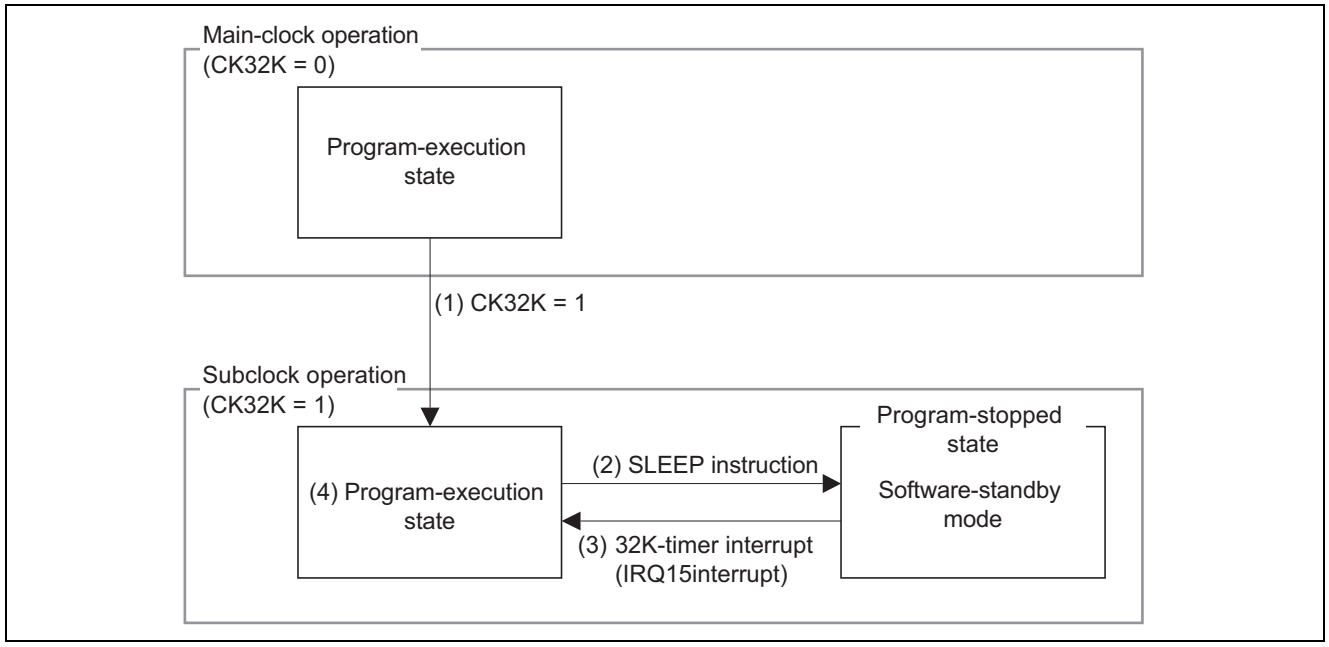


Figure 1 Mode-Transition Diagram for the Sample Application

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Details
Main-clock operating frequencies	EXTAL input clock: 12 MHz System clock (Iϕ): 24 MHz (input clock frequency-multiplied by 2) Peripheral-module clock (Pϕ): 24 MHz (input clock frequency-multiplied by 2) External-bus clock (Bϕ): 24 MHz (input clock frequency-multiplied by 2)
Subclock operating frequencies	Subclock: 32.768 kHz System clock (Iϕ): 32.768 kHz Peripheral-module clock (Pϕ): 32.768 kHz External-bus clock (Bϕ): 32.768 kHz
MD_CLK pin	MD_CLK = 0
Operating mode	Mode 7 (single-chip mode) Mode-pin setting: MD2 = 1, MD1 = 1, MD0 = 1

3. Description of Module Usage

3.1 32K Timer (TM32K)

In the sample application, TM32K is applied to obtain 24-hour clock operation. The characteristics of TM32K are described below

- A 32.768-kHz clock signal is frequency-divided to obtain four forms of counter-input clock.
- A 32K timer-interrupt (32KOVI) is generated when the counter overflows.
- The overflow period is selectable from among four values: 250 ms, 500 ms, 1 s, and 2 s.
- The counter is operational except in hardware-standby mode and the reset state.

3.2 Switching to Subclock Operation by Using the Multi-clock Function

The multi-clock function is for switching between main-clock operation and subclock operation. When the CK32K bit of the SUBCKR is set to 1, operation switches from the main clock to the subclock at the end of the current bus cycle, regardless of the setting of the SCKCR. In subclock operation, the system clock (Iϕ), peripheral-module clock (Pϕ), and external-bus clock (Bϕ) are all run from the 32.768-kHz subclock.

When the CK32K bit of the SUBCKR is set to 0 during subclock operation, operation switches from the subclock to the main clock at the end of the current bus cycle.

Operation or stopping of the main-clock oscillator during subclock operation can be selected by the setting of the EXSTP bit in the SUBCKR.

In the same way as during main-clock operation, executing a SLEEP instruction while the SSBY bit of the SBYCR is set to 1 during subclock operation initiates a transition to the software-standby mode. When a transition to software-standby mode is made during subclock operation, the operating clock after release from software-standby mode can be selected by the WAKE32K bit of the SUBCKCR. The WAKE32 bit is set to 1 in this sample application, so operation after release from software-standby mode is subclock operation.

3.3 Software Standby Mode

3.3.1 Transition to Software Standby Mode

If a SLEEP instruction is executed when the SSBY bit in SBYCR is set to 1, software standby mode is entered. In this mode, the CPU, on-chip peripheral functions, and oscillator all stop. However, the contents of the CPU's internal registers, on-chip RAM data, and the states of on-chip peripheral functions other than the SCI, and the states of the I/O ports, are retained. Whether the address bus and bus control signals are placed in the high-impedance state or retain the output state can be specified by the OPE bit in SBYCR. In this mode the oscillator stops, allowing power consumption to be significantly reduced.

3.3.2 Release from Software-Standby Mode

Interrupts from the NMI pin and pins IRQ0 to IRQ11, the 32K-timer interrupt (IRQ15 interrupt), and the active signals on the $\overline{\text{RES}}$ pin and $\overline{\text{STBY}}$ pin all drive release from software-standby mode.

- Release by the 32K-timer interrupt (IRQ15 interrupt)
  When a 32K-timer interrupt (IRQ15 interrupt) request is input, the clock starts to oscillate. After the time determined by the setting of the STS4 to STS0 bits in the SBYCR has elapsed, the stabilized clock signal is supplied throughout the IC, which is released from software-standby mode and then starts interrupt-exception processing.
  In cases where release from software-standby mode is to be by a 32K-timer interrupt (IRQ15 interrupt), ensure that bit IRQ15E in the IER and bit SSI15 in the SSIER are both set to 1 and that no interrupts with a priority higher than that of the 32K-timer interrupt (IRQ15 interrupt) will be generated. If interrupts are masked on the CPU side or the interrupt has been set as an initiating source for the DTC, release from software-standby mode will still not be possible.

3.3.3 Setting Oscillation Settling Time after Clearing Software Standby Mode

Bits STS4 to STS0 in SBYCR should be set as described below.

1. Using a crystal oscillator
   Set bits STS4 to STS0 so that the standby time is longer than the oscillation settling time.
   When the crystal oscillator frequency in sub clock mode (Pϕ) = 32.768 kHz, a recommended standby time is 512 states, which is determined by STS4 to 0 (= B'00110).
2. Using an external clock
   A PLL circuit settling time is necessary. Refer to table 23.2 to set the standby time.

4. Description of Operation

The timing of operations in the sample application is shown in figure 2. As an explanation of figure 2, table 2 gives details of hardware and software processing at the numbered points.

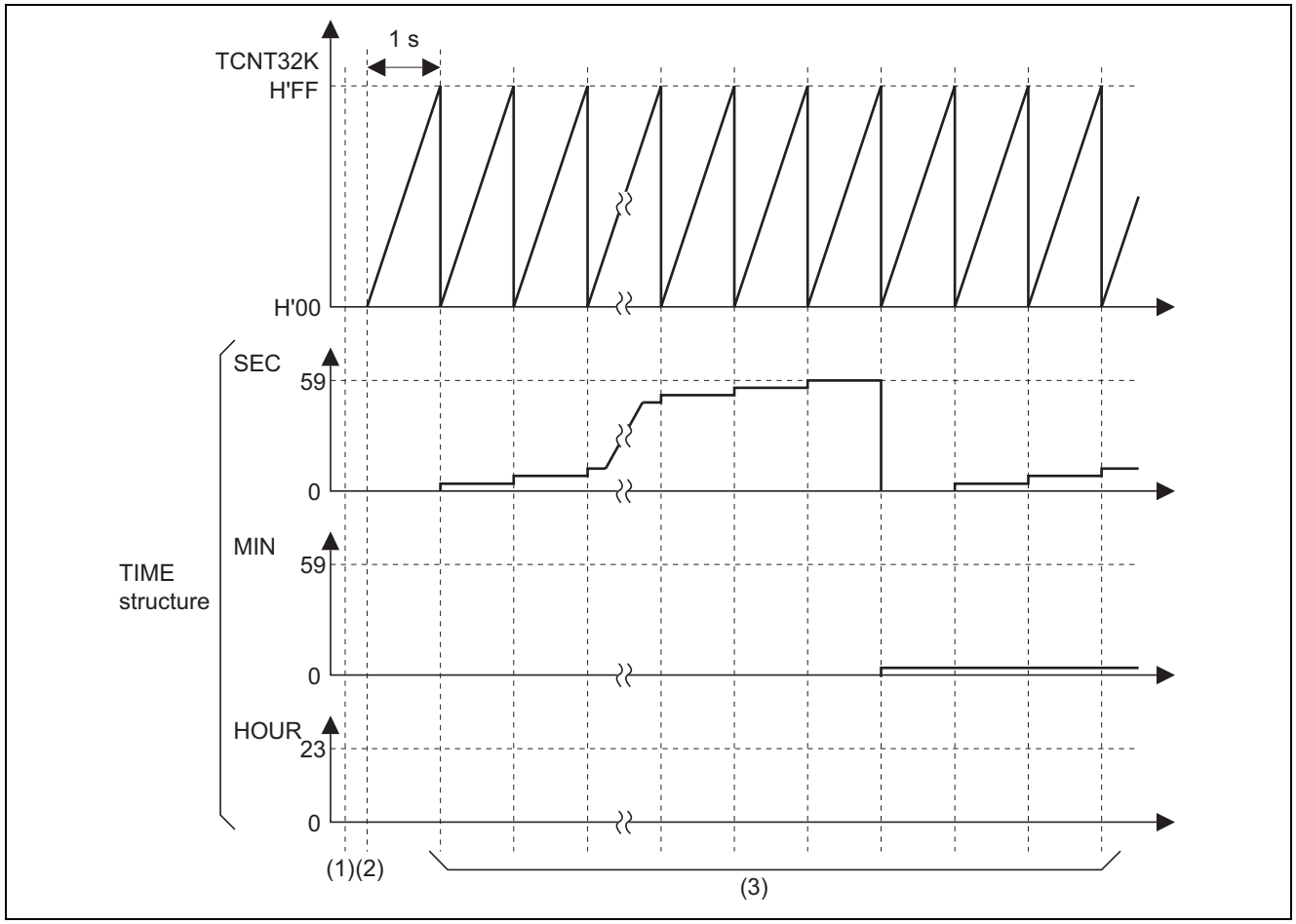


Figure 2 Operation of TCNT32K and the Software Counters

Table 2 Details of Processing

	Hardware Processing	Software Processing
1	Power-on reset	Initial settings (a) Settings for the 32K-timer interrupt (IRQ15 interrupt) (b) Setting the overflow period for TCNT32K to 1 s (c) Software-standby mode setting For details, see 5. Description of Software.
2	Start of counting by TCNT32K	No processing
3	32K-timer interrupts (a) Overflow of TCNT32K (b) Setting of IRQ15 status flag	32K-interrupt (IRQ15 interrupt) processing (a) Clearing the IRQ15 status flag (b) Counting up by the clock counters (TIME structure) in on-chip RAM

5. Description of Software

5.1 Operating Environment

Table 3 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Ver. 4.03.00
C/C++ compiler	H8, H8/300 Series C/C++ Compiler Ver. 6.02.00 from Renesas Technology
	Option settings -cpu=h8sxa:24:md, -code = machinecode, -optimize=1, -regparam=3 -speed=(register, shift, struct, expression)
Optimizing linkage editor	Optimizing Linkage Editor Ver. 9.03.00 from Renesas Technology
	Option settings: None

Table 4 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'FF2000	B	Non-initialized data area (on-chip RAM area)

Table 5 Interrupt- and Exception-Processing Vector Tables

Requesting Source	Vector Number	Vector Table Address	Destination Interrupt Function
Reset	0	H'000000	init
IRQ15	79	H'000013C	irq15_int

5.2 Description of Functions

The functions of the sample application are outlined in table 6. The hierarchy of calls is shown in figure 3.

Table 6 List of Functions

Function	Description
int	Initialization routine Releases required modules from the module-stop state, makes clock settings, and calls function main.
main	Main routine Sets the TM32K overflow period to one second and sets the 32K timer interrupt (IRQ15 interrupt). Also initiates the transition to software-standby mode after counting by the 32K timer has started.
irq15_int	Processing for the 32K timer interrupt (IRQ15 interrupt) Clears the IRQ15 interrupt flag, and stores the time in the SEC, MIN, and HOUR members of the TIME structure.

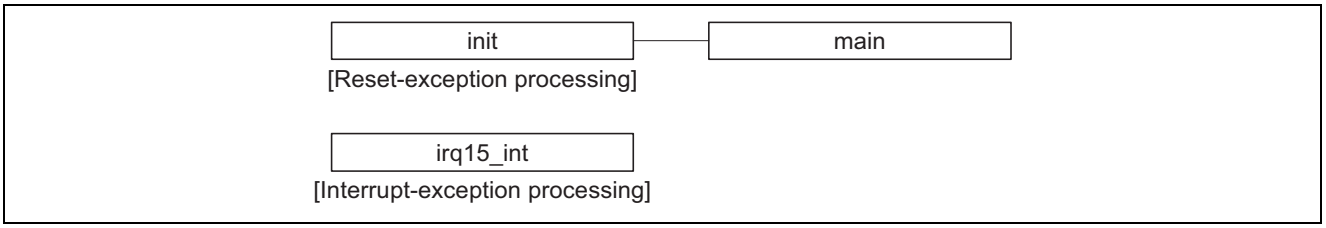


Figure 3 Hierarchical Structure of Function Calls

5.3 RAM Usage

Table 7 RAM Usage

Type	Variable Name	Description	Used in (Functions)
unsigned char	TIME.HOUR	Hours counter of the TIME structure Range: 0 to 23 (1 byte)	main, irq15_int
unsigned char	TIME.MIN	Minutes counter of the TIME structure Range: 0 to 59 (1 byte)	main, irq15_int
unsigned char	TIME.SEG	Seconds counter of the TIME structure Range: 0 to 59 (1 byte)	main, irq15_int

5.4 Description of Functions

5.4.1 Function init

1. Functional overview
   Initialization routine. Releases the required modules from module-stop mode, makes clock settings, and calls the main function.
2. Arguments
   None
3. Return value
   None
4. Description of employed internal registers
   The internal registers used in the sample application are listed below. Note that the settings below are for this sample task and are not the initial values.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
15	MDS7	—*	R	Indicates the value set by mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. This latching is released by a reset.
11	MDS3	—*	R	Mode Select 3 to 0 These bits indicate the operating mode selected by the mode pins (MD2 to MD0) (see table 8). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. These latches are released by a reset.
10	MDS2	—*	R	
9	MDS1	—*	R	
8	MDS0	—*	R	

Note: * Determined by pins MD3 to MD0.

Table 8 Setting of Bits MDS3 to MDS0

MCU Operating Mode	Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock provided to
8	ICK0	1	R/W	the CPU, DMAC, and DTC. 001: Input clock × 2
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 2

- MSTPCRA, MSTPCRB, and MSTPCRC control the module stop state. Setting a bit to 1 makes the corresponding module enter the module stop state, while clearing the bit to 0 clears the module stop state.

- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Target Module
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current consumption by stopping the bus controller and I/O ports operations when the CPU executes the SLEEP instruction after the module stop state has been set for all the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled. 1: All-module-clock-stop mode enabled.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timers (TMR_3 and TMR_2)
8	MSTPA8	1	R/W	8-bit timers (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

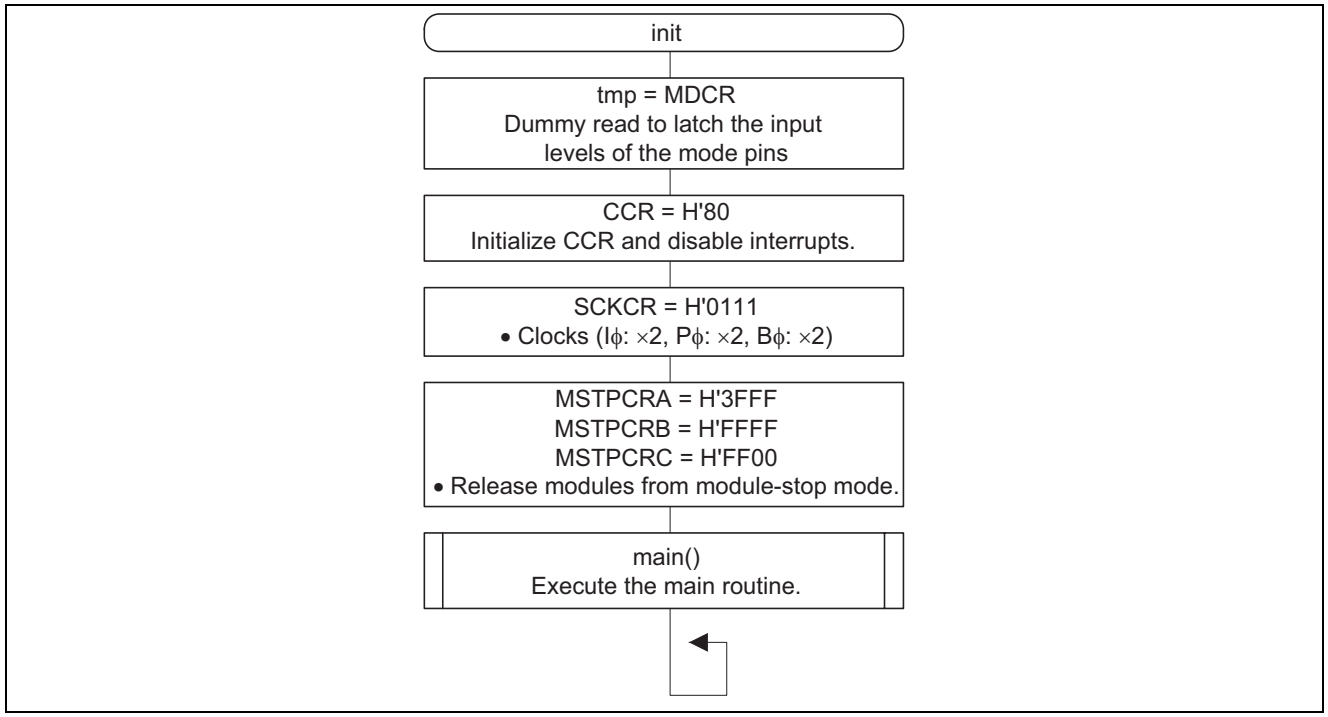
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Target Module
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface 1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface 0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Target Module
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart



5.4.2 Function main

1. Functional overview
   Main routine. Sets the overflow period for TM32K to one second and sets the 32K-timer interrupt (IRQ15 interrupt). After starting the 32K timer, initiates a transition to software-standby mode.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in the sample application are listed below. Note that the settings below are for this sample task and are not the initial values.

- Timer control register_3 (TCR32K) Number of bits: 8 Address: H'FFFABC

Bit	Bit Name	Setting	R/W	Description
5	TME	0/1	R/W	Timer Enable When this bit is set to 1, TCNT32K starts counting. When this bit is cleared, TCNT32K stops counting and is initialized to H'00.
2	OSC32STP*	0	R/W	32-kHz Oscillator Stop 0: Starts the 32-kHz oscillator 1: Stops the 32-kHz oscillator
1	CKS1	1	R/W	Clock Select 1, 0
0	CKS0	0	R/W	Select the clock source to be input to TCNT32K. The overflow cycle for SUBCK = 32.768 kHz is indicated in parentheses. 00: Clock SUBCK/32 (cycle: 250 ms) 01: Clock SUBCK/64 (cycle: 500 ms) 10: Clock SUBCK/128 (cycle: 1 s) 11: Clock SUBCK/512 (cycle: 2 s)

Note: * When the CK32K bit in SUBCKCR is 1, 1 cannot be written to this bit.

- Timer control register_3 (TCR32K) Number of bits: 8 Address: H'FFFABD

  Function: TCR32K is a readable up-counter. When the TME bit in the timer control register (TCR32K) is 0, TCNT32K is initialized to H'00.

- Software standby release IRQ enable register (SSIER) Number of bits: 16 Address: H'FFFBCE

Bit	Bit Name	Setting	R/W	Description
15	SSI15	0	R/W	Software Standby Release IRQ Setting This bit selects the IRQ15 interrupt used to leave software standby mode. 0: An IRQ15 request is not sampled in software standby mode 1: When an IR15 request occurs in software standby mode, this LSI leaves software standby mode after the oscillation settling time has elapsed

- IRQ sense control register H (ISCRH) Number of bits: 16 Address: H'FFFD68

Bit	Bit Name	Setting	R/W	Description
15	IRQ15SR	0	R/W	IRQ15 Sense Control Rise
14	IRQ15SF	1	R/W	IRQ15 Sense Control Fall IRQ15 is used as the 32KOVI interrupt in the TM32K. Make settings so that IRQ15 is generated on falling edge of $\overline{\text{IRQ15}}$. 01: Interrupt request generated on falling edge of $\overline{\text{IRQ15}}$

- Standby control register (SBYCR) Number of bits: 16 Address: H'FFFDC6

Bit	Bit Name	Setting	R/W	Description
15	SSBY	0	R/W	Software Standby Specifies the transition mode after executing the SLEEP instruction 0: Shifts to sleep mode after the SLEEP instruction is executed 1: Shifts to software standby mode after the SLEEP instruction is executed This bit remains the reset state when clearing the software standby mode by using external interrupts and shifting to normal operation. For clearing, write 0 to this bit. When the WDT is used as the watchdog timer, the setting of this bit is disabled. In this case, a transition is always made to sleep mode or all-module-clock-stop mode after the SLEEP instruction is executed. When the SLPIE bit is set to 1, this bit should be cleared to 0.
12	STS4	0	R/W	Standby Timer Select 4 to 0 These bits select the time the MCU waits for the clock to settle when software standby mode is cleared by an external interrupt or when a transition is made from the subclock operation to the main clock operation. For a crystal oscillator, make a selection according to the operating frequency so that the standby time is longer than the oscillation settling time. With an external clock, a PLL circuit settling time is necessary. While oscillation is being settled, the timer is counted on the Pϕ clock frequency. Careful consideration is required in multi-clock mode. 00110: Standby time = 512 states (Setting time in the case of subclock frequency (Pϕ) = 32.768 kHz)
11	STS3	0	R/W	
10	STS2	1	R/W	
9	STS1	1	R/W	
8	STS0	0	R/W	

- Subclock control register (SUBCKCR) Number of bits: 8 Address: H'FFFDCF

Bit	Bit Name	Setting	R/W	Description
2	EXSTP	1	R/W	Main Clock Oscillation Stop 0: The main clock oscillator and PLL remain active during subclock operation, but are stopped in standby mode. 1: The main clock oscillator and PLL are stopped during subclock operation.
1	WAKE32K	1	R/W	Wakeup Clock Select Selects the operating clock for use as the system clock when transition has been made from subclock operation to software standby mode and then the CPU returns from the software standby mode by an interrupt. 0: On leaving software standby mode, the main clock is the operating clock. 1: On leaving software standby mode, the subclock is the operating clock. This setting is valid when bit 0 (CK32K) is 1.
0	CK32K	1	R/W	Subclock Select 0: The system clock (Iϕ), peripheral module clock (Pϕ), and external bus clock (Bϕ) operate on the main clock. 1: The system clock (Iϕ), peripheral module clock (Pϕ), and external bus clock (Bϕ) operate on the subclock. When the OSC32STP bit in TCR32K is 1, 1 cannot be written to this bit. This bit is cleared to 0 when clearing software standby mode while the value of WAKE32K is 0. Dummy read of this bit must be performed twice immediately after this bit is written to.

- IRQ enable register (IER) Number of bits: 16 Address: H'FFFF34

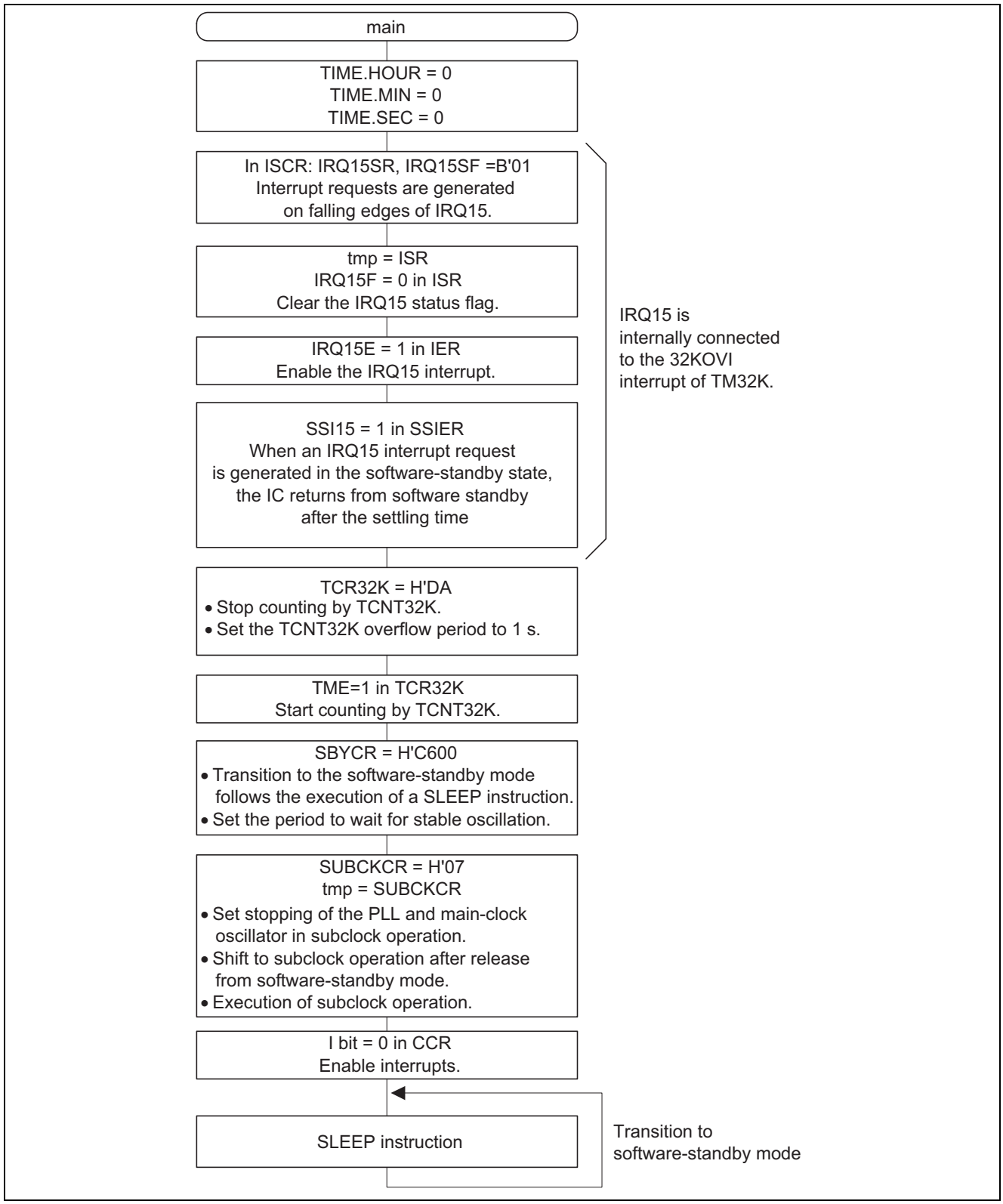
Bit	Bit Name	Setting	R/W	Description
15	IRQ15E	1	R/W	IRQ15 Enable IRQ15 is internally connected to the 32KOVI interrupt in the TM32K. 0: IRQ15 interrupt disabled 1: IRQ15 interrupt enabled

- IRQ status register (ISR) Number of bits: 16 Address: H'FFFF36

Bit	Bit Name	Setting	R/W	Description
15	IRQ15F	0	R/(W)*	[Setting condition] • When the interrupt selected by ISCR occurs [Clearing conditions] • Writing 0 after reading 1 • When IRQ15 interrupt exception handling is executed while falling-edge sensing is selected

Note: * Only 0 can be written, to clear the flag.

5. Flowchart


main
TIME.HOUR = 0
TIME.MIN = 0
TIME.SEC = 0
In ISCR: IRQ15SR, IRQ15SF =B'01
Interrupt requests are generated
on falling edges of IRQ15.
tmp = ISR
IRQ15F = 0 in ISR
Clear the IRQ15 status flag.
IRQ15E = 1 in IER
Enable the IRQ15 interrupt.
SSI15 = 1 in SSIER
When an IRQ15 interrupt request
is generated in the software-standby state,
the IC returns from software standby
after the settling time
IRQ15 is
internally connected
to the 32KOVI
interrupt of TM32K.
TCR32K = H'DA
• Stop counting by TCNT32K.
• Set the TCNT32K overflow period to 1 s.
TME=1 in TCR32K
Start counting by TCNT32K.
SBYCR = H'C600
• Transition to the software-standby mode
follows the execution of a SLEEP instruction.
• Set the period to wait for stable oscillation.
SUBCKCR = H'07
tmp = SUBCKCR
• Set stopping of the PLL and main-clock
oscillator in subclock operation.
• Shift to subclock operation after release
from software-standby mode.
• Execution of subclock operation.
I bit = 0 in CCR
Enable interrupts.
SLEEP instruction
Transition to
software-standby mode

5.4.3 Function irq15_int

1. Functional overview
   Processing routine for 32K-timer interrupts (IRQ15 interrupt processing). Clears the IRQ15 interrupt flag and stores the time in the SEC, MIN, and HOUR members of the TIME structure.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in the sample application are listed below. Note that the settings below are for this sample task and are not the initial values.

- IRQ status register (ISR) Number of bits: 16 Address: H'FFFF36

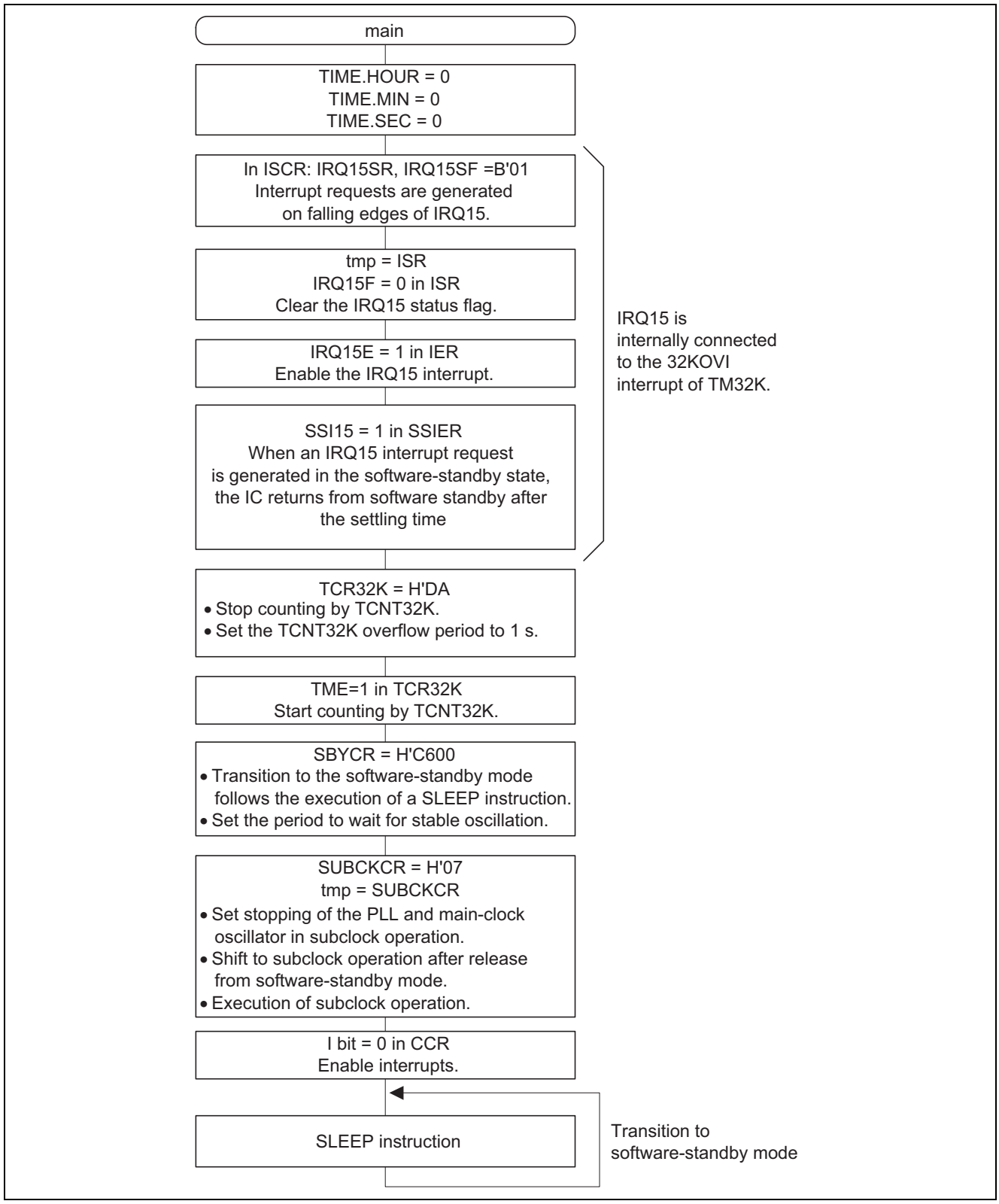
Bit	Bit Name	Setting	R/W	Description
15	IRQ15F	0	R/(W)*	[Setting condition] • When the interrupt selected by ISCR occurs [Clearing conditions] • Writing 0 after reading 1 • When IRQ15 interrupt exception handling is executed while falling-edge sensing is selected

Note: * Only 0 can be written, to clear the flag.

- Subclock control register (SUBCKCR) Number of bits: 8 Address: H'FFFDCF

Bit	Bit Name	Setting	R/W	Description
0	CK32K	1	R/W	Subclock Select 0: The system clock (Iϕ), peripheral module clock (Pϕ), and external bus clock (Bϕ) operate on the main clock. 1: The system clock (Iϕ), peripheral module clock (Pϕ), and external bus clock (Bϕ) operate on the subclock. When the OSC32STP bit in TCR32K is 1, 1 cannot be written to this bit. This bit is cleared to 0 when clearing software standby mode while the value of WAKE32K is 0. Dummy read of this bit must be performed twice immediately after this bit is written to.

5. Flowchart


main
TIME.HOUR = 0
TIME.MIN = 0
TIME.SEC = 0
In ISCR: IRQ15SR, IRQ15SF =B'01
Interrupt requests are generated
on falling edges of IRQ15.
tmp = ISR
IRQ15F = 0 in ISR
Clear the IRQ15 status flag.
IRQ15E = 1 in IER
Enable the IRQ15 interrupt.
SSI15 = 1 in SSIER
When an IRQ15 interrupt request
is generated in the software-standby state,
the IC returns from software standby after
the settling time
IRQ15 is
internally connected
to the 32KOVI
interrupt of TM32K.
TCR32K = H'DA
• Stop counting by TCNT32K.
• Set the TCNT32K overflow period to 1 s.
TME=1 in TCR32K
Start counting by TCNT32K.
SBYCR = H'C600
• Transition to the software-standby mode
follows the execution of a SLEEP instruction.
• Set the period to wait for stable oscillation.
SUBCKCR = H'07
tmp = SUBCKCR
• Set stopping of the PLL and main-clock
oscillator in subclock operation.
• Shift to subclock operation after release
from software-standby mode.
• Execution of subclock operation.
I bit = 0 in CCR
Enable interrupts.
SLEEP instruction
Transition to
software-standby mode

6. Documents for Reference

- Hardware Manual
  H8SX/1663 Group Hardware Manual
  The most up-to-date versions of these documents are available on the Renesas Technology Website.
- Technical News/Technical Update
  The most up-to-date information is available on the Renesas Technology Website.

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