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H8/300L Series

Using the 14-Bit PWM Function to Generate Variable-Duty-Cycle Pulse Output

Introduction

14-bit PWM function is used to output 75.4 % of duty-cycle pulse from the PWM output pin.

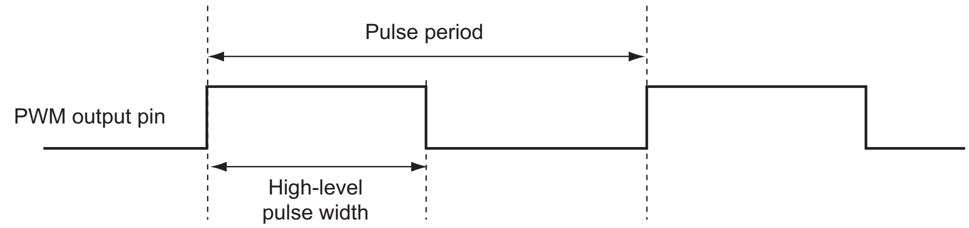
Target Device

H8/3644

Contents

1. Specifications

1. As shown in figure 1, the 14-bit PWM function is used to output a variable-duty-cycle pulse from the PWM output pin.
2. In this sample task, 75.4 % of duty-cycle pulse is output with a 102.4 µs of pulse cycle, and a 77.2 µs of pulse high width.



$$\text{Duty cycle} = \frac{\text{Pulse high width}}{\text{Pulse cycle}} \times 100\ (\%)$$

Figure 1 Duty Cycle Pulse Output By 14-Bit PWM Function

2. Description of Functions Used

1. In this sample task, the 14-bit PWM function is used to output a variable-duty-cycle pulse from the PWM output pin.
   a. Figure 2 is a block diagram of the 14-bit PWM function. The elements of the block diagram are described below.
      - The system clock (ϕ) is a 5-MHz clock that is generated by dividing a 10-MHz OSC clock by two. The system clock is used as a reference clock for operating the CPU and peripheral functions.
      - The PWM control register (PWCR) is an 8-bit write-only register that selects an input clock. The input clock can be selected as one of two conversion cycles: a conversion cycle of 32.768/ϕ with minimum change width of 2/ϕ or a conversion cycle of 16.384/ϕ with minimum change width of 1/ϕ.
      - The PWM function uses the pulse division method to reduce ripples.
      - The PWM data registers U and L (PWDRU and PWDRL) are a 14-bit write-only register where the upper 6 bits function as PWDRU and the lower 8 bits function as PWDRL. Data written to PWDRU and PWDRL corresponds to the total of high level widths of one PWM waveform cycle. When data is written to the 14 bits of PWDRU and PWDRL, the contents of PWDRU and PWDRL are fetched into the PWM waveform generator to change PWM waveform generation data. Note that 14-bit data should be written to the lower 8 bits of PWDRU and then to the upper 6 bits of PWDRL in this order.
      - The port mode register 1 (PMR1) is an 8-bit readable/writable register that controls the function switching of pins in port 1. The $P1_4$/PWM pin can function as PWM output pin by selecting the PWM pin function via bit 4 ($P1_4$/PWM pin function switching bit) of PMR1.
      - The PWM output pin (PWM) outputs a PWM waveform of a pulse division method.

Note: When a PWM waveform is output using the 14-bit PWM function used in this sample task, a correct PWM waveform may not be output depending on the PWM register rewrite timing.

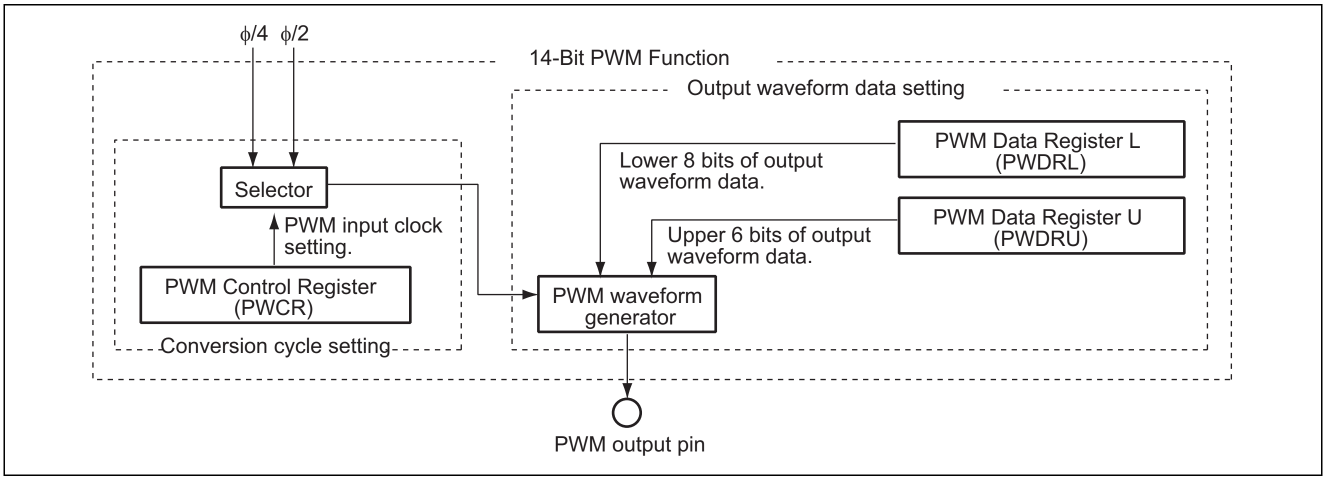


Figure 2 Block Diagram of 14-Bit PWM Function

2. Table 1 lists the function allocation for this sample task. The functions listed in table 1 are allocated so that a variable-duty-cycle pulse is output by the 14-bit PWM function.

Table 1 Function Allocation

Function	Description
PWCR	Selects a clock to be provided to the 14-bit PWM
PWDRU	Sets the upper 6 bits of PWM output waveform data
PWDRL	Sets the lower 8 bits of PWM output waveform data
PWM	PWM waveform output pin

3. Principle of Operation

1. Figure 3 illustrates the principle of operation of this sample task. The hardware and software processing shown in figure 3 applies the 14-bit PWM function to output a variable-duty-cycle pulse.

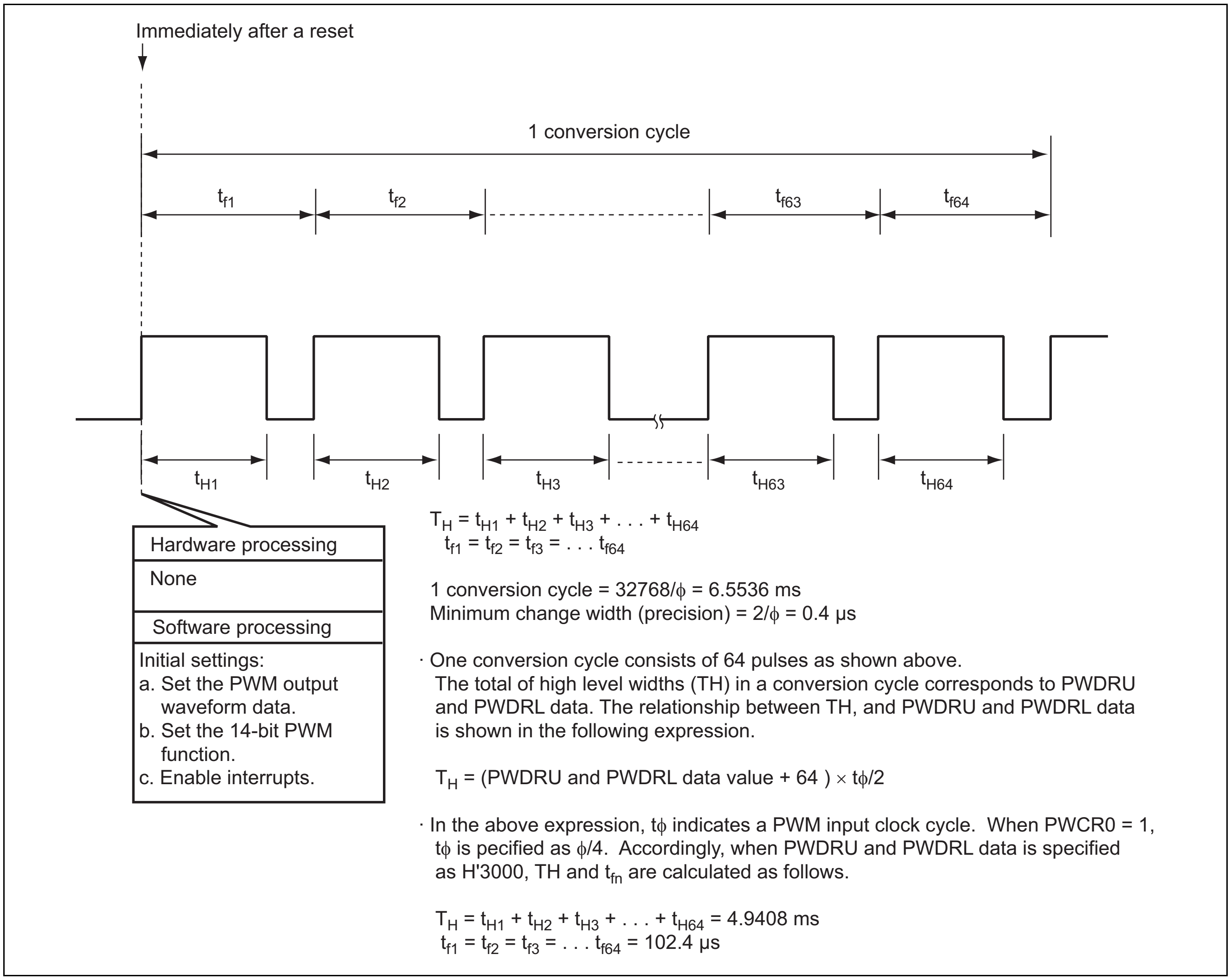


Figure 3 Operation Principle of duty-cycle pulse Output by 14-Bit PWM Function

4. Description of Software

4.1 Modules

Table 2 describes the module used in this sample task.

Table 2 Description of Modules

Module	Label	Function
Main routine	MAIN	Initializes the stack pointer, sets the 14-bit PWM function, and enables interrupts

4.2 Arguments

Table 3 describes the arguments used in this sample task.

Table 3 Description of Arguments

Argument	Function	Used in	Data Size	Input/ Output
R1H	Upper 6 bits of PWM output waveform data to be set in PWDRU	Main routine	1 byte	Input
R1L	Lower 8 bits of PWM output waveform data to be set in PWDRL	Main routine	1 byte	Input

4.3 Internal Registers

Table 4 describes the functions of internal registers used in this sample task.

Table 4 Description of Internal Registers

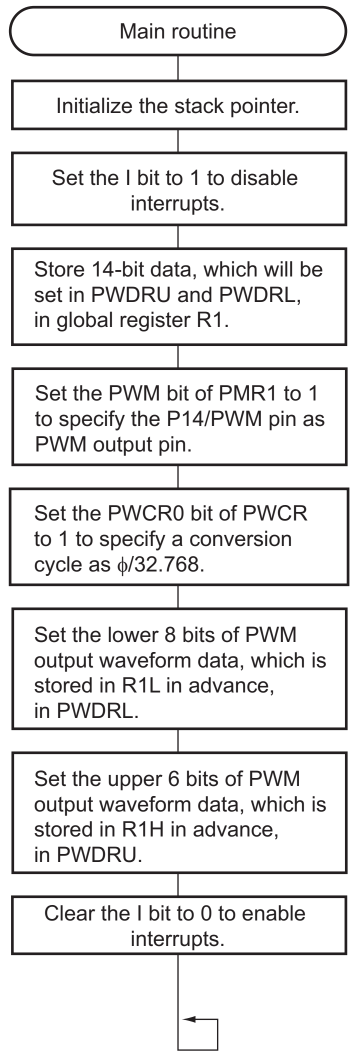
Register		Function	Address	Setting
PWCR	PWCR0	PWM control register (Clock select 0) PWCR0 = 1: Sets a clock to be provided to the 14-bit PWM as ϕ/4	H'FFD0 Bit 0	1
PWDRU		PWM data register U Sets the upper 6 bits of PWM output waveform data	H'FFD1	H'30
PWDRL		PWM data register L Sets the lower 8 bits of PWM output waveform data	H'FFD2	H'00
PMR1	PWM	Port mode register 1 (P14/PWM pin function switching) PWM = 1: Sets the P14/PWM pin as PWM output pin.	H'FFFC Bit 4	1

4.4 RAM

This sample task does not use RAM.

5. Flowchart

1. Main routine



6. Program Listing

```
;*************************************************************************************************
;*                                                                                              *
;*      H8/300L Series -H8/3644,H8/3657-                                                        *
;*      Application Note                                                                        *
;*                                                                                              *
;*      'Duty Pulse Output by 14-bit PWM Function'                                              *
;*                                                                                              *
;*      Function                                                                                *
;*      : 14bit PWM                                                                             *
;*                                                                                              *
;*      External Clock : 10MHz                                                                  *
;*      Internal Clock : 5MHz                                                                   *
;*      Sub Clock :      32.768kHz                                                              *
;*                                                                                              *
;*************************************************************************************************
;
          .cpu          300L
;
;*************************************************************************************************
;*  Symbol Defnition                                                                            *
;*************************************************************************************************
;
PWCR      .equ          H'FFD0                        ;PWM Control Register
PWCR0     .bequ         0,PWCR                        ;Clock Select
PWDRU     .equ          H'FFD1                        ;PWM Data Register U
PWDRL     .equ          H'FFD2                        ;PWM Data Register L
PMR1      .equ          H'FFFC                        ;Port Mode Register 1
PWM       .bequ         4,PMR1                        ;P14/PWM Terminal Function Change
;
;*************************************************************************************************
;*  Ram Allocation                                                                              *
;*************************************************************************************************
;
STACK     .equ          H'FF80                        ;Stack Pointer
;
;*************************************************************************************************
;*  Vector Address                                                                              *
;*************************************************************************************************
;
          .org          H'0000
          .DATA.W       MAIN                          ;Reset Interrupt
;
          .org          H'0008
          .data.w       MAIN                          ;IRQ0 Interrupt
          .data.w       MAIN                          ;IRQ1 Interrupt
          .data.w       MAIN                          ;IRQ2 Interrupt
          .data.w       MAIN                          ;IRQ3 Interrupt
          .data.w       MAIN                          ;INT0 - INT7 Interrupt
;
```

```
        .org        H'0014
        .data.w     MAIN                ;Timer A Interrupt
        .data.w     MAIN                ;Timer B1 Interrupt
;
        .org        H'0020
        .data.w     MAIN                ;Timer X Interrupt
        .data.w     MAIN                ;Timer V Interrupt
;
        .org        H'0026
        .data.w     MAIN                ;Sci1 Interrupt
;
        .org        H'002A
        .data.w     MAIN                ;Sci3 Interrupt
        .data.w     MAIN                ;A/D Converter Interrupt
        .data.w     MAIN                ;Sleep Interrupt
;
;***************************************************************************************************
;*  Main Program                                                                                   *
;***************************************************************************************************
;
        .org        H'1000
;
MAIN    .equ        $
        MOV.W       #STACK,SP           ;Initialize Stack Pointer
        ORC         #H'80,CCR           ;Interrupt Disable
;
        MOV.W       #H'3000,R1          ;Set 14-Bits PWM Output Pulse Data
;
        MOV.W       #H'14FF,R0
        MOV.B       R0H,@PMR1           ;Initialize PWM Output Terminal Function
        MOV.B       R0L,@PWCR           ;Initialize PWM Input Clock
;
        MOV.B       R1L,@PWDRL          ;Initialize PWM Output Pulse Data Higher
        MOV.B       R1H,@PWDRU          ;Initialize PWM Output Pulse Data Lower
;
        ANDC        #H'7F,CCR           ;Interrupt Enable
;
MAIN9   .equ        $
        BRA         MAIN9
;
        .end
```

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Revision Record

Rev.	Date	Description	
		Page	Summary
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2.00	Nov.30.06	All pages	Content correction

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