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SH7080 Series

User Program Mode (UART) Function

Introduction

The SH7080 has three on-board programming modes: boot mode, user boot mode, and user program mode. The user program mode provides for the erasure and programming of flash memory through a desired interface. This application describes how to erase and program the flash memory in the user program mode during execution of a user application when the flash reprogramming commands are received from a UART (Universal Asynchronous Receiver/Transmitter). The information has been collected for reference to help in the design of user software.

Target Device

SH7086

Contents

1. Specifications

In this sample application, the user program mode is employed to erase and program on-chip flash memory while a user application program is being executed. Serial transfer with the UART of a host system (PC) is employed, and the flash memory is placed in the programmable state by when reception of the corresponding command from the host (PC) is detected. Figure 1 shows the basic specifications of this sample application.

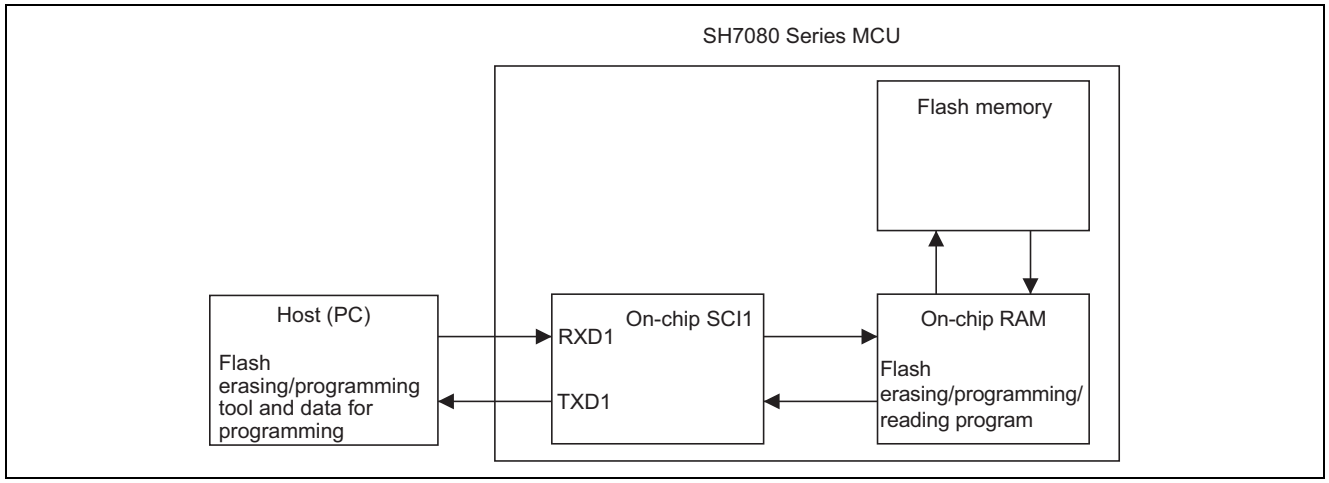


Figure 1 Erasing and Programming Flash Memory in User Program Mode

2. Applicable Conditions

Applicable conditions for this application sample are shown in table 1.

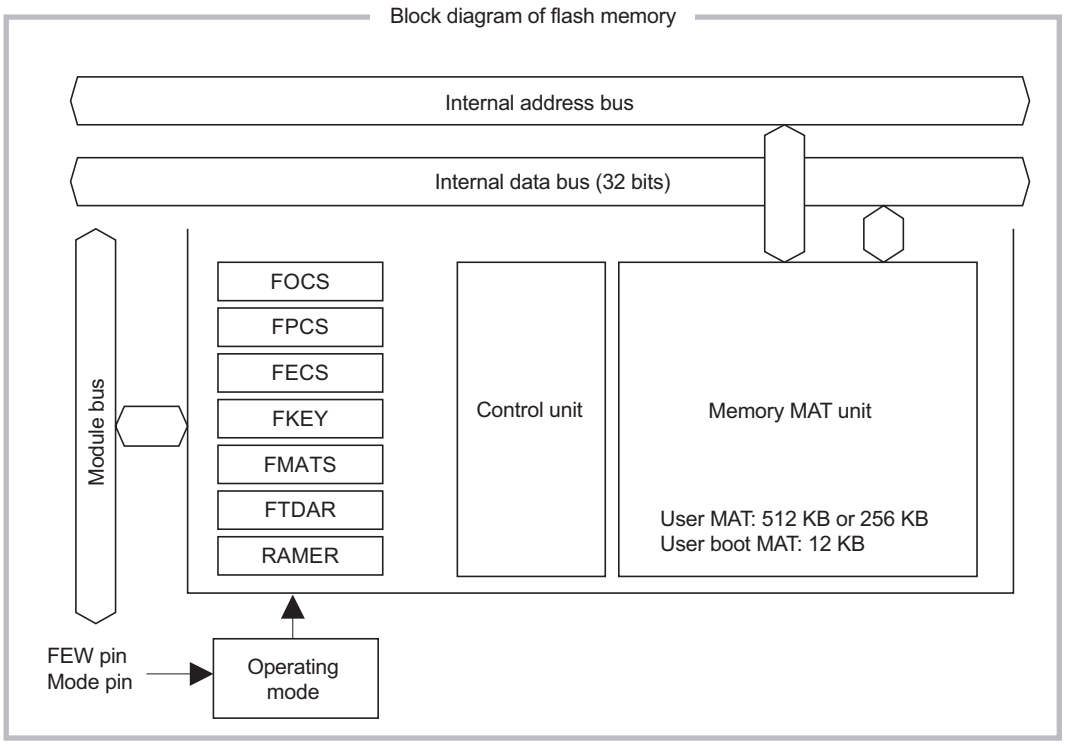
Table 1 Applicable Conditions

Item	Setting	
Device	SH7086 (R5F70865)	
Operating frequency	Internal clock	Iϕ= 20 MHz
	Bus clock	Bϕ=20 MHz
	Peripheral clock	Pϕ=20 MHz
	MTU2 clock	MPϕ= 20 MHz
	MTU2S clock	MIϕ=20 MHz
Device operating mode	Single-chip mode	
Development environment	High-performance Embedded Workshop Ver.4.03.00.001 SuperH RISC engine Standard Toolchain (V.9.1.0.0) SuperH RISC engine C/C++ Compiler (V.9.01.00) (manufactured by Renesas Technology)	
C compiler option	High-performance Embedded Workshop default setting -cpu=sh2 -include="$(WORKSPDIR)\inc" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo	

3. Description of Modules Used

3.1 Flash Memory

A block diagram of flash memory is shown in figure 2.



[Legend]
FCCS: Flash code control and status register
FPCS: Flash program code select register
FECS: Flash erase code select register
FKEY: Flash key code register
FMATS: Flash MAT select register
FTDAR: Flash transfer destination address register
RAMER: RAM emulation register

Figure 2 Block Diagram of Flash Memory

- Flash code control and status register (FCCS)
  FCCS is configured by bits which request the monitor of the FWE pin state and for error occurrence during programming or erasing flash memory and the download of the on-chip program.

- Flash program code select register (FPCS)
  FPCS selects the on-chip programming program to be downloaded.

- Flash erase code select register (FECS)
  FECS selects download of the on-chip erasing program.

- Flash key code register (FKEY)
  FKEY is a register for software protection that enables download of the on-chip program and programming/erasing of flash memory. Before setting the SCO bit to 1 in order to download the on-chip program or executing the downloaded programming/erasing program, each processing cannot be executed if the key code is not written.

- Flash MAT select register (FMATS)
  FMATS specifies whether user MAT or user boot MAT is selected.

- Flash transfer destination address register (FTDAR)
  FTDAR specifies the on-chip RAM address to which the on-chip program is downloaded. Make settings for FTDAR before writing 1 to the SCO bit in FCCS. The initial value is H'00 which points to the start address (H'FFFF9000) in on-chip RAM.

Note: For details regarding operational specification of each register, see the section on flash memory in SH7080 Series Hardware Manual.

3.2 Programming/Erasing Interface Parameters

The programming/erasing interface parameters specify the operating frequency, user branch destination address, storage place for program data, programming destination address, and erase block and exchanges the processing result for the downloaded on-chip program. The programming/erasing interface parameters are used in the following four items.

1. Download control
2. Initialization before programming or erasing
3. Programming
4. Erasing

Table 2 Usable Parameters and Target Modes

Parameter Name	Abbreviation	Download	Initialization	Programming	Erasure	Allocation
Download pass/fail result	DPFR	✓	—	—	—	On-chip RAM
Flash pass/fail result	FPFR1*	—	✓	✓	✓	R0 of CPU
Flash programming/erasing frequency control	FPEFEQ	—	✓	—	—	R4 of CPU
Flash user branch address set	FUBRA	—	✓	—	—	R5 of CPU
Flash multipurpose address area	FMPAR	—	—	✓	—	R5 of CPU
Flash multipurpose data destination area	FMPDR	—	—	✓	—	R4 of CPU
Flash erase block select	FEBS	—	—	—	✓	R4 of CPU

Note: For details regarding operational specification of each register, see the section flash memory in SH7080 Series Hardware Manual.

* The processing results of initialization, programming, and erasing and returned, but bit contents have different meanings according to the processing program. Every parameter in the table is readable/writable and has an undefined initial value.

3.3 Specifications of Flash Erasing/Programming

In this sample application, the user application is stored in the first block (EB0) of the user MAT (addresses H'0000000 to H'00000FFF). The first area in the on-chip RAM (addresses H'FFFF4000 to H'FFFF47FF) is used as a data area (storage for variables). The user application consists of a vector table, communications program, and the procedure program for reprogramming of flash memory.

The target area of flash memory for reprogramming is the user MAT area other than the area for storing the user application, i.e. the region starting with block EB1 at H'0001000. The flash memory is switched from the user program execution state to a reprogrammable state (user program mode). The procedure program for erasing and programming is copied from the flash memory to the region of on-chip RAM (addresses H'FFFF4800 to H'FFFF48FF) from which it will be executed. Addresses H'FFFF9000 to H'FFFFAFFF in the on-chip RAM is used as an area for downloading the specific programs to handle erasing and programming (erasing program and programming program).

The flash erasing/programming specifications are illustrated in figure 3. The memory map of the user MAT and on-chip RAM is shown in figure 4.

Figure 3 Flash Erasing/Programming Specifications

User MAT		
H'0000 0000 to 0000 03DF		Vector table
H'0000 0400 to 0000 05FF		User application
H'0000 0600 to 0000 07FF		SCI1 communications program
H'0000 0800 to 0000 0FFF		Procedure program storage area
H'0000 1000 to 0007 FFFF		Target area for reprogramming
On-chip RAM		
H'FFFF 4000 to FFFF 47FF		Data area
H'FFFF 4800 to FFFF 8FFF		Procedure program execution area
H'FFFF 9000 to FFFF 9FFF		Erasing program download area
	0000	DPFR (Return value: 1 byte)
	0001 to 000F	System area (15 bytes)
	0010 to 001F	Entry point for erasure processing
	0020 to 002F	Entry point for erasure initialization
	0030 to 0FFF	Erasing initialization + erasing program
H'FFFF A000 to FFFF AFFF		Programming program download area
	0000	DPFR (Return value: 1 byte)
	0001 to 000F	System area (15 bytes)
	0010 to 001F	Entry point for programming processing
	0020 to 002F	Entry point for programming initialization
	0030 to 0FFF	Programming initialization + programming program

Figure 4 Memory Map of the User MAT and On-Chip RAM

4. Description of Operation

In this sample application, commands to control reading and programming/erasing of data in the on-chip flash memory are sent from a host (PC) via serial communications. The program waits for commands from the host (PC) after a reset.

1. Reading data from the on-chip flash memory

When the program receives a read command (CMD_READ) from the host (PC), it enters the state for reading out the on-chip flash memory. The program receives the address where it is to start reading and number of bytes from the host and then transmits the data from the specified area of on-chip flash memory to the host.

2. Erasing/reprogramming the on-chip flash memory

When the program receives the command to start reprogramming (CMD_GO) from the host (PC), it enters the state where the on-chip flash memory can be erased and reprogrammed. After receiving the reprogramming start command (CMD_GO), the program executes the erasing or programming initialization program. The on-chip flash memory is then erased and reprogrammed by erasing request (CMD_ERASE) and programming request (CMD_WRITE) commands from the host. This erasing and reprogramming of the on-chip flash memory should be executed from the on-chip RAM.

The command specifications are shown in table 3. The command control sequence in this sample application is shown in figure 5.

Table 3 Command Specifications

Command	Command Value	Description
CMD_GO	0x55	Starts reprogramming of flash memory
CMD_READ	0xAA	Reads flash memory
CMD_ERASE	0x77	Requests erasing of flash memory
CMD_WRITE	0x88	Requests programming of flash memory
CMD_WEND	0x99	Ends programming of flash memory
CMD_OK	0x00	OK (response to normal end)
CMD_NG	0x01	NG (response to abnormal end)
CMD_REQUEST	0x11	Request for transmission

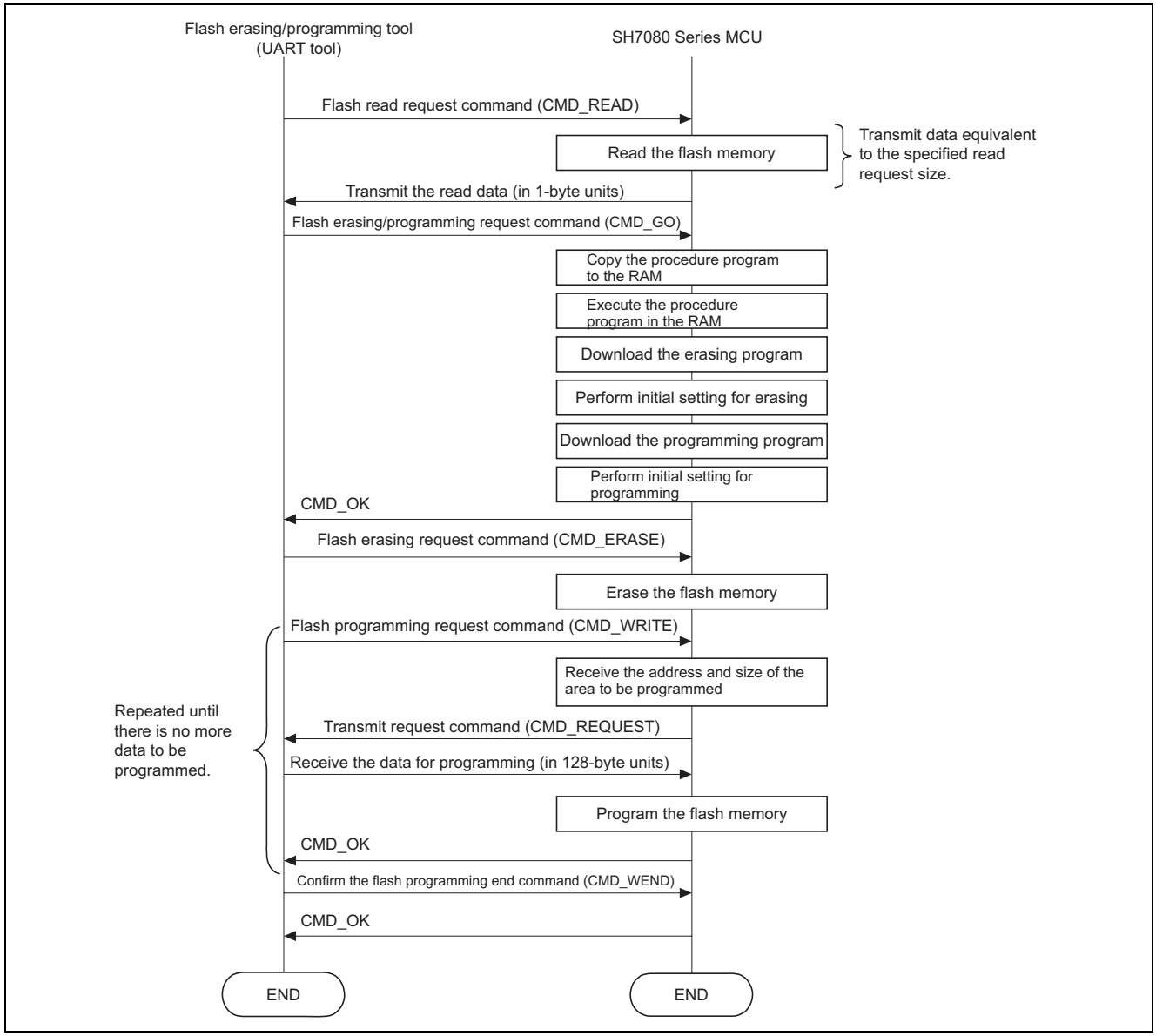


Figure 5 Control Sequence for Commands

5. Description of Software

5.1 Description of Functions

The functions used in this application sample are described in table 4.

Table 4 Description of Modules

Module Name	Label Name	File Name	Description
Main routine	main()	main.c	Initial setting of SCI ch1 Executes the user application program. Performs flash erasing/programming processing in response to requests for flash erasing/programming.
SCI channel 1 initial setting routine	com_init ()	sci.c	Handles SCIF transmit-FIFO-data-empty interrupts.
SCI1 receive data presence check routine	CheckRcv()		Checks whether received data are stored in SCRDR.
SCI1 n-byte reception routine	rcvnbyte()		Receives the specified number of bytes of data.
SCI1 1-byte transmission routine	trs1byte()		Writes 1 byte for serial output.
Erasing program download and initialization routine	SetupFlashErase()	flash.c	Downloads the erasing program into the RAM and performs initialization.
Flash erasing routine	FlashErase()		Erases the specified erase blocks in order from the EB0 block.
Programming program download and initialization routine	SetupFlashWrite()		Downloads the programming program into the RAM and performs initialization.
Flash programming routine	FlashWrite()		Writes data to the specified address.
Flash programming main routine	FlashMain()		Checks commands and performs erasing/programming.
Flash reading routine	FlashRead()		Reads the specified amount of flash memory starting from the specified address.

5.2 Variables Used

The variables used in this application sample are described in table 5.

Table 5 Variables Used

Variable and Label Name	Description	Used in
unsigned char WriteBuff[128]	Program data area	FlashMain ()
unsigned char flash_erase[2048]	Area for downloading the erasing program	SetupFlashErase()
unsigned char flash_write[2048]	Area for downloading the programming program	SetupFlashWrite()

5.3 Register Settings

This section describes the setting of registers used in this application sample. Note that the settings shown below are used in the sample task and are not initial values.

5.3.1 Register for Setting the Clock Pulse Generator (CPG)

- Frequency Control Register (FRQCR)
- This register specifies the division ratio of the frequency. The settings shown in the tables are the values used in this sample task and differ from the initial values.
  Setting: H'36DB

Bit	Bit Name	Value	Setting
15	—	0	Reserved
14 to 12	IFC2 to IFC0	011	Internal Clock (Iϕ) Frequency Division Ratio 011: × 1, 20 MHz when the input clock is 10 MHz
11 to 9	BFC2 to BFC0	011	Bus Clock (Bϕ) Frequency Division Ratio 011: × 1/4, 20 MHz when the input clock is 10 MHz
8 to 6	PFC2 to PFC0	011	Peripheral Clock (Pϕ) Frequency Division Ratio 011: × 1/4, 20 MHz when the input clock is 10 MHz
5 to 3	MIFC2 to MIFC0	011	MTU2S Clock (MIϕ) Frequency Division Ratio 011: × 1/4, 20 MHz when the input clock is 10 MHz
2 to 0	MPFC2 to MPFC0	011	MTU2 Clock (MPϕ) Frequency Division Ratio 011: × 1/4, 20 MHz when the input clock is 10 MHz

Note: When reprogramming flash memory, the procedure program must be executed from an area other than the flash memory to be programmed. In particular, the part where the SCO bit in FCCS is set to 1 for downloading of the procedure program to the on-chip RAM must be executed from the on-chip RAM. In the frequency control register (FRQCR), specify the frequency division ratios of the internal clock (Iϕ), bus clock (Bϕ), and peripheral clock (Pϕ) as 1/4 (initial value). After the programming/erasing program has been downloaded and the SCO bit is cleared to 0, the setting of the frequency control register (FRQCR) can be changed to the desired value.
For details on the specifications, see the section on flash memory in SH7080 Series Hardware Manual.

5.3.2 Setting the Power-Down Mode

- Standby Control Register 3 (STBCR3)
  This register controls the operation of modules in power-down mode.
  Setting: H'EF

Bit	Bit Name	Value	Setting
7	MSTP15	1	1: Clock signal supplied to I^2C2 is halted.
6	MSTP14	1	1: Clock signal supplied to SCIF is halted.
5	MSTP13	1	1: Clock signal supplied to SCI_2 is halted.
4	MSTP12	0	0: Clock signal is supplied (SCI_1 operates).
3	MSTP11	1	1: Clock signal supplied to SCI_0 is halted.
2	MSTP10	1	1: Clock signal supplied to SSU is halted.
1, 0	—	11	Reserved

5.3.3 Setting the Synchronous Serial Communication Interface ch1 (SCI1)

- Serial Control Register (SCSCR)
  This register selects transmission and reception by the SCI, enables or disables interrupt requests, and selects the clock source for transmission and reception.
  Setting: H'30

Bit	Bit Name	Value	Setting
7	TIE	1	0: Transmit-FIFO-data-empty interrupt request (TXI) is disabled 1: Transmit-FIFO-data-empty interrupt request (TXI) is enabled
6	RIE	0	0: Receive-data-full interrupt (RXIF), receive-error interrupt (ERIF), and break interrupt (BRIF) requests are disabled
5	TE	1	0: Transmission disabled 1: Transmission enabled
4	RE	0	0: Reception disabled
3	REIE	0	0: Receive-error interrupt (ERIF) and break interrupt (BRIF) requests are disabled
2	—	0	Reserved
1, 0	CKE1 and CKE0	00	00: Internal clock, SCK pin used for input pin (The input signal is ignored.

- Serial Mode Register (SCSMR)
  This register specifies the SCI serial communication format and selects the clock source for the baud rate generator.
  Setting: H'00

Bit	Bit Name	Value	Setting
7	C/$\overline{A}$	0	0: Asynchronous mode
6	CHR	0	0: 8-bit data
5	PE	0	0: Parity bit not added or checked
4	O/$\overline{E}$	0	0: The O/$\overline{E}$ bit is ignored because PE=0.
3	STOP	0	0: One stop bit
2	—	0	Reserved
1, 0	CKS1 and CKS0	00	00: Pϕ clock

- Bit Rate Register (SCBRR)
  This register determines the serial transmit/receive bit rate.
  Setting: 64 (H'40)

Bit	Bit Name	Value	Setting
7 to 0	—	0100 0000	Bit rate for serial transmission and reception

5.3.4 Registers for Setting the Pin Function Controller (PFC)

- Port A I/O Register L (PAIORL)
  This register selects the input direction for the pins of port A.
  Setting: H'0010

Bit	Bit Name	Value	Setting
15	PA15IOR	0	0: PA15 input
14	PA14IOR	0	0: PA14 input
13	PA13IOR	0	0: PA13 input
12	PA12IOR	0	0: PA12 input
11	PA11IOR	0	0: PA11 input
10	PA10IOR	0	0: PA10 input
9	PA9IOR	0	0: PA9 input
8	PA8IOR	0	0: PA8 input
7	PA7IOR	0	0: PA7 input
6	PA6IOR	0	0: PA6 input
5	PA5IOR	0	0: PA5 input
4	PA4IOR	1	0: PA4 output, TXD1 pin
3	PA3IOR	0	0: PA3 input, RXD1 pin
2	PA2IOR	0	0: PA2 input
1	PA1IOR	0	0: PA1 input
0	Pa0IOR	0	0: PA0 input

- Port A Control Register L2(PACRL2)
  This register selects the functions of multiplexed pins of port A.
  Setting: H'0001

Bit	Bit Name	Value	Setting
15	—	0	Reserved
14 to 12	PA7MD2 to PA7MD0	000	000: PA7 input/output (port)
11	—	0	Reserved
10 to 8	PA6MD2 to PA6MD0	000	000: PA6 input/output (port)
7	—	0	Reserved
6 to 4	PA5MD2 to PA5MD0	000	000: PA6 input/output (port)
3	—	0	Reserved
2 to 0	PA4MD2 to PA4MD0	001	001: TXD1 output (SCI)

- Port A Control Register L1 (PACRL1)
  This register selects the functions of multiplexed pins in port A.
  Setting: H'1000

Bit	Bit Name	Value	Setting
15	—	0	Reserved
14 to 12	PA3MD2 to PA3MD0	001	001: RXD1 input (SCI)
11	—	0	Reserved
10 to 8	PA2MD2 to PA2MD0	000	000: PA2 input/output (port)
7	—	0	Reserved
6 to 4	PA1MD2 to PA1MD0	000	000: PA1 input/output (port)
3	—	0	Reserved
2 to 0	PA0MD2 to 0	000	000: PA0 input/output (port)

6. Flowcharts

The process flows in this application sample are given below.

6.1 Main Routine

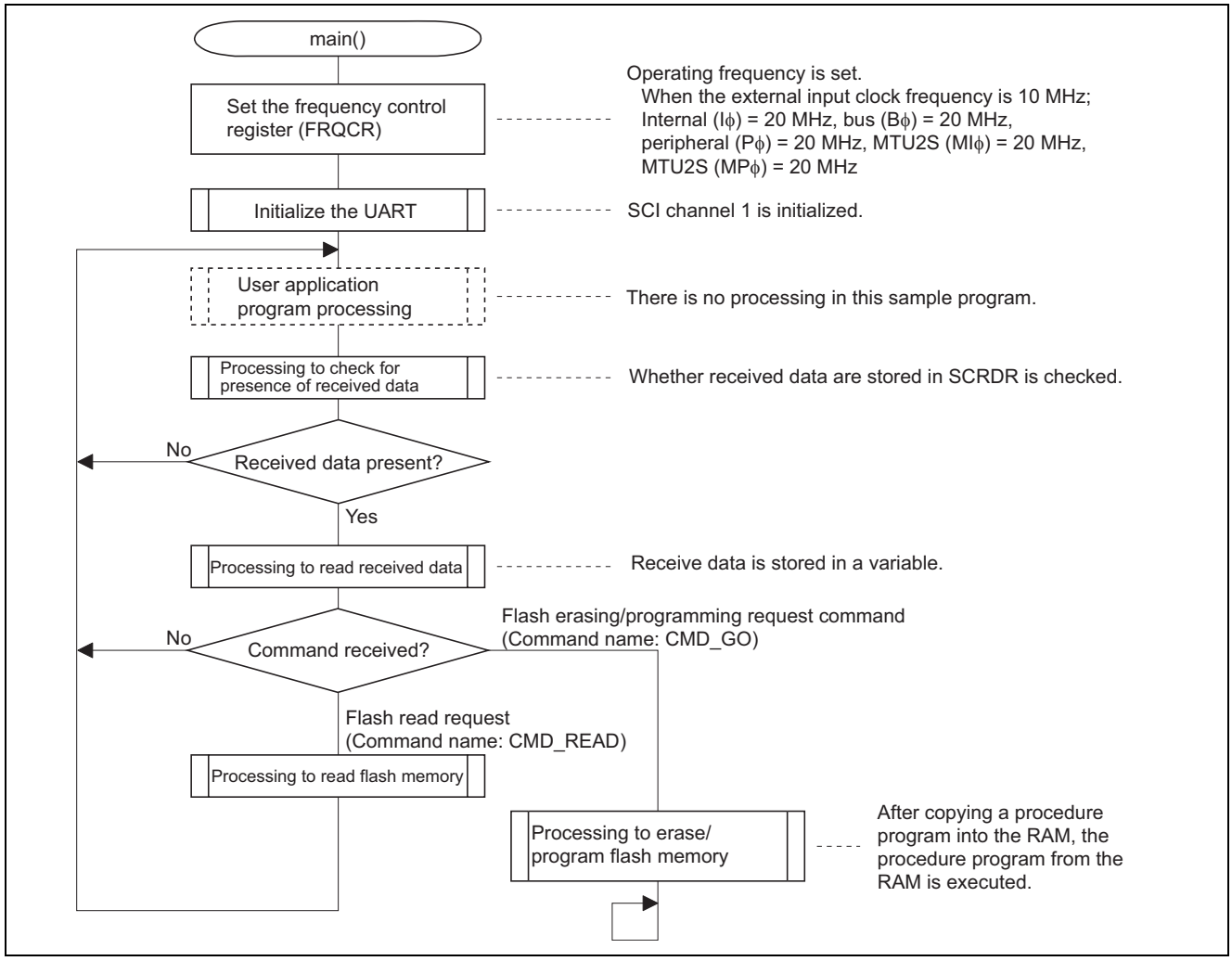


Figure 6 Main Routine Processing

6.2 SCI Channel 1 Initialization Routine

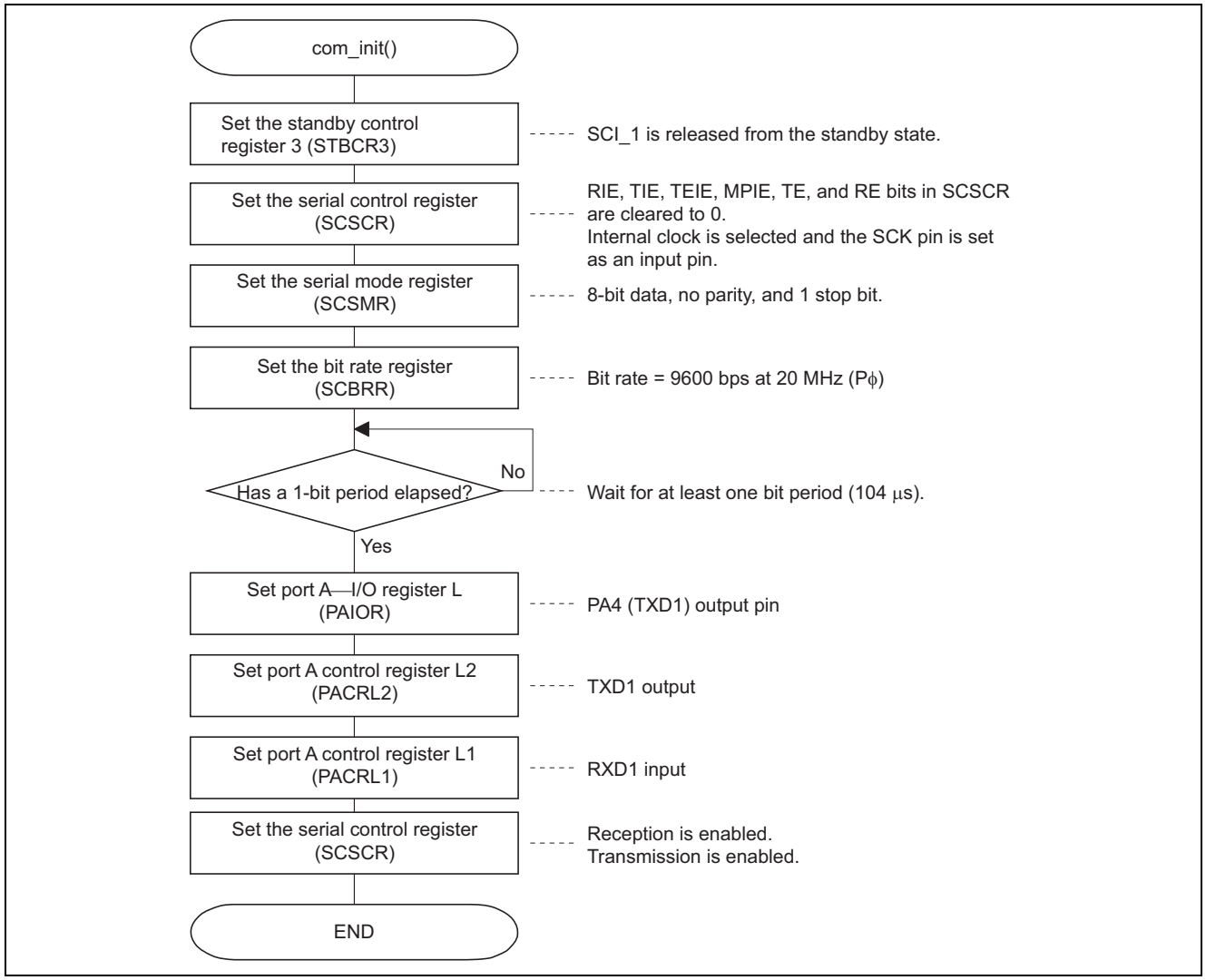


Figure 7 Processing by the SCI Channel 1 Initialization Routine

6.3 Routine to Check for SCI_1 Received Data

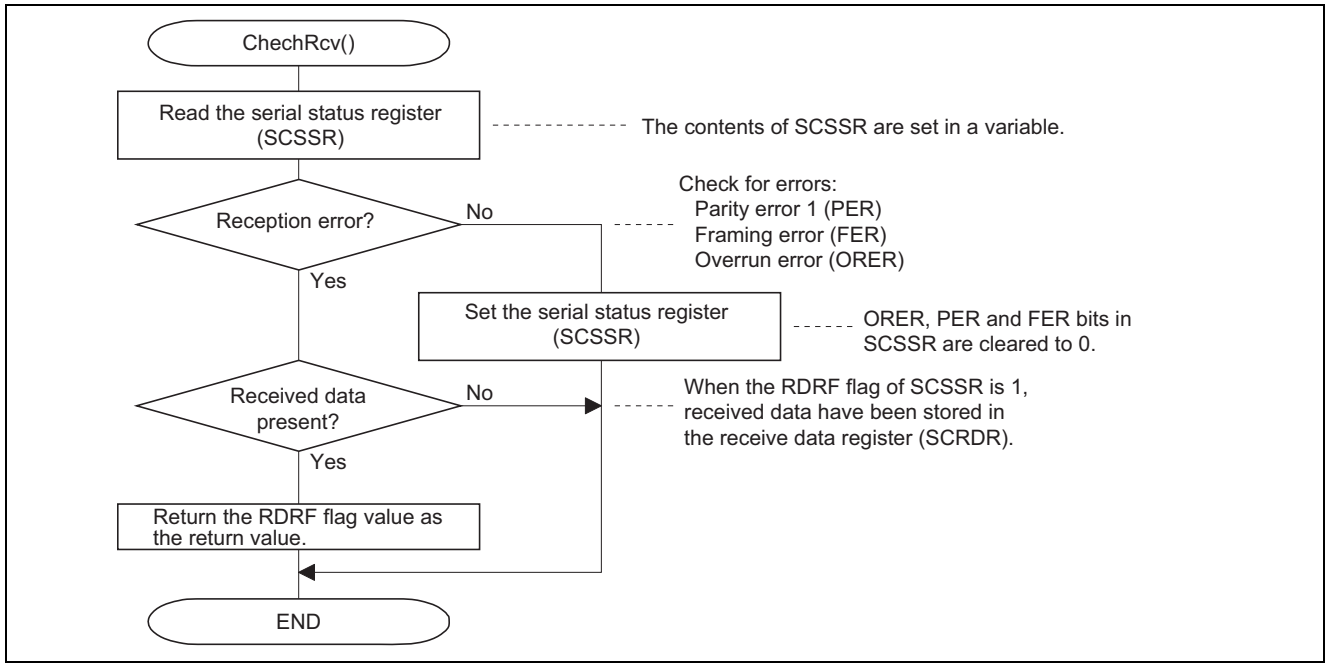


Figure 8 Processing by the Routine to Check for SCI_1 Received Data

6.4 SCI_1 n-Byte Reception Routine

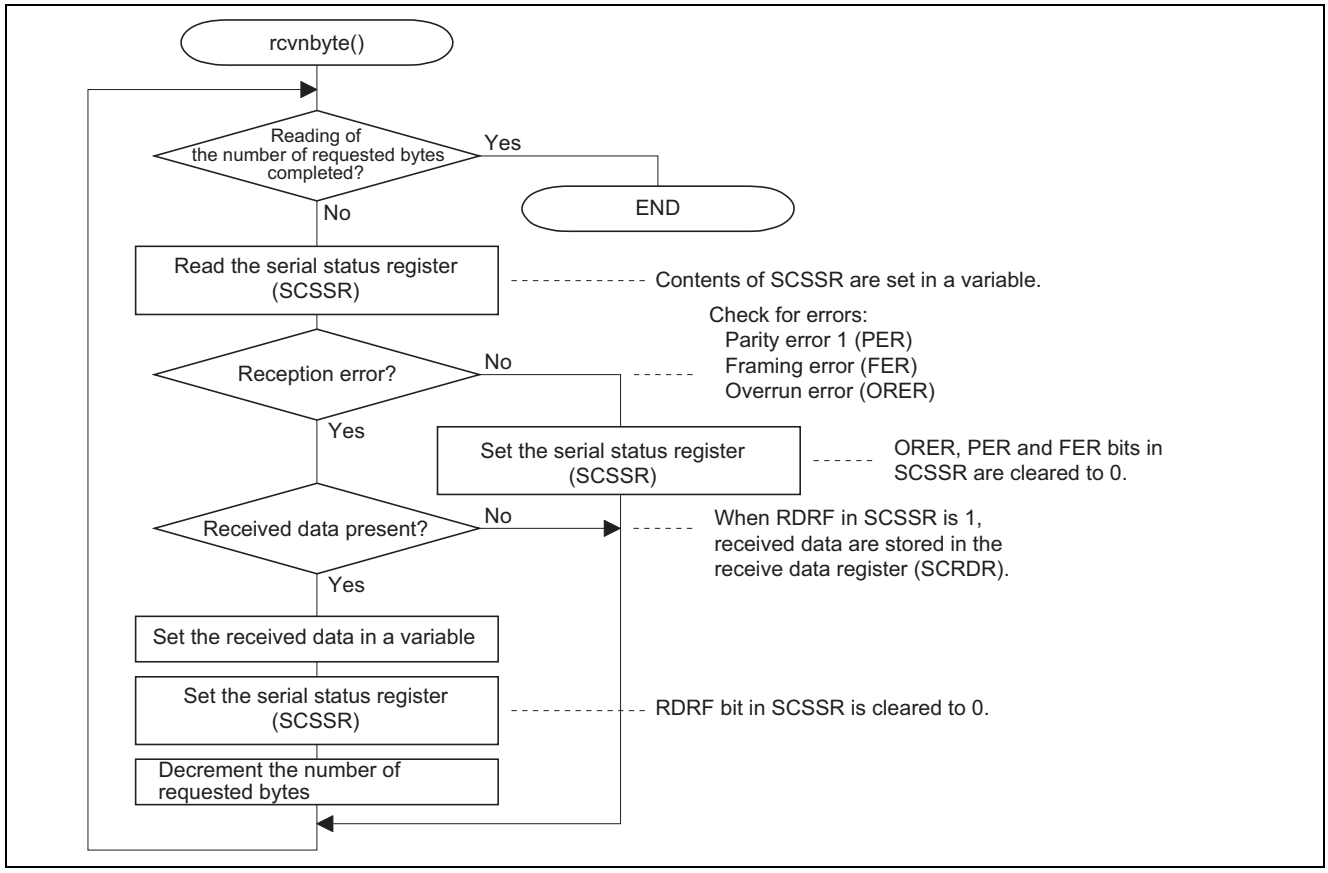


Figure 9 Processing by the SCI_1 n-Byte Reception Routine

6.5 SCI_1 1-Byte Transmission Routine

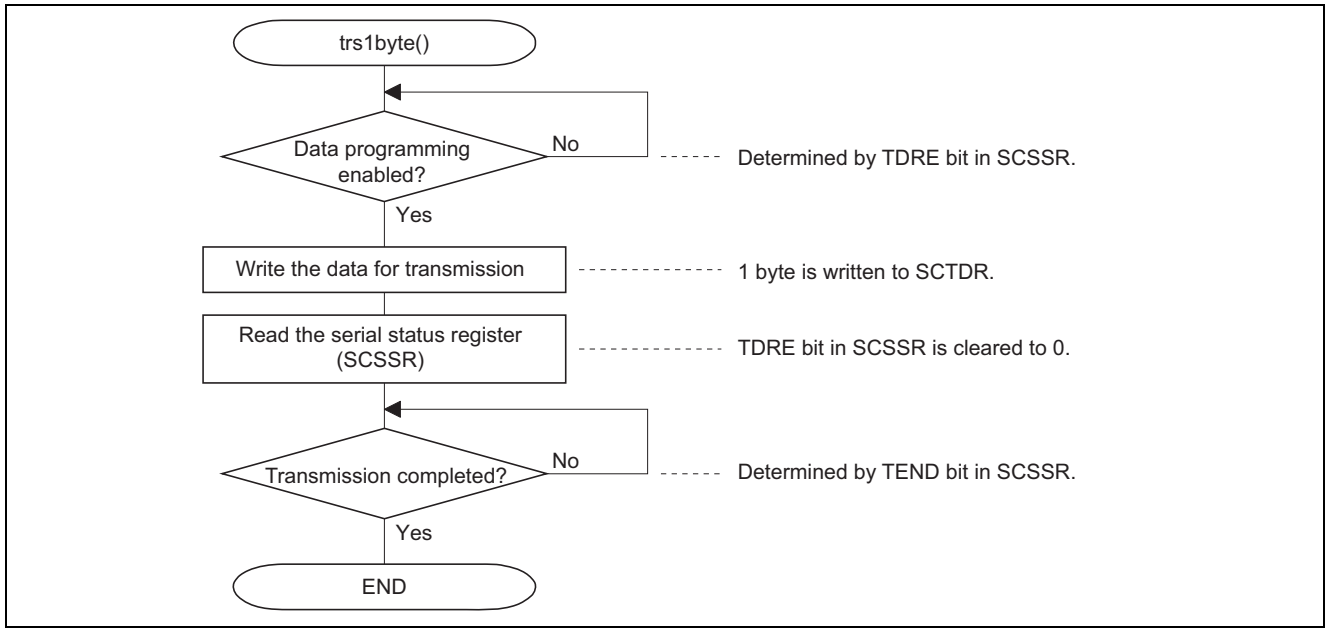


Figure 10 Processing by the SCI_1 1-Byte Transmission Routine

6.6 Main Routine for Flash Programming Main Routine

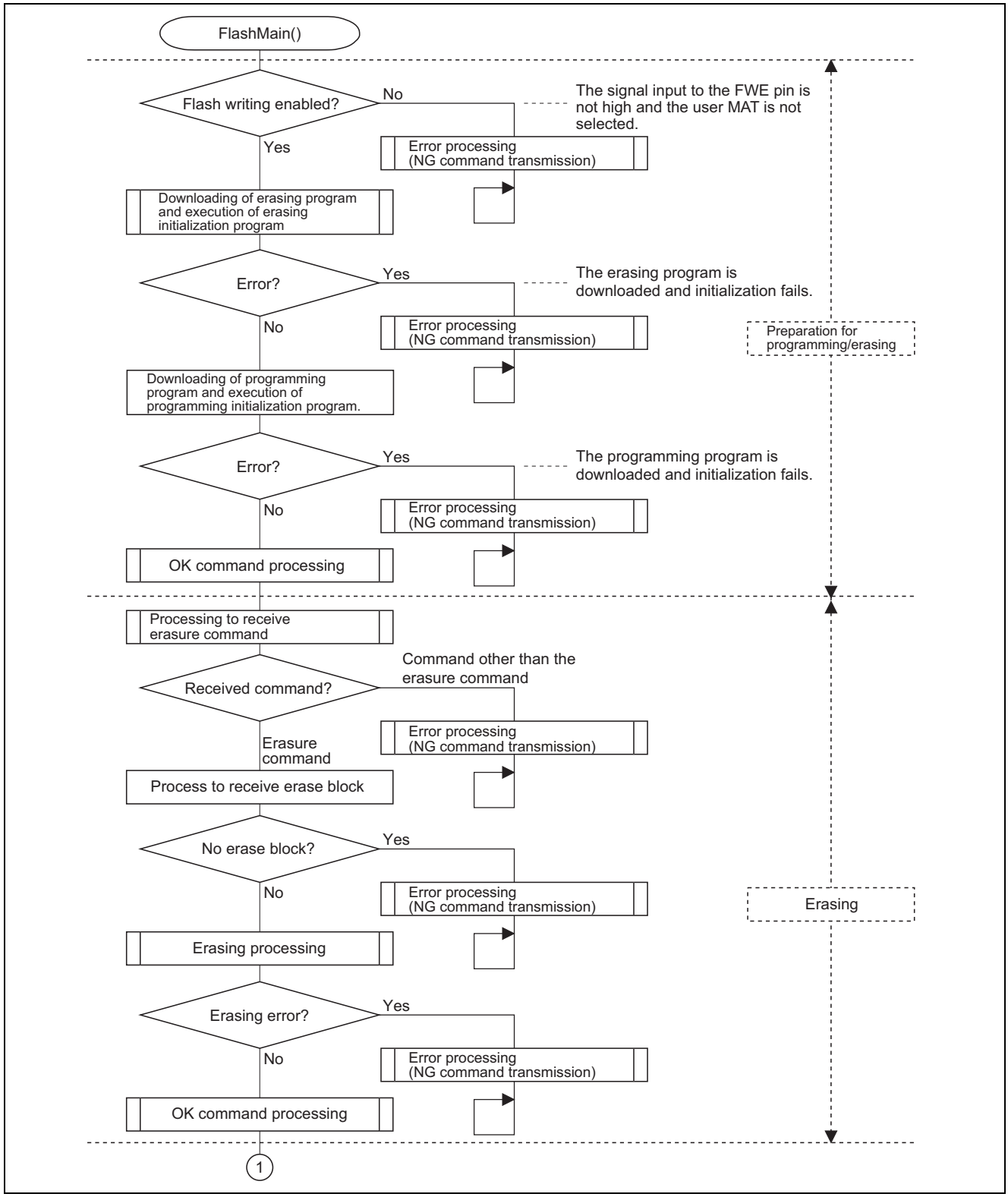


Figure 11 Processing by the Main Routine for Flash Programming (1)

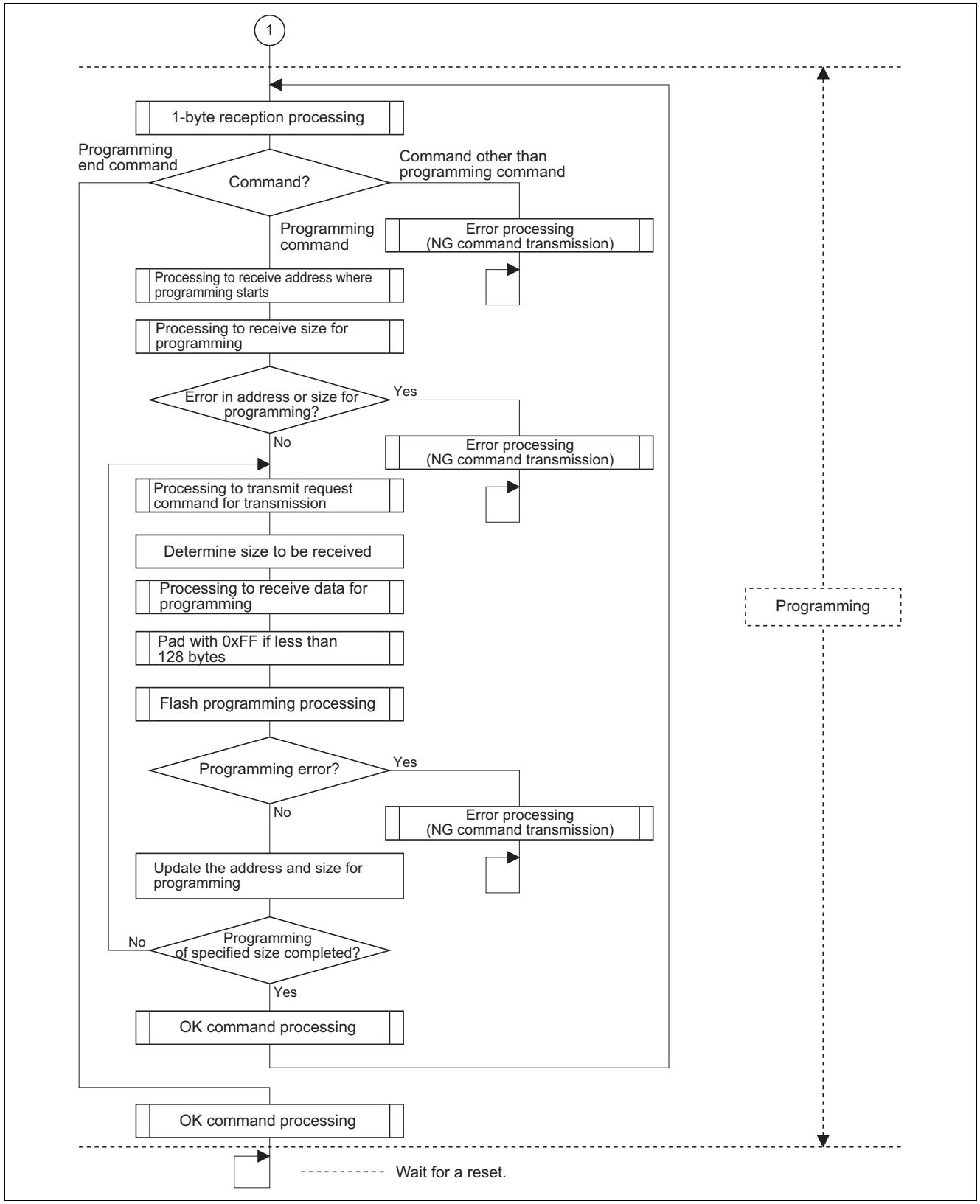


Figure 12 Processing by the Main Routine for Flash Programming (2)

6.7 Flash Reading Routine

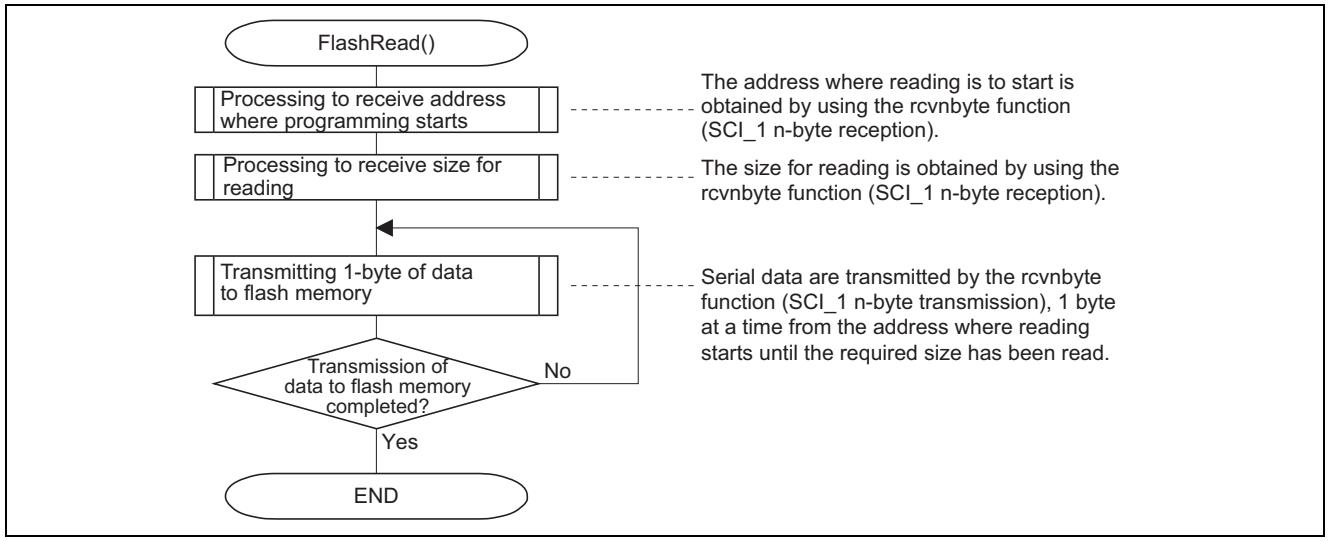


Figure 13 Processing to Read Flash Memory

6.8 Erasing Program Downloading and Initialization Routine

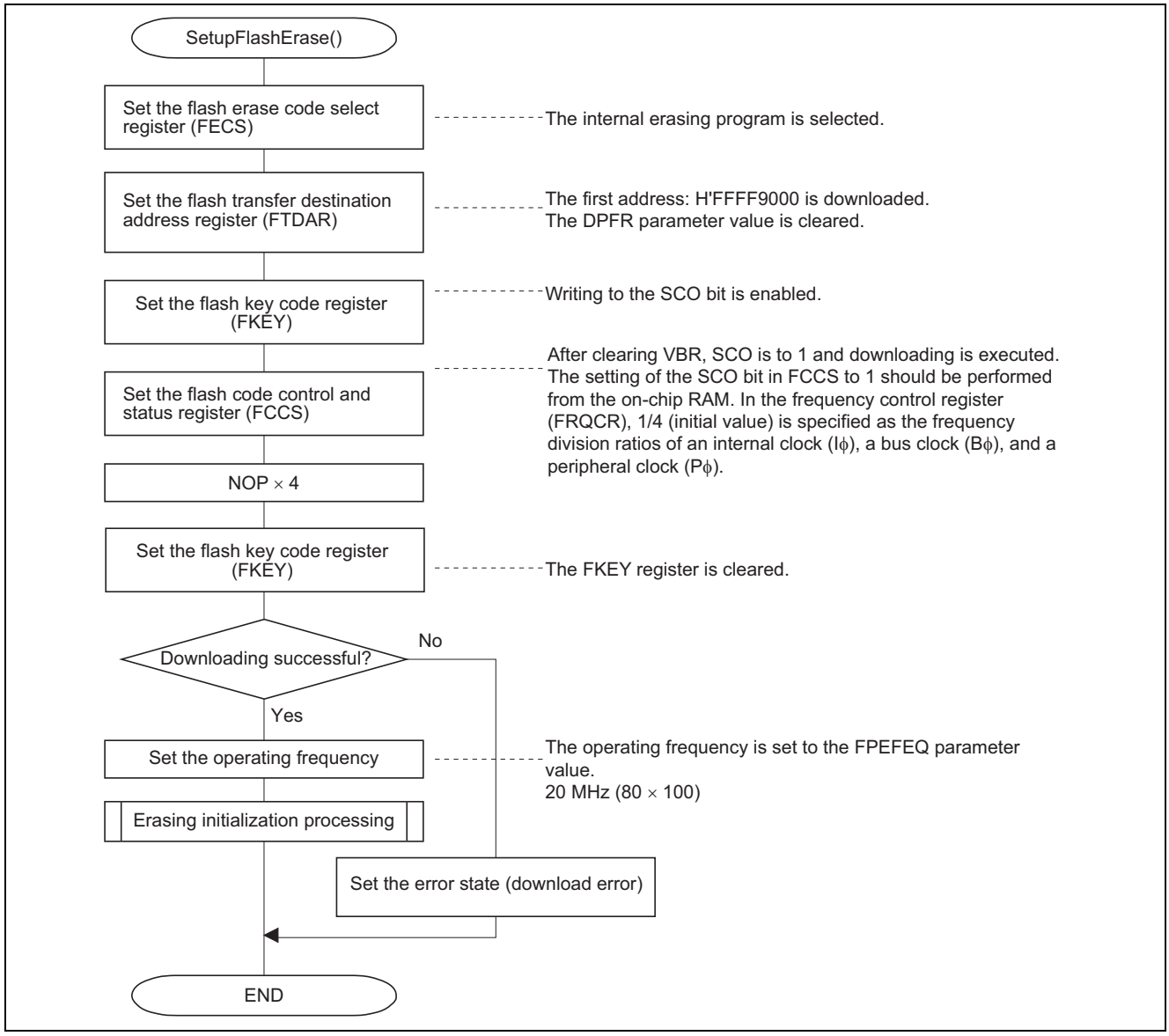


Figure 14 Processing by the Erasing Program Downloading and Initialization Routine

6.9 Flash Erasing Routine

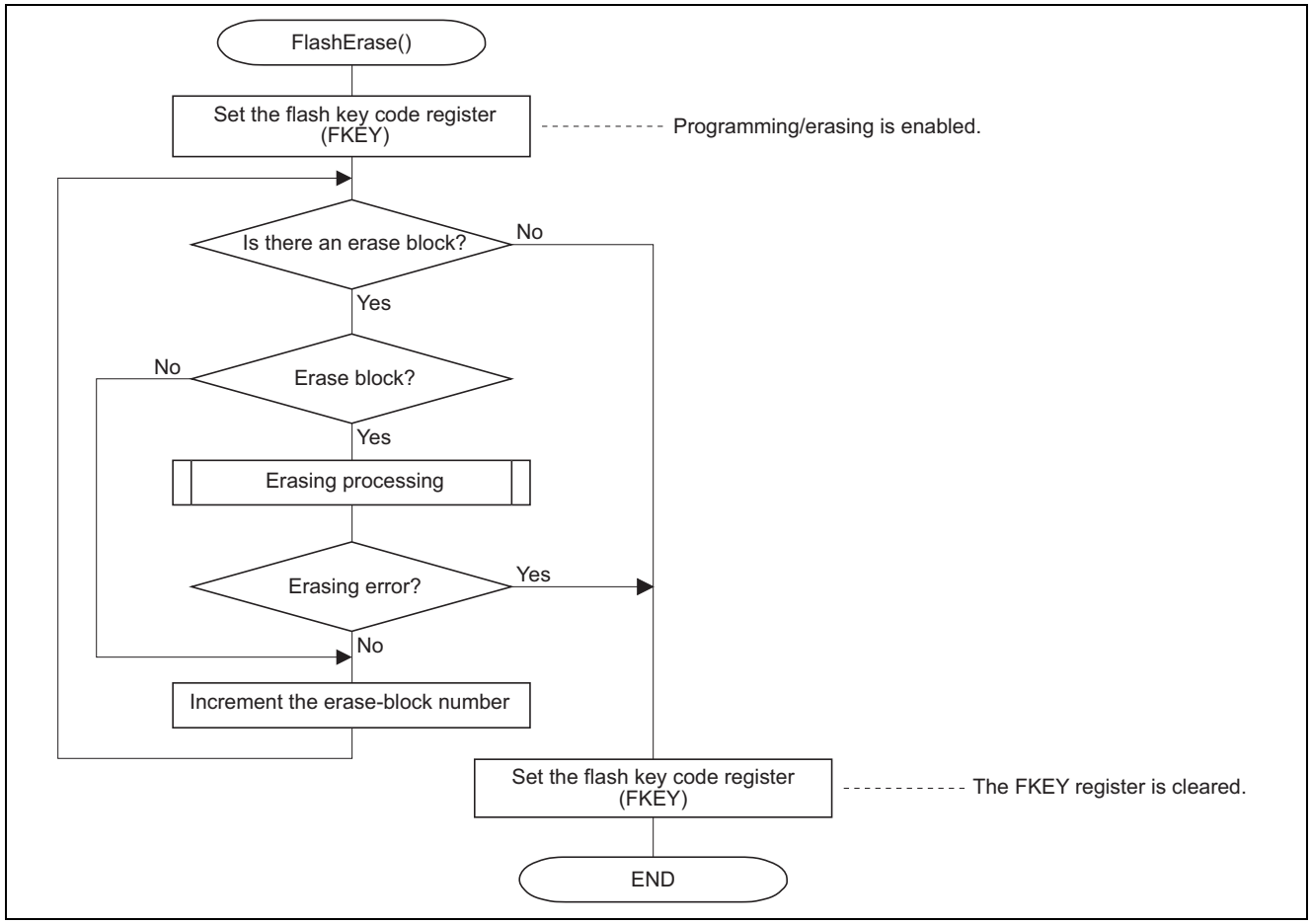


Figure 15 Processing by the Flash Erasing Routine

6.10 Programming Program Downloading and Initialization Routine

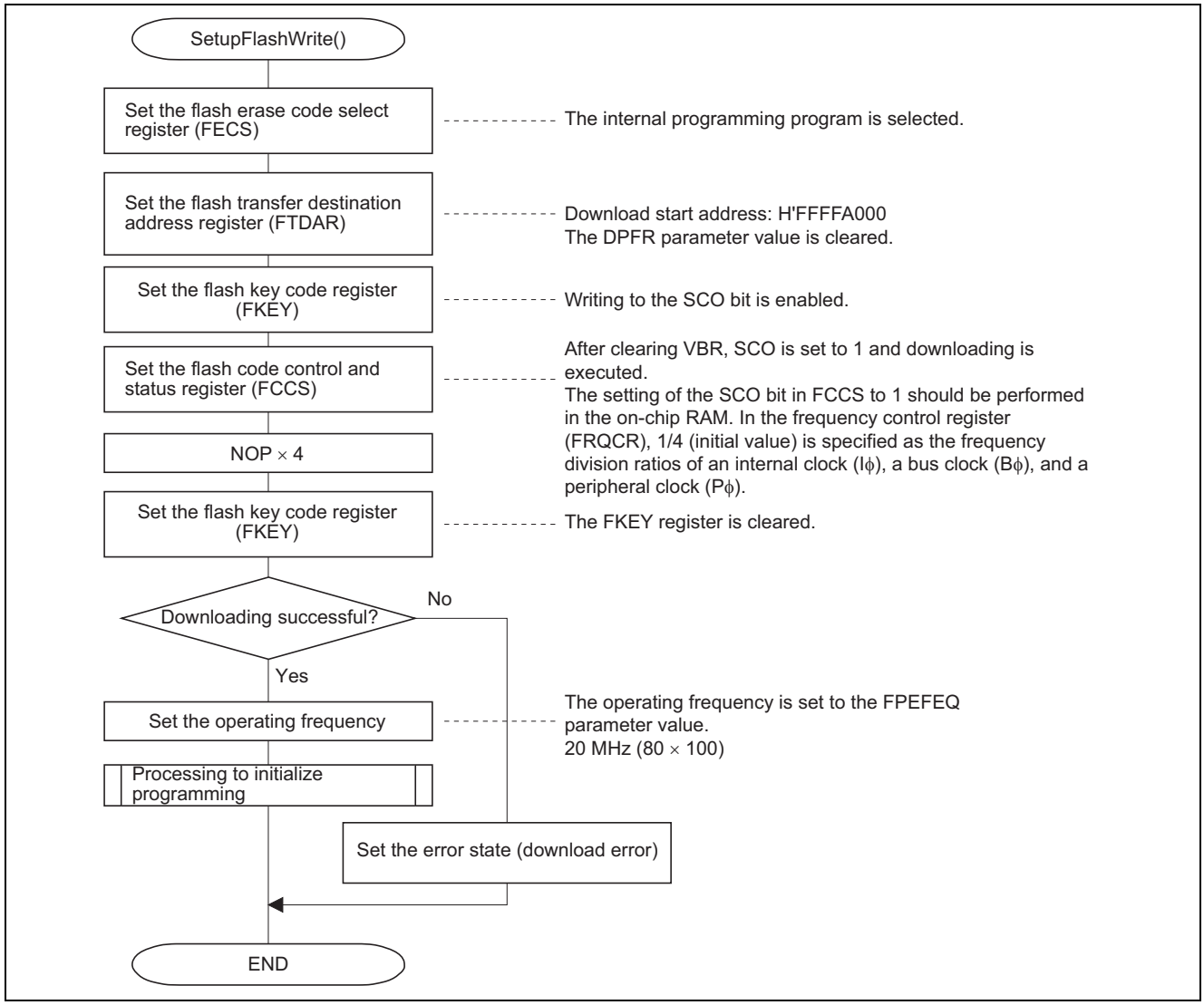


Figure 16 Processing by the Programming Program Downloading and Initialization Routine

6.11 Flash Programming Routine

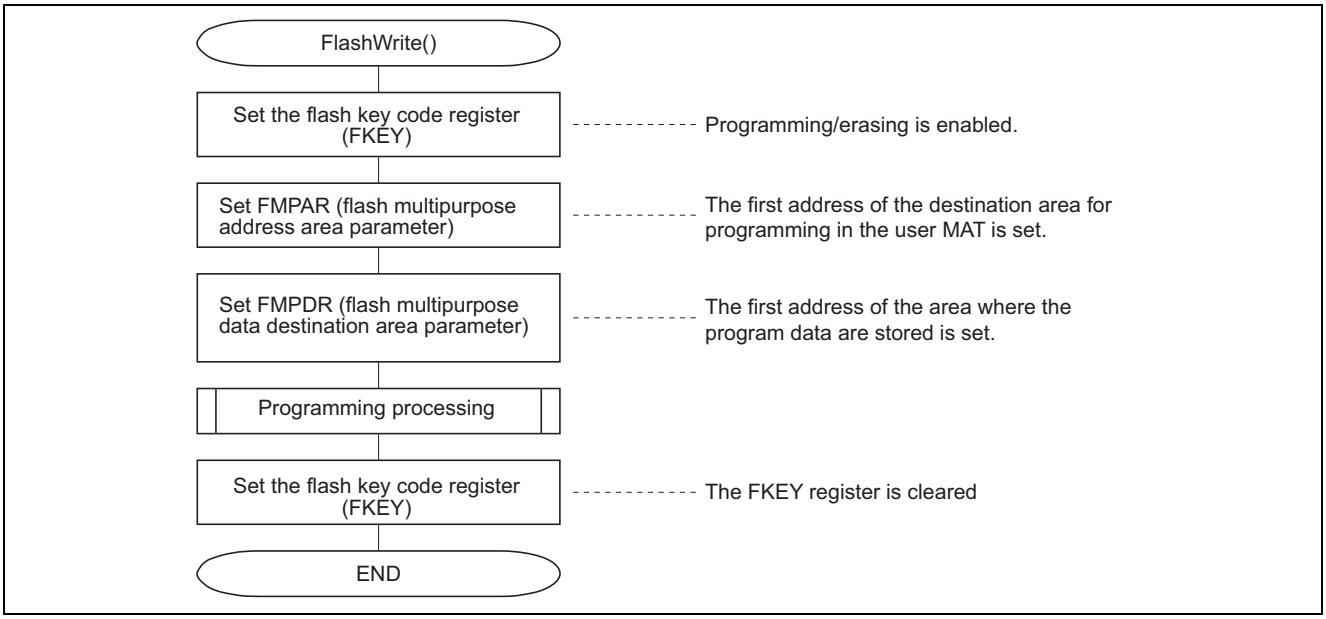


Figure 17 Processing by the Flash Programming Routine Processing

7. Documents for Reference

- Software Manual
  SH-1/SH-2/SH-DSP Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7080 Series Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

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Revision Record

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