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Old Company Name in Catalogs and Other Documents

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April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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SH7080 Series
User Program Mode (UART) Function

Introduction
The SH7080 has three on-board programming modes: boot mode, user boot mode, and user program mode. The user program mode provides for the erasure and programming of flash memory through a desired interface. This application describes how to erase and program the flash memory in the user program mode during execution of a user application when the flash reprogramming commands are received from a UART (Universal Asynchronous Receiver/Transmitter). The information has been collected for reference to help in the design of user software.

Target Device
SH7086

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1. Specifications .................................................................................................................. 2
2. Applicable Conditions ....................................................................................................... 3
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1. Specifications

In this sample application, the user program mode is employed to erase and program on-chip flash memory while a user application program is being executed. Serial transfer with the UART of a host system (PC) is employed, and the flash memory is placed in the programmable state by when reception of the corresponding command from the host (PC) is detected. Figure 1 shows the basic specifications of this sample application.

![Diagram of SH7080 Series MCU with Host (PC), Flash erasing/programming tool, On-chip SCI1, On-chip RAM, and Flash memory connections]

**Figure 1 Erasing and Programming Flash Memory in User Program Mode**
2. Applicable Conditions

Applicable conditions for this application sample are shown in table 1.

Table 1 Applicable Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>SH7086 (R5F70865)</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>Internal clock ( I_\phi = 20 \text{ MHz} )</td>
</tr>
<tr>
<td></td>
<td>Bus clock ( B_\phi = 20 \text{ MHz} )</td>
</tr>
<tr>
<td></td>
<td>Peripheral clock ( P_\phi = 20 \text{ MHz} )</td>
</tr>
<tr>
<td></td>
<td>MTU2 clock ( MP_\phi = 20 \text{ MHz} )</td>
</tr>
<tr>
<td></td>
<td>MTU2S clock ( MI_\phi = 20 \text{ MHz} )</td>
</tr>
<tr>
<td>Device operating mode</td>
<td>Single-chip mode</td>
</tr>
<tr>
<td>Development environment</td>
<td>High-performance Embedded Workshop Ver.4.03.00.001</td>
</tr>
<tr>
<td></td>
<td>SuperH RISC engine Standard Toolchain (V.9.1.0.0)</td>
</tr>
<tr>
<td></td>
<td>SuperH RISC engine C/C++ Compiler (V.9.01.00)</td>
</tr>
<tr>
<td></td>
<td>(manufactured by Renesas Technology)</td>
</tr>
<tr>
<td>C compiler option</td>
<td>High-performance Embedded Workshop default setting</td>
</tr>
</tbody>
</table>
|                       | \(-\text{cpu=sh2 -include="$\{WORKSPDIR\}\inc" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1} -nologo\)
3. Description of Modules Used

3.1 Flash Memory

A block diagram of flash memory is shown in figure 2.

![Block Diagram of Flash Memory](image-url)

**Figure 2** Block Diagram of Flash Memory
• Flash code control and status register (FCCS)
  FCCS is configured by bits which request the monitor of the FWE pin state and for error occurrence during programming or erasing flash memory and the download of the on-chip program.

• Flash program code select register (FPCS)
  FPCS selects the on-chip programming program to be downloaded.

• Flash erase code select register (FECS)
  FECS selects download of the on-chip erasing program.

• Flash key code register (FKEY)
  FKEY is a register for software protection that enables download of the on-chip program and programming/erasing of flash memory. Before setting the SCO bit to 1 in order to download the on-chip program or executing the downloaded programming/erasing program, each processing cannot be executed if the key code is not written.

• Flash MAT select register (FMATS)
  FMATS specifies whether user MAT or user boot MAT is selected.

• Flash transfer destination address register (FTDAR)
  FTDAR specifies the on-chip RAM address to which the on-chip program is downloaded. Make settings for FTDAR before writing 1 to the SCO bit in FCCS. The initial value is H'00 which points to the start address (H'FFFF9000) in on-chip RAM.

Note: For details regarding operational specification of each register, see the section on flash memory in SH7080 Series Hardware Manual.
3.2 Programming/Erasing Interface Parameters

The programming/erasing interface parameters specify the operating frequency, user branch destination address, storage place for program data, programming destination address, and erase block and exchanges the processing result for the downloaded on-chip program. The programming/erasing interface parameters are used in the following four items.

1. Download control
2. Initialization before programming or erasing
3. Programming
4. Erasing

<table>
<thead>
<tr>
<th>Table 2 Usable Parameters and Target Modes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter Name</td>
</tr>
<tr>
<td>Download pass/fail result</td>
</tr>
<tr>
<td>Flash pass/fail result</td>
</tr>
<tr>
<td>Flash programming/erasing frequency control</td>
</tr>
<tr>
<td>Flash user branch address set</td>
</tr>
<tr>
<td>Flash multipurpose address area</td>
</tr>
<tr>
<td>Flash multipurpose data destination area</td>
</tr>
<tr>
<td>Flash erase block select</td>
</tr>
</tbody>
</table>

Note: For details regarding operational specification of each register, see the section flash memory in SH7080 Series Hardware Manual.

* The processing results of initialization, programming, and erasing and returned, but bit contents have different meanings according to the processing program. Every parameter in the table is readable/writable and has an undefined initial value.
3.3 Specifications of Flash Erasing/Programming

In this sample application, the user application is stored in the first block (EB0) of the user MAT (addresses H'00000000 to H'00000FFF). The first area in the on-chip RAM (addresses H'FFFF4000 to H'FFFF47FF) is used as a data area (storage for variables). The user application consists of a vector table, communications program, and the procedure program for reprogramming of flash memory.

The target area of flash memory for reprogramming is the user MAT area other than the area for storing the user application, i.e. the region starting with block EB1 at H'00010000. The flash memory is switched from the user program execution state to a reprogrammable state (user program mode). The procedure program for erasing and programming is copied from the flash memory to the region of on-chip RAM (addresses H'FFFF4800 to H'FFFF4AFF) from which it will be executed. Addresses H'FFFF9000 to H'FFFFAFFF in the on-chip RAM is used as an area for downloading the specific programs to handle erasing and programming (erasing program and programming program).

The flash erasing/programming specifications are illustrated in figure 3. The memory map of the user MAT and on-chip RAM is shown in figure 4.

![Figure 3 Flash Erasing/Programming Specifications]
| H'0000 0000 to 0000 03DF | Vector table |
| H'0000 0400 to 0000 05FF | User application |
| H'0000 0600 to 0000 07FF | SCI1 communications program |
| H'0000 0800 to 0000 0FFF | Procedure program storage area |
| H'0000 1000 to 0007 FFFF | Target area for reprogramming |

**On-chip RAM**

| H'FFFF 4000 to FFFF 47FF | Data area |
| H'FFFF 4800 to FFFF 8FFF | Procedure program execution area |
| H'FFFF 9000 to FFFF 9FFF | Erasing program download area |

0000 DPFR (Return value: 1 byte)
0001 to 000F System area (15 bytes)
0010 to 001F Entry point for erasure processing
0020 to 002F Entry point for erasure initialization
0030 to 0FFF Erasing initialization + erasing program

| H'FFFF A000 to FFFF AFFF | Programming program download area |

0000 DPFR (Return value: 1 byte)
0001 to 000F System area (15 bytes)
0010 to 001F Entry point for programming processing
0020 to 002F Entry point for programming initialization
0030 to 0FFF Programming initialization + programming program

**Figure 4  Memory Map of the User MAT and On-Chip RAM**
4. Description of Operation

In this sample application, commands to control reading and programming/erasing of data in the on-chip flash memory are sent from a host (PC) via serial communications. The program waits for commands from the host (PC) after a reset.

1. Reading data from the on-chip flash memory

When the program receives a read command (CMD_READ) from the host (PC), it enters the state for reading out the on-chip flash memory. The program receives the address where it is to start reading and number of bytes from the host and then transmits the data from the specified area of on-chip flash memory to the host.

2. Erasing/reprogramming the on-chip flash memory

When the program receives the command to start reprogramming (CMD_GO) from the host (PC), it enters the state where the on-chip flash memory can be erased and reprogrammed. After receiving the reprogramming start command (CMD_GO), the program executes the erasing or programming initialization program. The on-chip flash memory is then erased and reprogrammed by erasing request (CMD_ERASE) and programming request (CMD_WRITE) commands from the host. This erasing and reprogramming of the on-chip flash memory should be executed from the on-chip RAM.

The command specifications are shown in table 3. The command control sequence in this sample application is shown in figure 5.

<table>
<thead>
<tr>
<th>Command</th>
<th>Command Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMD_GO</td>
<td>0x55</td>
<td>Starts reprogramming of flash memory</td>
</tr>
<tr>
<td>CMD_READ</td>
<td>0xAA</td>
<td>Reads flash memory</td>
</tr>
<tr>
<td>CMD_ERASE</td>
<td>0x77</td>
<td>Requests erasing of flash memory</td>
</tr>
<tr>
<td>CMD_WRITE</td>
<td>0x88</td>
<td>Requests programming of flash memory</td>
</tr>
<tr>
<td>CMD_WEND</td>
<td>0x99</td>
<td>Ends programming of flash memory</td>
</tr>
<tr>
<td>CMD_OK</td>
<td>0x00</td>
<td>OK (response to normal end)</td>
</tr>
<tr>
<td>CMD_NG</td>
<td>0x01</td>
<td>NG (response to abnormal end)</td>
</tr>
<tr>
<td>CMD_REQUEST</td>
<td>0x11</td>
<td>Request for transmission</td>
</tr>
</tbody>
</table>
Figure 5  Control Sequence for Commands
5. Description of Software

5.1 Description of Functions

The functions used in this application sample are described in table 4.

Table 4 Description of Modules

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Label Name</th>
<th>File Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>main()</td>
<td>main.c</td>
<td>Initial setting of SCI ch1. Executes the user application program. Performs flash erasing/programming processing in response to requests for flash erasing/programming.</td>
</tr>
<tr>
<td>SCI channel 1 initial setting routine</td>
<td>com_init()</td>
<td>sci.c</td>
<td>Handles SCIF transmit-FIFO-data-empty interrupts.</td>
</tr>
<tr>
<td>SCI1 receive data presence check routine</td>
<td>CheckRcv()</td>
<td></td>
<td>Checks whether received data are stored in SCRRD.</td>
</tr>
<tr>
<td>SCI1 n-byte reception routine</td>
<td>rcvnbyte()</td>
<td></td>
<td>Receives the specified number of bytes of data.</td>
</tr>
<tr>
<td>SCI1 1-byte transmission routine</td>
<td>trs1byte()</td>
<td></td>
<td>Writes 1 byte for serial output.</td>
</tr>
<tr>
<td>Erasing program download and initialization routine</td>
<td>SetupFlashErase()</td>
<td>flash.c</td>
<td>Downloads the erasing program into the RAM and performs initialization.</td>
</tr>
<tr>
<td>Flash erasing routine</td>
<td>FlashErase()</td>
<td></td>
<td>Erases the specified erase blocks in order from the EB0 block.</td>
</tr>
<tr>
<td>Programming program download and initialization routine</td>
<td>SetupFlashWrite()</td>
<td></td>
<td>Downloads the programming program into the RAM and performs initialization.</td>
</tr>
<tr>
<td>Flash programming routine</td>
<td>FlashWrite()</td>
<td></td>
<td>Writes data to the specified address.</td>
</tr>
<tr>
<td>Flash programming main routine</td>
<td>FlashMain()</td>
<td></td>
<td>Checks commands and performs erasing/programming.</td>
</tr>
<tr>
<td>Flash reading routine</td>
<td>FlashRead()</td>
<td></td>
<td>Reads the specified amount of flash memory starting from the specified address.</td>
</tr>
</tbody>
</table>

5.2 Variables Used

The variables used in this application sample are described in table 5.

Table 5 Variables Used

<table>
<thead>
<tr>
<th>Variable and Label Name</th>
<th>Description</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char WriteBuff[128]</td>
<td>Program data area</td>
<td>FlashMain()</td>
</tr>
<tr>
<td>unsigned char flash_erase[2048]</td>
<td>Area for downloading the erasing program</td>
<td>SetupFlashErase()</td>
</tr>
<tr>
<td>unsigned char flash_write[2048]</td>
<td>Area for downloading the programming program</td>
<td>SetupFlashWrite()</td>
</tr>
</tbody>
</table>
5.3 Register Settings

This section describes the setting of registers used in this application sample. Note that the settings shown below are used in the sample task and are not initial values.

5.3.1 Register for Setting the Clock Pulse Generator (CPG)

- Frequency Control Register (FRQCR)
  - This register specifies the division ratio of the frequency. The settings shown in the tables are the values used in this sample task and differ from the initial values.
  - Setting: H'36DB

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Value</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>⎯</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>14 to 12</td>
<td>IFC2 to IFC0</td>
<td>011</td>
<td>Internal Clock (Iφ) Frequency Division Ratio 011: × 1, 20 MHz when the input clock is 10 MHz</td>
</tr>
<tr>
<td>11 to 9</td>
<td>BFC2 to BFC0</td>
<td>011</td>
<td>Bus Clock (Bφ) Frequency Division Ratio 011: × 1/4, 20 MHz when the input clock is 10 MHz</td>
</tr>
<tr>
<td>8 to 6</td>
<td>PFC2 to PFC0</td>
<td>011</td>
<td>Peripheral Clock (Pφ) Frequency Division Ratio 011: × 1/4, 20 MHz when the input clock is 10 MHz</td>
</tr>
<tr>
<td>5 to 3</td>
<td>MIFC2 to MIFC0</td>
<td>011</td>
<td>MTU2S Clock (MIφ) Frequency Division Ratio 011: × 1/4, 20 MHz when the input clock is 10 MHz</td>
</tr>
<tr>
<td>2 to 0</td>
<td>MPFC2 to MPFC0</td>
<td>011</td>
<td>MTU2 Clock (MPφ) Frequency Division Ratio 011: × 1/4, 20 MHz when the input clock is 10 MHz</td>
</tr>
</tbody>
</table>

Note: When reprogramming flash memory, the procedure program must be executed from an area other than the flash memory to be programmed. In particular, the part where the SCO bit in FCCS is set to 1 for downloading of the procedure program to the on-chip RAM must be executed from the on-chip RAM. In the frequency control register (FRQCR), specify the frequency division ratios of the internal clock (Iφ), bus clock (Bφ), and peripheral clock (Pφ) as 1/4 (initial value). After the programming/erasing program has been downloaded and the SCO bit is cleared to 0, the setting of the frequency control register (FRQCR) can be changed to the desired value. For details on the specifications, see the section on flash memory in SH7080 Series Hardware Manual.

5.3.2 Setting the Power-Down Mode

- Standby Control Register 3 (STBCR3)
  - This register controls the operation of modules in power-down mode.
  - Setting: H'EF

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Value</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>MSTP15</td>
<td>1</td>
<td>1: Clock signal supplied to I^C2 is halted.</td>
</tr>
<tr>
<td>6</td>
<td>MSTP14</td>
<td>1</td>
<td>1: Clock signal supplied to SCIF is halted.</td>
</tr>
<tr>
<td>5</td>
<td>MSTP13</td>
<td>1</td>
<td>1: Clock signal supplied to SCI_2 is halted.</td>
</tr>
<tr>
<td>4</td>
<td>MSTP12</td>
<td>0</td>
<td>0: Clock signal is supplied (SCI_1 operates).</td>
</tr>
<tr>
<td>3</td>
<td>MSTP11</td>
<td>1</td>
<td>1: Clock signal supplied to SCI_0 is halted.</td>
</tr>
<tr>
<td>2</td>
<td>MSTP10</td>
<td>1</td>
<td>1: Clock signal supplied to SSU is halted.</td>
</tr>
<tr>
<td>1, 0</td>
<td>⎯</td>
<td>11</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
5.3.3 Setting the Synchronous Serial Communication Interface ch1 (SCI1)

- **Serial Control Register (SCSCR)**
  This register selects transmission and reception by the SCI, enables or disables interrupt requests, and selects the clock source for transmission and reception.
  Setting: H'30

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Value</th>
<th>Setting</th>
</tr>
</thead>
</table>
| 7   | TIE      | 1     | 0: Transmit-FIFO-data-empty interrupt request (TXI) is disabled  
                                 1: Transmit-FIFO-data-empty interrupt request (TXI) is enabled |
| 6   | RIE      | 0     | 0: Receive-data-full interrupt (RXIF), receive-error interrupt (ERIF), and break interrupt (BRIF) requests are disabled |
| 5   | TE       | 1     | 0: Transmission disabled  
                                 1: Transmission enabled |
| 4   | RE       | 0     | 0: Reception disabled |
| 3   | REIE     | 0     | 0: Receive-error interrupt (ERIF) and break interrupt (BRIF) requests are disabled |
| 2   | —        | 0     | Reserved |
| 1, 0| CKE1 and CKE0 | 00 | 00: Internal clock, SCK pin used for input pin (The input signal is ignored. |

- **Serial Mode Register (SCSMR)**
  This register specifies the SCI serial communication format and selects the clock source for the baud rate generator.
  Setting: H'00

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Value</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>C/Â</td>
<td>0</td>
<td>0: Asynchronous mode</td>
</tr>
<tr>
<td>6</td>
<td>CHR</td>
<td>0</td>
<td>0: 8-bit data</td>
</tr>
<tr>
<td>5</td>
<td>PE</td>
<td>0</td>
<td>0: Parity bit not added or checked</td>
</tr>
<tr>
<td>4</td>
<td>O/E</td>
<td>0</td>
<td>0: The O/E bit is ignored because PE=0.</td>
</tr>
<tr>
<td>3</td>
<td>STOP</td>
<td>0</td>
<td>0: One stop bit</td>
</tr>
<tr>
<td>2</td>
<td>—</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1, 0</td>
<td>CKS1 and CKS0</td>
<td>00</td>
<td>00: P quốc</td>
</tr>
</tbody>
</table>

- **Bit Rate Register (SCBRR)**
  This register determines the serial transmit/receive bit rate.
  Setting: 64 (H'40)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Value</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 to 0</td>
<td>—</td>
<td>0100</td>
<td>Bit rate for serial transmission and reception</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0000</td>
<td></td>
</tr>
</tbody>
</table>
### 5.3.4 Registers for Setting the Pin Function Controller (PFC)

- **Port A I/O Register L (PAIORL)**
  
  This register selects the input direction for the pins of port A.

  Setting: H'0010

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Value</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>PA15IOR</td>
<td>0</td>
<td>0: PA15 input</td>
</tr>
<tr>
<td>14</td>
<td>PA14IOR</td>
<td>0</td>
<td>0: PA14 input</td>
</tr>
<tr>
<td>13</td>
<td>PA13IOR</td>
<td>0</td>
<td>0: PA13 input</td>
</tr>
<tr>
<td>12</td>
<td>PA12IOR</td>
<td>0</td>
<td>0: PA12 input</td>
</tr>
<tr>
<td>11</td>
<td>PA11IOR</td>
<td>0</td>
<td>0: PA11 input</td>
</tr>
<tr>
<td>10</td>
<td>PA10IOR</td>
<td>0</td>
<td>0: PA10 input</td>
</tr>
<tr>
<td>9</td>
<td>PA9IOR</td>
<td>0</td>
<td>0: PA9 input</td>
</tr>
<tr>
<td>8</td>
<td>PA8IOR</td>
<td>0</td>
<td>0: PA8 input</td>
</tr>
<tr>
<td>7</td>
<td>PA7IOR</td>
<td>0</td>
<td>0: PA7 input</td>
</tr>
<tr>
<td>6</td>
<td>PA6IOR</td>
<td>0</td>
<td>0: PA6 input</td>
</tr>
<tr>
<td>5</td>
<td>PA5IOR</td>
<td>0</td>
<td>0: PA5 input</td>
</tr>
<tr>
<td>4</td>
<td>PA4IOR</td>
<td>1</td>
<td>0: PA4 output, TXD1 pin</td>
</tr>
<tr>
<td>3</td>
<td>PA3IOR</td>
<td>0</td>
<td>0: PA3 input, RXD1 pin</td>
</tr>
<tr>
<td>2</td>
<td>PA2IOR</td>
<td>0</td>
<td>0: PA2 input</td>
</tr>
<tr>
<td>1</td>
<td>PA1IOR</td>
<td>0</td>
<td>0: PA1 input</td>
</tr>
<tr>
<td>0</td>
<td>Pa0IOR</td>
<td>0</td>
<td>0: PA0 input</td>
</tr>
</tbody>
</table>

- **Port A Control Register L2 (PACRL2)**
  
  This register selects the functions of multiplexed pins of port A.

  Setting: H'0001

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Value</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>—</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>14 to 12</td>
<td>PA7MD2 to PA7MD0</td>
<td>000</td>
<td>000: PA7 input/output (port)</td>
</tr>
<tr>
<td>11</td>
<td>—</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10 to 8</td>
<td>PA6MD2 to PA6MD0</td>
<td>000</td>
<td>000: PA6 input/output (port)</td>
</tr>
<tr>
<td>7</td>
<td>—</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>6 to 4</td>
<td>PA5MD2 to PA5MD0</td>
<td>000</td>
<td>000: PA6 input/output (port)</td>
</tr>
<tr>
<td>3</td>
<td>—</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>2 to 0</td>
<td>PA4MD2 to PA4MD0</td>
<td>001</td>
<td>001: TXD1 output (SCI)</td>
</tr>
</tbody>
</table>
- Port A Control Register L1 (PACRL1)
  This register selects the functions of multiplexed pins in port A.
  Setting: H'1000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Value</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td></td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>14 to 12</td>
<td>PA3MD2 to PA3MD0</td>
<td>001</td>
<td>001: RXD1 input (SCI)</td>
</tr>
<tr>
<td>11</td>
<td></td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>10 to 8</td>
<td>PA2MD2 to PA2MD0</td>
<td>000</td>
<td>000: PA2 input/output (port)</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>6 to 4</td>
<td>PA1MD2 to PA1MD0</td>
<td>000</td>
<td>000: PA1 input/output (port)</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>2 to 0</td>
<td>PA0MD2 to 0</td>
<td>000</td>
<td>000: PA0 input/output (port)</td>
</tr>
</tbody>
</table>
6. Flowcharts

The process flows in this application sample are given below.

6.1 Main Routine

```
main()

Set the frequency control register (FRQCR)

Operating frequency is set.
When the external input clock frequency is 10 MHz;
Internal (Iφ) = 20 MHz, bus (Bφ) = 20 MHz,
peripheral (Pφ) = 20 MHz, MTU2S (Mφ) = 20 MHz,
MTU2S (MPφ) = 20 MHz

Initialize the UART

SCI channel 1 is initialized.

User application program processing

There is no processing in this sample program.

Processing to check for presence of received data

Whether received data are stored in SCRDR is checked.

Received data present?

Yes

Processing to read received data

Receive data is stored in a variable.

No

Command received?

Yes

Flash erasing/programming request command
(Command name: CMD_GO)

Processing to erase/program flash memory

No

Flash read request
(Command name: CMD_READ)

Processing to read flash memory

After copying a procedure program into the RAM, the procedure program from the RAM is executed.
```

Figure 6 Main Routine Processing
6.2 SCI Channel 1 Initialization Routine

com_init()

Set the standby control register 3 (STBCR3)

Set the serial control register (SCSCR)

Set the serial mode register (SCSMR)

Set the bit rate register (SCBRR)

Has a 1-bit period elapsed?

No

SCI_1 is released from the standby state.

RIE, TIE, TEIE, MPIE, TE, and RE bits in SCSCR are cleared to 0.
Internal clock is selected and the SCK pin is set as an input pin.

8-bit data, no parity, and 1 stop bit.

Bit rate = 9600 bps at 20 MHz (P\_\phi)

Wait for at least one bit period (104 \( \mu \)s).

Set port A—I/O register L (PAIOR)

Set port A control register L2 (PACRL2)

Set port A control register L1 (PACRL1)

Set the serial control register (SCSCR)

END

Figure 7 Processing by the SCI Channel 1 Initialization Routine
6.3 Routine to Check for SCI_1 Received Data

![Flowchart Diagram]

- **CheckRcv()**

  - Read the serial status register (SCSSR)
  - The contents of SCSSR are set in a variable.

  - Reception error?
    - Yes
      - Set the serial status register (SCSSR)
      - ORER, PER and FER bits in SCSSR are cleared to 0.
    - No
      - Check for errors:
        - Parity error 1 (PER)
        - Framing error (FER)
        - Overrun error (ORER)

  - Received data present?
    - Yes
      - When the RDRF flag of SCSSR is 1, received data have been stored in the receive data register (SCRDR).
    - No
      - Return the RDRF flag value as the return value.

- **END**

*Figure 8  Processing by the Routine to Check for SCI_1 Received Data*
6.4 SCI_1 n-Byte Reception Routine

Figure 9  Processing by the SCI_1 n-Byte Reception Routine
6.5 SCI_1 1-Byte Transmission Routine

Figure 10 Processing by the SCI_1 1-Byte Transmission Routine
6.6 Main Routine for Flash Programming Main Routine

Figure 11 Processing by the Main Routine for Flash Programming (1)
Figure 12  Processing by the Main Routine for Flash Programming (2)
6.7  Flash Reading Routine

Figure 13  Processing to Read Flash Memory

1. The address where reading is to start is obtained by using the rcvnbty function (SCI_1 n-byte reception).
2. The size for reading is obtained by using the rcvnbty function (SCI_1 n-byte reception).
3. Serial data are transmitted by the rcvnbty function (SCI_1 n-byte transmission), 1 byte at a time from the address where reading starts until the required size has been read.

The address where reading starts is obtained by using the rcvnbty function (SCI_1 n-byte reception).

The size for reading is obtained by using the rcvnbty function (SCI_1 n-byte reception).

Serial data are transmitted by the rcvnbty function (SCI_1 n-byte transmission), 1 byte at a time from the address where reading starts until the required size has been read.
6.8 Erasing Program Downloading and Initialization Routine

![Flowchart](image)

- **SetupFlashErase()**
  - Set the flash erase code select register (FECS)
  - The internal erasing program is selected.
  - Set the flash transfer destination address register (FTDAR)
  - The first address: H'FFFF9000 is downloaded.
  - The DPFR parameter value is cleared.
  - Set the flash key code register (FKEY)
  - Writing to the SCO bit is enabled.
  - Set the flash code control and status register (FCCS)
  - After clearing VBR, SCO is to 1 and downloading is executed.
- **NOP × 4**
- **Set the flash key code register (FKEY)**
  - The FKEY register is cleared.
  - Downloading successful?
    - No
      - Set the error state (download error)
    - Yes
      - Set the operating frequency
      - Erasing initialization processing
  - The operating frequency is set to the FPEFEQ parameter value.
  - 20 MHz (80 × 100)
  - END

Figure 14 Processing by the Erasing Program Downloading and Initialization Routine
6.9 Flash Erasing Routine

Figure 15 Processing by the Flash Erasing Routine
6.10 Programming Program Downloading and Initialization Routine

**Flowchart:**
- **SetupFlashWrite()**
- Set the flash erase code select register (FECS)
- Set the flash transfer destination address register (FTDAR)
- Set the flash key code register (FKEY)
- Set the flash code control and status register (FCCS)
- NOP × 4
- Set the flash key code register (FKEY)
- Downloading successful?
  - No
    - Set the error state (download error)
  - Yes
    - The internal programming program is selected.
    - Download start address: H'FFFFA000
    - The DPFR parameter value is cleared.
    - Writing to the SCO bit is enabled.
    - After clearing VBR, SCO is set to 1 and downloading is executed.
    - The setting of the SCO bit in FCCS to 1 should be performed in the on-chip RAM. In the frequency control register (FRQCR), 1/4 (initial value) is specified as the frequency division ratios of an internal clock (Iφ), a bus clock (Bφ), and a peripheral clock (Pφ).
    - The FKEY register is cleared.

**Figure 16** Processing by the Programming Program Downloading and Initialization Routine

The operating frequency is set to the FPEFEQ parameter value. 20 MHz (80 × 100)
6.11 Flash Programming Routine

- **FlashWrite()**
- Set the flash key code register (FKEY)
- Set FMPAR (flash multipurpose address area parameter)
- Set FMPDR (flash multipurpose data destination area parameter)
- Programming processing
- Set the flash key code register (FKEY)
- END

---

**Figure 17** Processing by the Flash Programming Routine Processing
7. **Documents for Reference**

- **Software Manual**
  The most up-to-date version of this document is available on the Renesas Technology Website.

- **Hardware Manual**
  SH7080 Series Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

Revision Record

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