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H8SX Family

LibUSB Device Demonstration

Introduction

This application note introduces the LibUSB library and shows an example of how to directly communicate with a USB device over the Bulk pipes. This document refers to the RSK H8SX/1664 USB kit and specifically to the included LibUSB application example.

Target Device

H8SX1664 (RSKH8SX1664)

Contents

1. Overview

The Renesas USB Stack and MSC sample program is an example of how to create a vendor defined class device that uses the LibUSB library to communicate with the PC.

2. Introduction to USB

The USB (Universal Serial Bus) is an interface and a protocol that allows a single host computer to communicate with a variety of peripheral devices. The USB 2.0 spec defines this interface. Although it is dependant on the application most USB projects will require a host side interface app and the device firmware. Every USB communication is between a host and a device, where the host controls the bus and initiates communication all the time, except in case of devices with the remote-wakeup feature (USB On-The-Go allows for devices to negotiate for the role of host and thus bus control). In comparison with other interfaces, USB offers a host of advantages which include, automatic configuration (enumeration), minimum IRQ lines used, hot pluggable, low cost, low power consumption, speed and reliability. Depending on the application, the developers can chose one of four USB transfer types for his project; Control, Bulk, Interrupt and Isochronous. These classifications are based on frequency of transfer, amount of data to be transferred and the kind of data being transferred.

In USB terminology, individual devices are referred to as *functions*, which are linked in series through *hubs*. The hubs are special-purpose devices that are not considered functions. There always exists one hub known as the root hub, which is attached directly to the host controller.

Endpoints:

Functions and hubs have associated *pipes* (logical channels). Pipes are connections from the host controller to a logical entity on the device named an *endpoint.* The end point thus serves as a data buffer; typically it is a block of data memory or a register in the device; each endpoint can transfer data in one direction only (except endpoint 0), either into or out of the device/function, thus making pipes unidirectional. Every device has endpoint zero configured for bidirectional control transfer. The number of available endpoints and supported transfer types vary with each device. The different kinds of endpoints are Bulk, Control, Interrupt and Isochronous. Since endpoints are unidirectional, they will be followed by an “in” or “out” specification (e.g. Bulk-In).

Device Information:

To identify itself as a USB device and to conform to the spec for a certain class, a device needs to have in its firmware certain elements of information that the host can access in order to successfully enumerate and then communicate with the device. These elements are broadly known as Descriptors and are further classified into:

a. Device descriptor: Information such as the device class, the device sub-class, number of configurations, max packet size and other info about the device as a whole are present in this descriptor.

b. Configuration Descriptor: Information about the number of interface supported and power consumption is provided in this descriptor; most devices usually support only a single configuration, but multiple configurations are allowed.

c. Interface descriptor: Each interface on the device has its own descriptor and subordinate descriptors (descriptors for endpoints used in the interface.

d. Endpoint Descriptors (at least 2): Endpoint descriptors contain information about the endpoints to be used in that interface. This includes maximum packet size, polling rate, endpoint type (Interrupt, Bulk, Control or Isochronous) and endpoint direction (in or out).

e. Report Descriptor: This descriptor is required only in case of HID class devices and contains information on the format of data being transmitted.

f. String Descriptor: Human readable information i.e. messages to be displayed on device enumeration etc are stored in this descriptor. It is optional.

Enumeration:

Before the host can begin using a USB device, it has to learn about the device capabilities, resources and other features in order to assign a device driver. The procedure by which a device identifies itself (including all resources and capabilities available) to the host is known as enumeration. When a function or hub is attached to the host controller through any hub on the bus (including the root hub), it is given a unique 7 bit address on the bus by the host controller. On any USB system all communication is initiated by the host. The host uses a specific set of requests to retrieve required information from the device. These requests can be classified as standard requests and class-specific requests. There are eleven standard requests in the USB. An example of this is Get_Descriptor.

The Get_Descriptor command is used to retrieve descriptors. The Set_Descriptor request lets the host change descriptors in the device.The host controller then polls the bus for traffic, usually in a round-robin fashion, so no function can transfer any data on the bus without explicit request from the host controller.

Frames:

USB establishes a 1 millisecond time base called a frame on a full-/low-speed bus. A frame can contain several transactions. Each transfer type defines what transactions are allowed within a frame for an endpoint. Isochronous and interrupt endpoints are given opportunities to access the bus every N frames. This information is set in the "*bInterval"* or Polling Interval field in the endpoint descriptor. For Bulk endpoints, this filed is not applicable.

2.1 Transfer types

There are four transfer types defined by the USB specification:

2.1.1 Control transfers

Control transfers are facilitated by the device control endpoint (endpoint zero). The host uses control transfers to configure the device, request device information and other settings. Control transfers are different from other transfers in that they have stages; typically three stages. The host sends a request in the Setup stage; the Data stage is used by the host/device to send data (not all requests have this stage) and the device reports the status information in the Status stage. Control transfers may also be used to send vendor specific requests.

2.1.2 Interrupt Transfers

Interrupt transfers are typically non-periodic communication requiring bounded latency. An Interrupt request is queued by the device until the host polls the USB device asking for data. These transfers require an Interrupt-In endpoint on the device.

2.1.3 Bulk transfers:

Bulk transfers can be used for large bursty data. It is ideal in situations where the transfer rate is not critical. Data transfer using bulk transfers are very fast if the bus is idle; if the bus is busy, the transfers are delayed. This type of transfer is supported only by Full-Speed and High-Speed devices and require a Bulk-In endpoint and a Bulk-Out endpoint for data to and from the PC respectively.

2.1.4 Isochronous transfers:

Isochronous transfers occur continuously and periodically. They typically contain time sensitive information, such as an audio or video stream. There is no retry or guarantee of delivery, although for the kind of application it is designed for, loss of a packet or frame does not cause critical issues with application performance e.g. audio or video glitches too small to be noticed by the user. This transfer mode is supported only by Full and High speed USB devices.

Refer to the Universal Serial Bus Specification [b] on usb.org for more details

2.2 The "Bulk-Only" class

USB does not specify a Bulk Only class. During enumeration, the host attempts to load the appropriate driver based on the device class, which is specified in the Device descriptor. However, if the descriptor does not specify a defined USB class (Vendor Defined Class), then no drivers will be loaded. Enumeration will proceed as expected, and the device will declare its resources including endpoints etc. Thus the host is aware of the device capabilities, but does not load a Windows USB class driver, since no class was specified; the user has to provide the driver in this case. In the included Bulk-Only application, the device descriptors have been modified to do just that. A driver is required to access the USB device, which is provided via the libusb-win32 library.

The "Bulk-Only" class is like a psuedo-UART, in the sense that it allows high speed transfer of data over USB without having to enumerate as a defined USB class device. The data to be transferred from the device is loaded into the appropriate driver and the transmit flag is set. When the host polls that endpoint the next time, the data is transmitted. Data reception occurs similarly on the device. The data transfer occurs over the bulk endpoints and is not limited by USB in terms of format or function. It is up to the user application to make sense of data format. Thus operation is very similar to a Mass Storage class device, except for the fact that in Mass Storage devices, the data transferred over the bulk pipes have to conform to a specific format (SCSI); whereas in the Bulk-Only class, raw data can be transferred, since the user writes the host application that makes sense of the data.

2.3 Libusb-win32

Libusb-win32 is an open source library that allows users to access USB devices in their application without having to write OS kernel code. The library has been ported to run on most operating systems including Microsoft Windows. The

website also includes many useful applications, including one that allows creation of a custom .inf file for any device. The function calls are simplistic and allow the user to directly communicate with the Bulk and Interrupt endpoints on the USB device. The library has been ported to most Operating Systems.

The library has been used in the included Bulk-Only application to access the specific USB device.

Refer to the libusb-win32 homepage for more information.

3. Program Description

Below is a layout of different layers of the USB stack

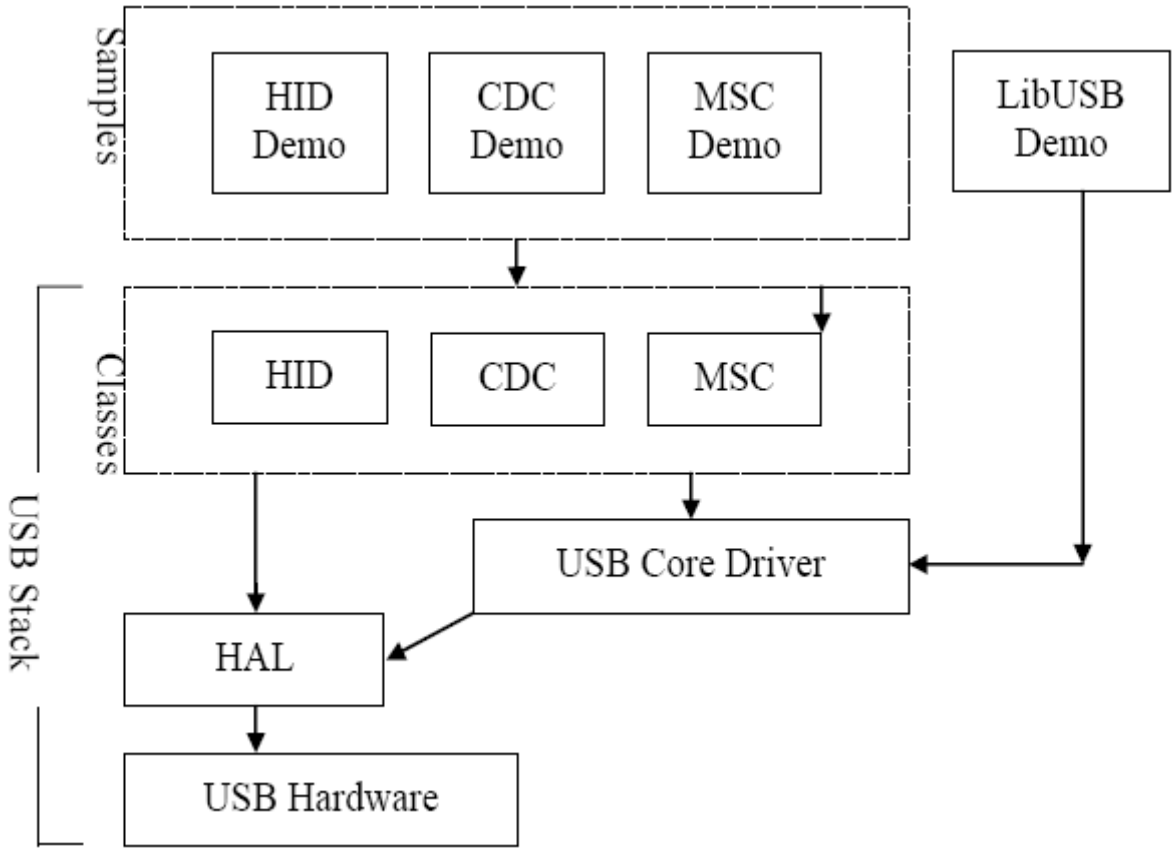

Figure 1: Sample program layout

The USB stack is split into three layers, namely the Hardware Abstraction Layer, the USB Core Layer and the USB Class layer.

The Hardware Abstraction layer interfaces directly with the hardware and provides the higher layers with a uniform hardware independent API. Thus when moving between devices, only the functions in this layer have to be modified since the higher layers are abstracted to the hardware features and operation. This implementation is maintained across all the versions of this program developed for different Renesas devices. The Hal currently supports the following transfer modes

Control (Setup, Data IN/OUT, Status)

Bulk (IN and OUT)

Interrupt (IN)

Isochronous transfer modes are not currently supported.

The USB Core layer implements protocol specific commands and response decoding. This layer uses the HAL layer for actual data transfer and reception. For example the USB Core layer handles the Get_Descriptor requests from the host *This layer can be further expanded to support additional USB host requests* . The HAL layer notifies the USB core layer of USB events via call back functions.

The individual class layer implements functions that are specific to that particular class. In case of the CDC class device, the application support the class requests required for communication over hyper-terminal namely (GET_LINE_CODING, SET_LINE_CODING and SET_CONTROL_STATE)

3.1 Configuring the device for different USB events

The following section talks about the operation of the USB clock and how to configure the registers to respond to different USB events

3.1.1 Interrupt Vectors

This device has a total of 5 USB interrupt vectors.

- Vector 232; USBINTN0
- Vector 233; USBINTN1
- Vector 234; USBINTN2
- Vector 235; USBINTN3
- Vector 238; RESUME

All USB events are channeled through these interrupt vector. In the ISR, the user has to check the flag register to determine the actual cause of the interrupt. USBINTN0 and USBINTN1 are only required when combining USB and DMAC transfers. In the included sample program, this feature is not used.

The RESUME signal is used to wake the device out of software stand-by mode. This is useful in applications where the device has to go into low power and will be waken up remotely when required.

All of the remaining interrupts are channeled though USBINTN2 and USBINTN3.

3.1.2 Initialization

This section lists the initialization sequence for the USB block

(a) **Pin Configuration**

This Device has a total of 5 USB pins all of which are dedicated for USB operation and hence do not need to be configured as inputs or outputs.

- VBUS
- DrVSS
- USD-
- USD+
- DrVCC

During initialization, before enabling the pull-up for USBD+, the port is forced low. This is to ensure that if the USB device is already plugged in before the software runs, then the forced pull down and release will start the enumeration process.

(b) **Module Enable**

By default, all peripheral modules including USB are disabled on the H8SX/1664.

To access any USB registers, the module needs to be enabled by setting `MSTP._CRC.BIT._USB = 0`

(c) **Clock Configuration**

Once the initialization is done, the device has to be configured to respond to different USB events. The following sections explain the configuration required to respond to each of the different USB events.

3.1.3 Cable Connection/Disconnection

When properly configured, this LSI generates an interrupt to the CPU when the USB cable is plugged in or disconnected. To enable this interrupt, the VBUSF bit in IER1 has to be set (`USB.IER1.BIT.VBUSF = 1`).

Since this interrupt is usually followed by the Bus Reset interrupt, ensure that this is enabled as well by setting the BRST bit in IER0 (`USB.IER1.BIT.VBUSF = 1`).

Since both of these interrupts are routed via USBINTN2, in the interrupt handler check the flag registers to determine the interrupt source (`USB.IFR1.BIT.VBUSF` and USB.IFR0.BIT.BRST). In case of the VBUS interrupt, clear the flag register, notify the software layer, and if the cable is connected, initialize the data elements used by the software stack.

When the Bus Reset interrupt occurs after this, make sure to initialize the block by clearing all the FIFOs and stall states. This is done by

```
USB.FCLR.BYTE = 0x73;    /* Clear FIFOS   */
USB.EPSTL.BYTE = 0x00;   /* Clear all stalls */
```

3.1.4 Control Transfer

Once the Bus Reset has occurred, the enumeration process begins. The details of the enumeration process and the control transfer used for this process are described in section 2.1.1.

(a) **Setup Stage**

When the host sends the SETUP command, if the SETUPTS bit in IER0 has been set, the device will issue an interrupt request. The source can be determined by interrogating the SETUPTS bit in the flag register IFR0. Since the reception of the Setup command packet indicates the start of a new command sequence, it is necessary to flush out the FIFOs to prevent the software from reading data packets from a prior command. Once this is done, read all the 8 byts of the Setup packet and notify the higher layer for processing. Then set the hardware bit indicating that the 8 bytes have been read. This is done as shown below:

```
  /*Clear EP0i and EP0o FIFOs*/
USB.FCLR.BYTE = 0x03;/* EP0oCLR = 1 and EP0iCLR = 1 */
  /*Read 8 bytes of data from EP0 into tempory buffer*/
  for(index = 0; index < USB_SETUP_PACKET_SIZE; index++)
  {
   SetupCmdBuffer[index] = USB.EPDR0s;
  }
  /*Set EP0 Status Read Complete*/
  USB.TRG.BIT.EP0sRDFN = 1;
```

The H8S/1664 USB block automatically decodes the following Setup commands. These commands do not generate an interrupt request to the CPU and all three stages including command, data and status stages are automatically processed by the hardware.

- Clear Feature
- Get Configuration
- Get Interface
- Get Status
- Set Address
- Set Configuration
- Set Feature
- Set Interface

The following commands require firmware support to proceed with the subsequent stages. An interrupt request is generated when these commands are received.

- Get Descriptor
- Class/Vendor commands
- Set Descriptor
- Sync Frame

If the application does not support a particular command, the slave can respond by setting the Control endpoint to a “stall” state. This will cause the block to send a “stall” packet to the host indicating that the particular command is not

supported. The stall state can also be used by other endpoints to let the host know that it is not yet ready to respond to further host requests. These two stall states are known as *protocol stall* and *commanded stall* respectively.

(b) **Control-Data Stage**

As mentioned in section 2.1.1, the command stage is followed by an optional data stage and a mandatory status stage. Depending on the command sent during the Setup stage, there may be a Data-IN or Data-OUT stage. An important thing to remember is that the subsequent *Status stage has a direction opposite to the preceding Data stage*. The interrupt sources are configured based on this.

To handle Data-IN, enable the EP0iTS and EP0oTS interrupts. The data is sent to the host via the EPDR0i register. If there are more packets still to send, the deice waits for either the EP0iTS interrupt (indicating that the host is asking for the rest of the data) or the EP0oTS interrupt (indicating that the host is done and now sending the Status). Once all the packets have been sent, set the EP0iPKTE bit to indicate to the host that all the data has been sent.

The EP0iTR (Request for information by the host) interrupt will not be used in this case since the host requests for further data packets by means of the EP0iTS interrupt. And since the subsequent Status stage will consist of *receiving* information from the host, the EP0iTR is not required.

To handle Data-OUT, enable the EP0iTS, EP0oTS and the EP0iTR interrupts. The data from the host is received on the EPDR0o register. Once the data has been read, set the EP0oRDFN to indicate to the host that it has been read so that the next packet can be sent by the host. Once all the data has been read, the host attempts to read the Status from the device. This will cause the EP0iTR interrupt to trigger.

(c) **Control-Status Stage**

The direction of the Status stage is opposite to that of the preceding data stage (if there was one) or the Setup stage. If the host has requested for the status by means of the EP0iTR interrupt, then the device will send one of the following packets depending on the outcome of the process: ACK, NAK or STALL. The ACK is generated by sending a zero-byte packet to the host. This is done by setting the EP0iPKTE bit without writing anything to the EPDR0i register.

Conversely, if the host is the source of the Status stage, then the EP0oTS interrupt will trigger on receiving an ACK.

3.1.5 Bulk-In Transfer

On the H8SX/1664, endpoint 2 is the Bulk-IN endpoint. Interrupts requests for this endpoint are enabled by setting the EP2TR bit.

When the host wants to receive over this endpoint, it sends a request which triggers the EP2TR interrupt. In the interrupt handler, the application writes out a packet to the EPDR2 register byte by byte and then sets the EP2PKTE bit so that the data is sent to the host. Once the data is successfully sent, the interrupt will be retriggered. The application will then write out any more remaining packets and repeat the process until all the data is sent to the host.

If at any point the EP2PKTE bit is set without writing a full packet worth of data (64 bytes for this device) to EPDR2, then the host will consider this as an indication that the device has finished sending all the available data.

If then total data to be sent is a multiple of 64, then to end the transmission, send an empty packet by setting the EP2PKTE bit without writing any data to EPDR2.

3.1.6 Bulk-Out Transfer

On the H8SX/1664, endpoint 1 is the Bulk-OUT endpoint. Interrupts requests for this endpoint are enabled by setting the EP1FULL bit.

When the host sends data over this endpoint, the EP1FULL interrupt is triggered. The total size of the data sent by the host is in the EPSZ1 register and the actual data in the EPDR1 register. Once the application reads out all the data from the register, it sets the EP1RDFN bit to indicate to the host that all the data has been read out.

3.1.7 Interrupt-In Transfer

On the H8SX/1664, endpoint 3 is the Bulk-OUT endpoint. Interrupts requests for this endpoint are enabled by setting the EP3TR the EP3TS bits.

To send data to the host over this endpoint, the application writes a packet (or less) worth of data to the EPDR3 register one byte at a time and then sets the EP3PKTE bit to send the data. If a full packet was sent, the EP3TS interrupt will be generated again indicating that the data was sent and the host is requesting the rest of the data. The procedure is repeated until all the data is sent or until the EP3PKTE bit is set without writing a full packet worth of data to the EP3DR register.

If the host attempts to read the EP3DR register and finds no data in the buffer, the EP3TR interrupt will be triggered. This case is not handled in the provided sample code and hence this interrupt is disabled.

4. Using the software in your application

The sample program uses the Bulk Endpoints to send and receive “raw” data. This means that the format of the data is not specified by USB and the user thus has plenty of flexibility in sending and receiving any kind of data including custom commands.

There are primarily two functions in firmware that are used to send and receive data over the bulk pipes

- `USBHAL_Bulk_OUT()`
- `USBHAL_Bulk_IN()`

The stack provides a debugging layer which outputs debug messages over the serial port. This can be enabled or disabled by defining the project level macros VERRBOSE_HIGH, VERBOSE_MID and VERBOSE_LOW.

Refer to the sample program on how to initialize the hardware and stack before using the API.

Reference

a. H8SX/1664 group manual. Document number: REJ09B0294
b. Universal Serial Bus Specification Revision 2.0
c. "USB Complete: Everything You Need to Develop Custom USB Peripherals" by Jan Axelson.
d. libusb-win32 homepage

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