

Renesas RA Family

Usage of Schmitt Trigger Input Pins on RA2E1

Introduction

This document answers common questions and points out subtleties in the usage of the Schmitt Trigger Input Pins on the RA2E1 that might be missed unless the hardware manual was extensively reviewed. This document is not intended to be a replacement for the hardware manual. It is intended to supplement the manual by highlighting some key items that most engineers will need to start their own design. It also discusses some design decisions from an application point of view.

Target Device

RA2E1

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1. Usage of Schmitt Trigger Input Pins

GPIO used as normal Input has no Schmitt Trigger as described in the hardware manual. However, it can be used as Input Pins with a Schmitt Trigger with the following restriction. Kindly ensure that you thoroughly evaluate in your own environment before use.

First set bit 16, PMR = 1 in the Port mn Pin Function Select Register.

The following Input Pins have Schmitt Trigger Input capability. This Schmitt Trigger Input capability is usable by the following considerations:

1. The peripheral functions must be selected for the individual Input Pin, but peripheral functions cannot be used once Schmitt Trigger Input capability is selected.
2. With PMR = 1 current consumption may increase compared to using PMR = 0.

1.1 Settings for Using Peripheral Mode

Table 1.1 Register settings for input/output pin function (PORT0)

PSEL[4:0] settings	Function	Pin										
		P000	P001	P002	P003	P004	P010	P011	P012	P013	P014	P015
00000b	(initial)	—	—	—	—	—	—	—	—	—	—	—
01100b	CTSU	—	—	—	—	—	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—
ISEL bit		✓	✓	✓	—	✓	—	—	—	—	—	✓
NCODR bit		—	—	—	—	—	—	—	—	—	—	—

✓ : Available
 —: Setting prohibited

Table 1.2 Register settings for input/output pin function (PORT1)

PSEL[4:0] settings	Function	Pin													
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113
0000b	(initial)	—	—	—	—	—	—	—	—	✓	—	—	—	—	—
0000b	AGT	✓	✓	✓	—	—	—	—	—	—	—	—	✓	✓	—
0001b	GPT	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓	—	—	—
0001b	GPT	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓	✓	✓	—
0010b	SCI	✓	✓	✓	—	✓	—	—	—	—	✓	—	✓	✓	—
0010b	SCI	✓	—	✓	—	—	—	—	—	—	✓	✓	✓	✓	—
0011b	SPI	✓	✓	✓	✓	✓	✓	✓	—	—	—	—	—	—	—
0011b	IIC	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—
0100b	KINT	✓	✓	✓	✓	✓	✓	✓	✓	—	—	—	—	—	—
0100b	CLKOUT/ ACMPLP /RTC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
0101b	CAC/ ADC12	—	—	✓	—	—	—	—	—	—	—	—	—	—	—
0110b	CTSU	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL bit		✓	✓	—	—	✓	✓	—	—	—	—	✓	✓	—	—

✓ : Available
 — : Setting prohibited

Table 1.3 Register settings for input/output pin function (PORT2) (1 of 2)

PSEL[4:0] settings	Function	Pin										
		P200	P201	P204	P205	P206	P207	P208	P212	P213	P214	P215
0000b	(initial)	—	—	—	—	—	—	—	—	—	—	—
0000b	AGT	—	—	✓	✓	—	—	✓	✓	—	—	—
0001b	GPT	—	—	✓	✓	✓	—	—	✓	✓	—	—
0001b	GPT	—	—	—	—	—	—	—	✓	✓	—	—
0010b	SCI	—	—	✓	✓	✓	—	—	—	—	—	—
0010b	SCI	—	—	✓	—	—	—	—	✓	✓	—	—
0011b	SPI	—	—	—	—	—	—	—	—	—	—	—
0011b	IIC	—	—	✓	—	—	—	—	—	—	—	—
0100b	CLKOUT/ ACMPLP/R TC	—	—	—	—	—	—	—	—	—	—	—
0101b	CAC/ADC12	—	—	✓	—	—	—	—	—	—	—	—

✓ : Available
 — : Setting prohibited

Table 1.4 Register settings for input/output pin function (PORT2) (2 of 2)

PSEL[4:0] settings	Function	Pin										
		P200	P201	P204	P205	P206	P207	P208	P212	P213	P214	P215
0110b	CTSU	—	—	—	—	—	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—
ISEL bit		—	—	—	✓	✓	—	—	✓	✓	—	—

✓ : Available
 — : Setting prohibited

Table 1.5 Register settings for input/output pin function (PORT3)

PSEL[4:0] settings	Function	Pin				
		P300	P301	P302	P303	P304
00000b	(initial)	✓	—	—	—	—
00001b	AGT	—	✓	—	—	—
00010b	GPT	✓	✓	✓	—	—
00011b	GPT	✓	✓	✓	—	—
00100b	SCI	—	✓	✓	—	—
00101b	SCI	—	—	—	—	—
00110b	SPI	—	—	—	—	—
01100b	CTSU	—	—	—	—	—
ASEL bit		—	—	—	—	—
ISEL bit		—	✓	✓	—	—

✓ : Available

—: Setting prohibited

Table 1.6 Register settings for input/output pin function (PORT4) (1 of 2)

PSEL[4:0] settings	Function	Pin								
		P400	P401	P402	P403	P407	P408	P409	P410	P411
00000b	(initial)	—	—	—	—	—	—	—	—	—
00001b	AGT	✓	—	✓	✓	✓	—	—	✓	✓
00010b	GPT	—	✓	—	—	—	✓	✓	✓	✓
00011b	GPT	✓	✓	—	—	—	—	—	—	—
00100b	SCI	✓	—	—	—	—	—	—	✓	✓
00101b	SCI	✓	✓	✓	—	—	—	—	—	—
00110b	SPI	—	—	—	—	—	—	—	✓	✓
00111b	IIC	✓	✓	—	—	✓	✓	—	—	—
01001b	CLKOUT/ ACMPLP/RTC	—	—	—	—	✓	—	—	—	—

✓ : Available

—: Setting prohibited

Table 1.7 Register settings for input/output pin function (PORT4) (2 of 2)

PSEL[4:0] settings	Function	Pin								
		P400	P401	P402	P403	P407	P408	P409	P410	P411
01010b	CAC/ADC12	✓	—	—	—	✓	—	—	—	—
01100b	CTSU	—	—	—	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—
ISEL bit		✓	✓	✓	—	—	✓	✓	✓	✓

✓ : Available

—: Setting prohibited

Table 1.8 Register settings for input/output pin function (PORT5)

PSEL[4:0] settings	Function	Pin		
		P500	P501	P502
00000b	(initial)	—	—	—
00010b	GPT	✓	✓	✓
00011b	GPT	✓	✓	—
00101b	SCI	—	✓	✓
ASEL bit		—	—	—
ISEL bit		—	—	—

✓ : Available
 —: Setting prohibited

Table 1.9 Register settings for input/output pin function (PORT9)

PSEL[4:0] settings	Function	Pin		
		P913	P914	P915
00000b	(initial)	—	—	—
00001b	AGT	✓	✓	—
00010b	GPT	✓	✓	—

✓ : Available
 —: Setting prohibited

1.2 Steps for Setting and Using Peripheral Mode

1. Set prohibit for peripheral mode.
2. Clear PWPR_BOW1 to enable write to PWPR_PFSWE.
3. Set PWPR_PFSWE to enable PmmPFS.
4. Set PmmPFS.PSEL[4:0] for the peripheral that you choose to use.
5. Set PMR = 1 (to set peripheral mode).
6. Clear PWPR_PFSWE to prohibit writing to PmmPFS.
7. Set PWPR_BOW1 to prohibit writing to PWPR_PFSWE.
8. Then, you can read port with Schmitt characteristics.

*Note: With PMR = 1 current consumption may increase compared to using PMR = 0.

Software Code Example - Setting Port P100 (AGT) to Schmitt Trigger Inputs

Table 1.2 Register settings for input/output pin function (PORT1)

PSEL[4:0] settings ^{a2}	Function ^{a3}	Pin ^{a3}													
		P100 ^{a3}	P101 ^{a3}	P102 ^{a3}	P103 ^{a3}	P104 ^{a3}	P105 ^{a3}	P106 ^{a3}	P107 ^{a3}	P108 ^{a3}	P109 ^{a3}	P110 ^{a3}	P111 ^{a3}	P112 ^{a3}	P113 ^{a3}
00000b ^{a3}	(initial) ^{a3}	— ^{a3}								✓ ^{a3}					
00001b ^{a3}	AGT ^{a3}	✓ ^{a3}	✓ ^{a3}	✓ ^{a3}	— ^{a3}	— ^{a3}	— ^{a3}	— ^{a3}	— ^{a3}	— ^{a3}	— ^{a3}		✓ ^{a3}	✓ ^{a3}	— ^{a3}

- For a pin with IRQ functionality, the Schmitt Trigger functionality can be enabled with the following code example:

```
R_IOPORT_PinCfg(&g_ioport_ctrl, BSP_IO_PORT_00_PIN_00,
  (uint32_t) (IOPORT_CFG_IRQ_ENABLE));
```

For a pin for which enabling the AGT enables the Schmitt trigger functionality:

```
R_IOPORT_PinCfg(&g_ioport_ctrl, BSP_IO_PORT_01_PIN_02,
  (((uint32_t) IOPORT_CFG_PORT_DIRECTION_INPUT) |
  ((uint32_t) IOPORT_CFG_PERIPHERAL_PIN | (uint32_t) IOPORT_PERIPHERAL_AGT)));
//set to input
// & set PMR to Schmitt Trigger input
// & select AGT
```

2. Website and Support

Visit the following URLs to learn about key elements of the RA family, download components and related documentation, and get support:

RA Product Information	renesas.com/ra
RA Product Support Forum	renesas.com/ra/forum
RA Flexible Software Package	renesas.com/FSP
Renesas Support	renesas.com/support

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Oct.19.23	—	Initial release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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