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RENESAS

Application Note

Usage and Applications of μPC8119T and μPC8120T

Variable-gain High-frequency Amplifier Silicon MMIC for AGC Unit of Mobile Communications

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[MEMO]

The information in this document will be updated without notice.

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

This document provides the general outline of the products, i.e., the design concepts for the external circuits that must be directly connected to the products. The quality and characteristics described in the Data Sheet of these products are guaranteed but NEC takes no responsibility for your design and application using these products.
Therefore, design external circuits on your own responsibility by referring to this document and in accordance with the planned system requirements, and confirm the characteristics of your application circuit.

[MEMO]

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PRECAUTIONS FOR DESIGN-INS

(1) Observe precautions for handling because of electro-static sensitive devices.

(2) Form as wide a ground pattern as possible to minimize the ground impedance. Especially, connect patterns to avoid generating different impedance among the ground pins.

(3) Insert a feedback capacitor (of 1000 pF for example) between the V_{CC} and AGC pins.

(4) Insert a π type circuit consisting of a series inductor and two parallel capacitors (4.7 nH and 1000 pF for example) outside the feedback capacitor of the V_{CC} pin.

(5) Connect an external LC matching circuit including a parallel inductor to the output pins. The RF ground of the parallel inductor must be the π type circuit opposite to the V_{CC} pin.

(6) The DC cut capacitor must be attached to the input pin. Do not externally adjust the pin voltage.

[MEMO]

1. PREFACE

Mobile telephones have rapidly become widespread and radio communications have become popular in recent years. Because mobile telephones perform radio communication at high frequencies, demand for high-frequency ICs is growing. In addition, these high-frequency ICs also require low current in order to realize longer talk time and waiting time. Moreover, they are also required to be low-cost and be able to be densely mounted on a printed circuit board in order to create compact application systems.

To satisfy these requirements, NEC has developed variable-gain amplifier ICs for transmission AGC of silicon MMICs, namely the μPC8119T and μPC8120T. Because the circuits of these products are designed as to allow you to adjust the external components such as inductors and capacitors, the relation between the external components and internal circuits must be clearly grasped. This document explains the approach toward designing application systems of these ICs.

2. PRODUCT OUTLINE

The μPC8119T and μPC8120T are silicon microwave monolithic ICs developed for the transmission-stage AGC of mobile communications equipment. The gain of these ICs can be varied by an external control circuit. The μPC8119T is for forward control and the μPC8120T is for reverse control. Both the products are packaged in a 6-pin mini-mold for high-density and surface mounting. The operating frequency can be adjusted by external matching constants to the output pins. Both products have an operating frequency range of 100 MHz to 1.9 GHz. At first, these products were developed for PDC800 M/1.5 G, but they are actually used not only in PDC but also in PHS because they can operate at up to 1.9 GHz.

Because these ICs are variable gain amplifiers, the user must prepare an external control circuit such as an AGC detector circuit when AGC operation is to be performed. This external control circuit may be an ordinary circuit and not limited in any way, and no special circuit is recommended.

The details of specifications and characteristic curves of these ICs should be referred to their Data Sheets.

3. PRODUCTION PROCESS

NEC's original silicon bipolar process NESAT-III is employed as the production process of both the μPC8119T and μPC8120T. The features of this production process are briefly explained below.

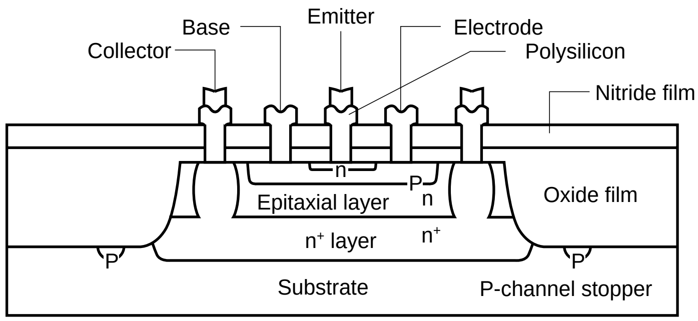
<1> High f_T (gain bandwidth product) of 20 GHz is realized by reducing the emitter junction thickness of the transistor.

<2> Low noise and high gain by minimizing the emitter width (0.6 μm) and base junction thickness of the transistor and thereby lowering the base resistance and E-B junction capacitance.

<3> High reliability, including moisture proofness, through employment of direct nitride film structure by which the base and emitter surfaces are covered with a nitride film via a thin oxide film.

Because of these features, NESAT-III is suitable for producing low-voltage ICs with excellent electrical characteristics.

Figure 3-1. Cross-Sectional View of Transistor Created by NESAT Process (internal element of IC)

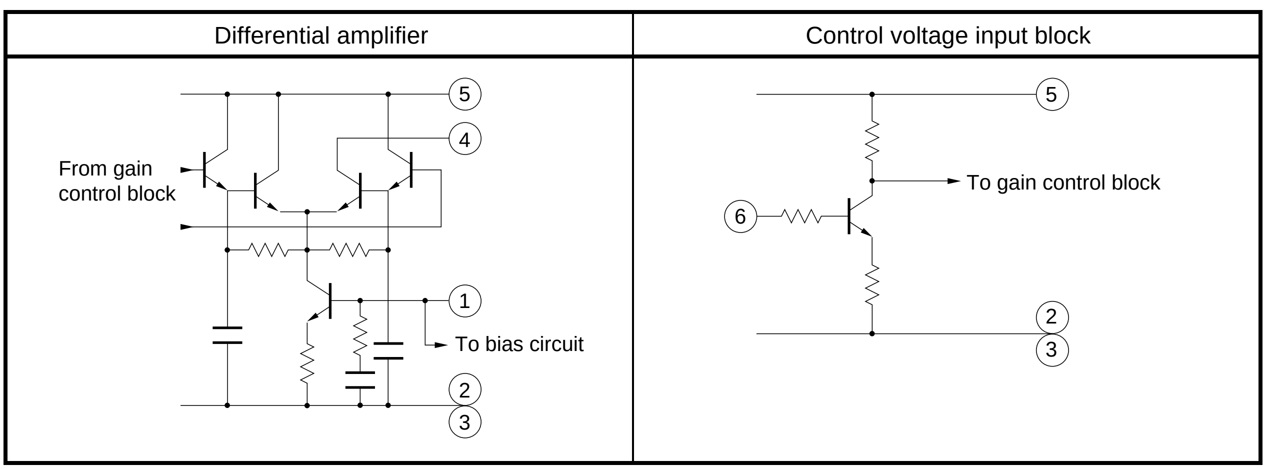


4. INTERNAL CIRCUIT CONFIGURATION AND OPERATION

Figure 4-1 shows the internal equivalent circuit of the μPC8119T and μPC8120T. The internal circuits of the μPC8119T and μPC8120T are identical except for the internal control circuit.

Both the μPC8119T and μPC8120T are differential amplifiers and vary the gain by changing the current proportion of the differential transistor pairs of control circuit side and output side. The output pins are of the open-collector of the output transistor and externally configure a matching circuit. The same voltage as V_{CC} is applied to the output pin as a bias via the inductor of the matching circuit. The circuit current is the sum of the current into V_{CC} pin and into the output pin. Although the proportion of these circuit current changes with the control voltage, the sum of the current into the output pin and into the V_{CC} pin is constant. The current into the V_{CC} pin is minimum at the maximum gain, and maximum at the minimum gain (at maximum attenuation). Conversely, the current into the output pin is maximum at the maximum gain, and minimum at the minimum gain (at maximum attenuation). To get maximum gain, AGC control voltage should be minimized on μPC8119T of forward control type but should be maximized on μPC8120T of reverse control type. (Refer to the **characteristic curves** in **Data Sheet**.) The explanation here can be summarized in the Table 4-1.

Figure 4-1. Equivalent Circuit of Internal Block



Remark The gain control block is not described at element level because the internal design of the IC is confidential.

Table 4-1. Operational Differences between μPC8119T and μPC8120T

DC Parameters	Operation		Part Number
	At maximum gain	At minimum gain	
AGC control voltage (forward control)	Minimum	Maximum	μPC8119T
Current into V_{CC} pin	Minimum	Maximum	
AGC control voltage (reverse control)	Maximum	Minimum	μPC8120T
Current into output pin	Maximum	Minimum	

5. EXTERNAL CIRCUIT CONFIGURATION

Figures 5-1 and 5-2 show an example of external circuit configuration and an example of configuration on an evaluation board. With these ICs, the external capacitors connected to the V_{CC} line and V_{AGC} pin determine the minimum gain, and the output matching circuit determines the maximum gain.

The external circuit of each pin is explained in detail below.

5.1 V_{CC} Line and V_{AGC} Pin (Determining minimum gain)

The output pin is the collector of the differential output transistor, so the bias is applied to the output pin by connecting an inductor to the V_{CC} line that is connected to the V_{CC} pin, which is another collector of the differential control circuit. Unless an external circuit is connected so that the V_{CC} line is the load, therefore, the high-frequency signal from the V_{CC} pin leaks to the output pin at the minimum gain (because the current of the transistor at the control side is maximum at the minimum gain). It is therefore necessary to optimize the feedback by inserting a feedback capacitor between the V_{CC} and AGC pins and by inserting a π type circuit consisting of a series inductor and two parallel capacitors outside the feedback capacitor of the V_{CC} pin. As a result, the leakage of the high-frequency signal from the V_{CC} pin can be attenuated. Without the feedback capacitance, the minimum gain increases about 10 dB. Without the π type circuit, it increases about 20 dB. You, however, should note that this feedback capacitance is affected by variations of the products if its value is too small to have frequency characteristics. In the test circuit shown in the Data Sheet, each capacitance is 1000 pF which value is insensitive to characteristics in VHF band. In the Data Sheet, a test circuit using a jumper line or pattern L as the series inductor of the π type circuit is shown. This circuit is for simple evaluation and actually, a multi layer chip inductor of 4.7 nH can be used.

5.2 Output Matching (Determining maximum gain)

Because these ICs are of the open-collector output type, configure an LC matching circuit for RF impedance with external components. The matching circuit consists of a parallel inductor at the V_{CC} side and a series capacitor toward the following stage. The collector of the output pin is biased by the voltage on the V_{CC} pin via an inductor for RF matching, as described above. Consequently, the inductor connected to the output pin has two effects: RF effect of frequency matching and DC effect of applying a bias. Therefore, use a high-frequency inductor with a low DC resistance. The LC value should be determined by referring to the S parameter at the maximum gain of the IC, so that a power gain is obtained in a narrow region according to the operating frequency. Select a value so that S22 drops to –20 dBm at the maximum gain of the frequency band used. To bias the inductance connected to the output pin, connect the output pin to the outside of the π type circuit (not to the IC side) connected to the V_{CC} line (otherwise, the high-frequency signal from the V_{CC} pin leaks out to the output pin and the minimum gain will not be available below this leak level).

5.3 Input Pin

The impedance of the input pin is relatively low but is higher than 50 Ω. The presence or absence of matching should be determined by the impedance of the preceding stage. The bias must not be externally applied to input pin.

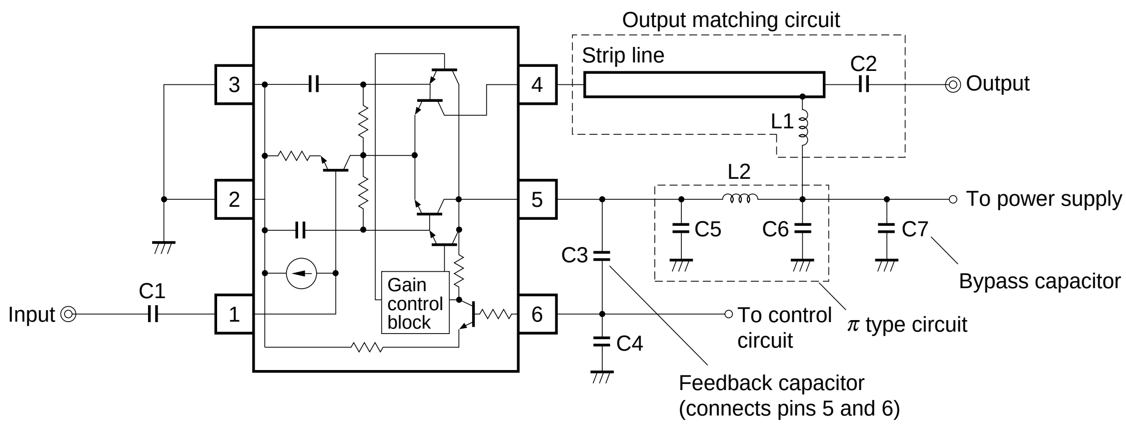
Figure 5-1. Example of External Circuit Configuration

Matching at f = 950 MHz or 1440 MHz

C1, C3 through C7 : 1000 pF

L2 : 4.7 nH

Determine L1 and C2 based on the S parameter of pin 4, including the strip line length of the board and according to the frequency. Connect output matching inductor L1 to outside the π type circuit (not to the IC side).



Determine whether matching is necessary for input, depending on the relation with the impedance of the preceding stage.

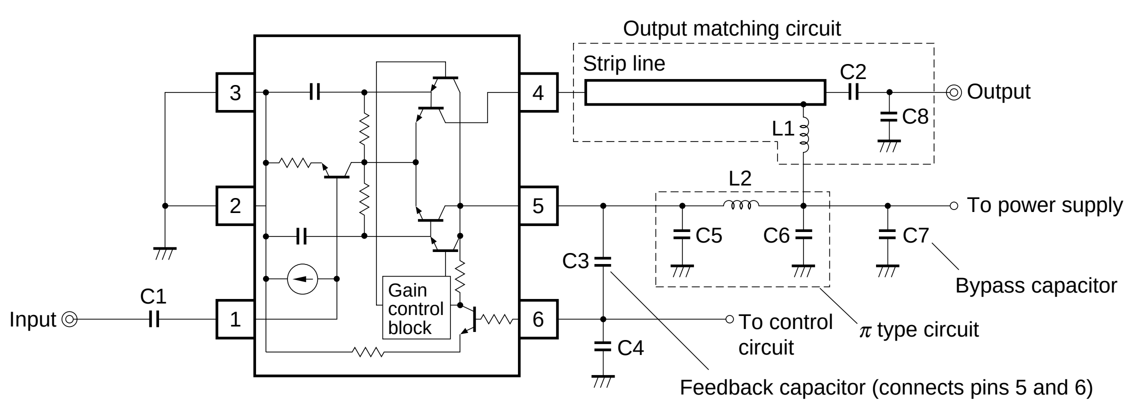
The output matching is of high-pass type. The circuit format is the same at 950 and 1440 MHz. The output matching constants differ depending on the frequency used.

Matching at f = 1900 MHz

C1, C3 through C7 : 1000 pF

L2 : 4.7 nH

Determine L1, C2, and C8 based on the S parameter of pin 4, including the strip line length of the board and according to the frequency. Connect output matching inductor L1 to outside the π type circuit (not to the IC side).



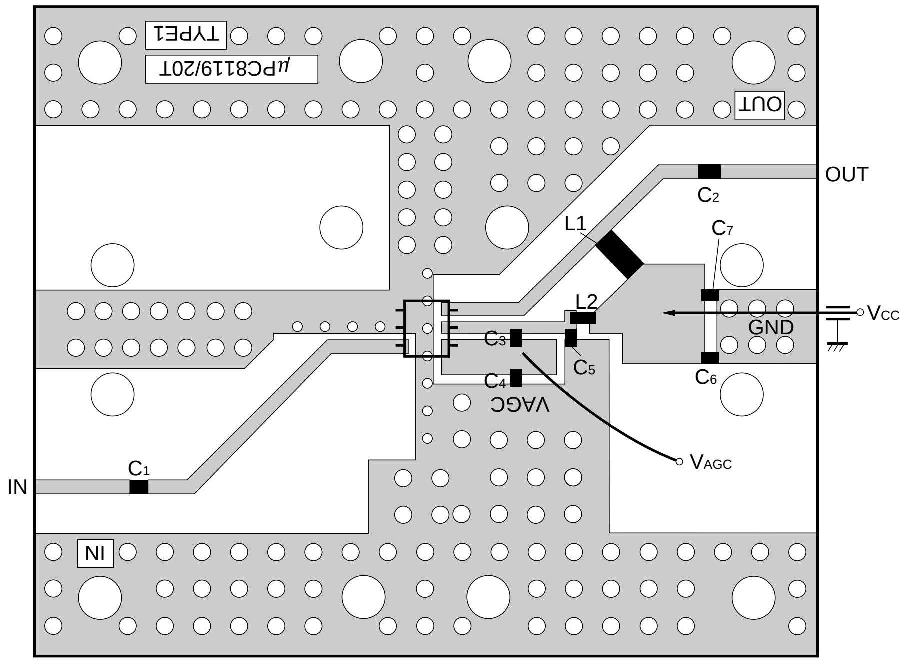
Determine whether matching is necessary for input, depending on the relation with the impedance of the preceding stage.

The output matching is of low-pass type. The minimum gain is higher than that shown in the Data Sheet in the case of high-pass matching.

Figure 5-2. Example of External Circuit Configuration on Evaluation Board

(a) On TYPE1 board

Matching at f = 950 or 1440 MHz



- Example of using multi layer chip inductor as each inductor
- Inductor L1 of output matching circuit consists of one chip with optimum L value[Note].

Matching at f = 1900 MHz

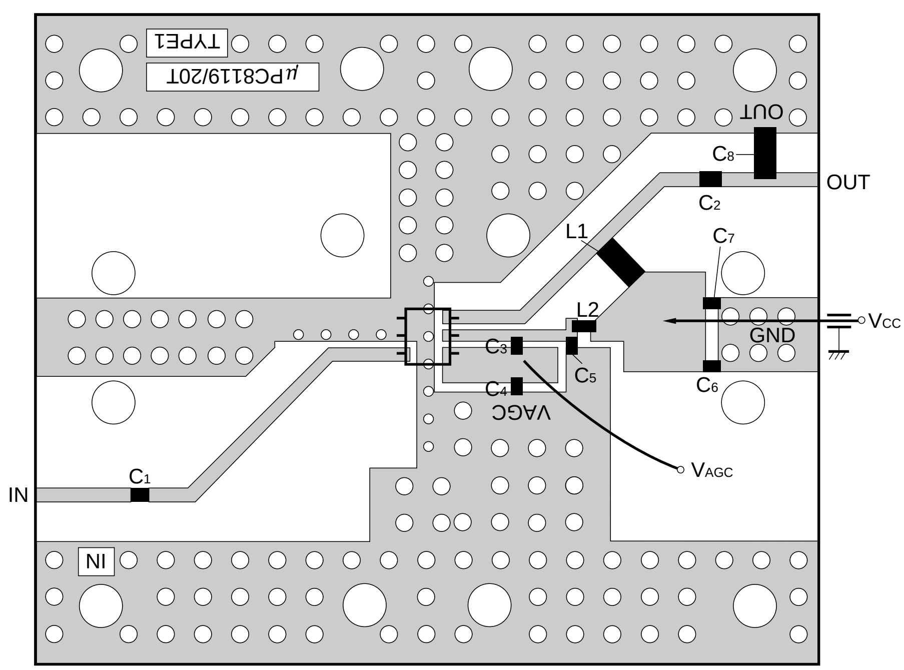
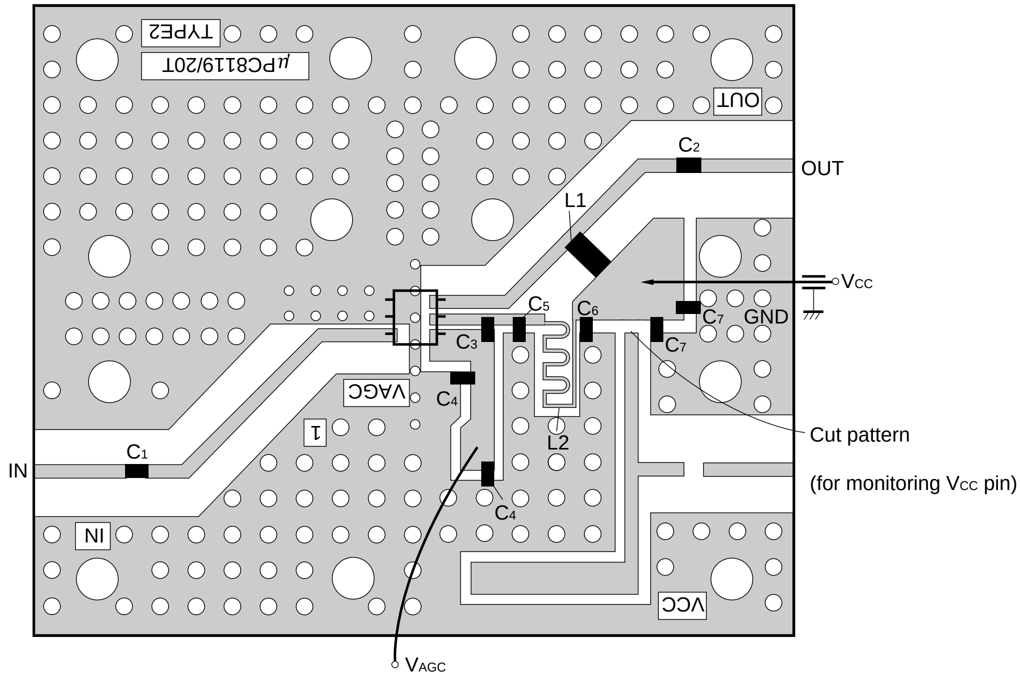


Figure 5-2. Example of External Circuit Configuration on Evaluation Board

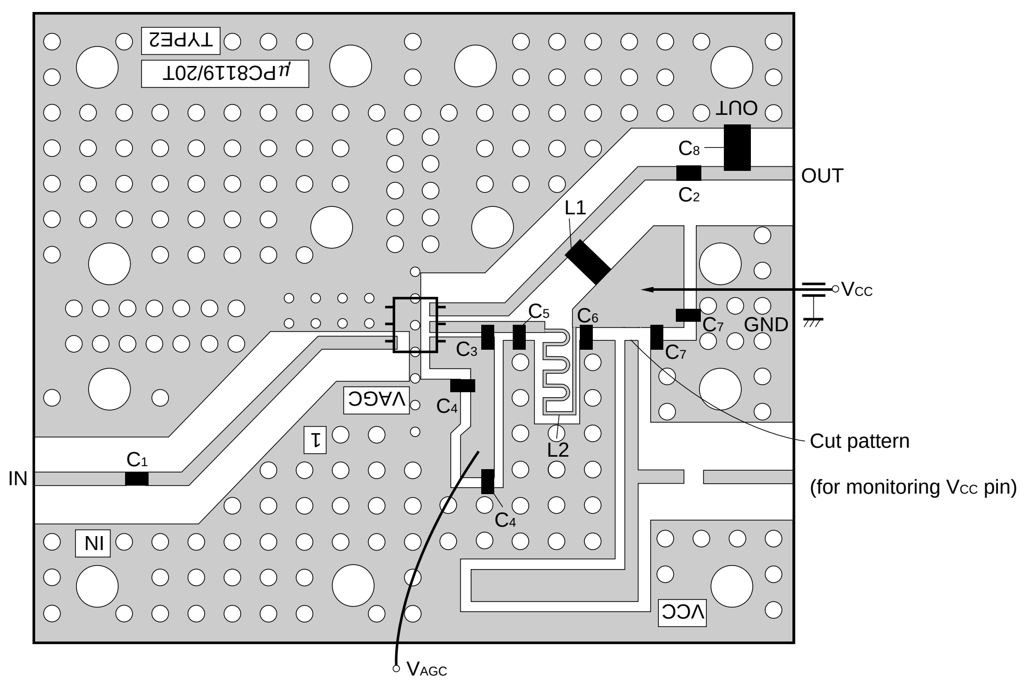
(b) On TYPE2 board

Matching at f = 950 or 1440 MHz



- Example of configuration of L2 on board pattern (Equivalent to 5 nH)
- Inductor L1 of output matching circuit consists of one chip with optimum L value[Note].

Matching at f = 1900 MHz



Note In the example of mounting on a printed circuit board in the test circuit in the Data Sheet, more than one inductor L1 for output matching is connected in parallel. Because the test circuit is an NEC test fixture for inspection and because there is no optimum L value for the inspection fixture, the necessary L value is created by connecting plural L1s in parallel. In actual application by the user, the optimum L value can be obtained by using one chip inductor as described in 5.4.

Remark Evaluation board

The following two types of evaluation boards are available for these ICs. Because the patterns on these boards are used for an inspection fixture that easily confirms the characteristics of the ICs, and because components cannot be mounted in the vicinity of the ICs, the pattern size is greater than the actual size. This means that these patterns are not recommended patterns.

Table 5-1 shows the major differences of the two types of evaluation boards: TYPE1 and TYPE2. Because TYPE1 can mount an external inductor to the π type circuit of the V_{CC} line, it can evaluate whether this inductor is provided or the dependency of the L value.

TYPE2 can evaluate whether the characteristics can be ensured by using the inductor of about 5 nH of the power supply π type circuit as pattern L when the number of components is reduced. In addition, because a V_{CC} pin monitor line is provided, the leakage from the V_{CC} pin can be also evaluated.

The constants of the mounted components for output matching and type differ depending on the frequency used, and TYPE is not divided by the part number or frequency. When purchasing an evaluation board, specify the type No. by referring to Table 5-1.

Table 5-1. Types of Evaluation Boards

Type Name (inscribed on pattern)	Features
μPC8119/20T TYPE1	Can connect external inductor to π type circuit of V_{CC} line
μPC8119/20T TYPE2	Pattern L equivalent to 5 nH is printed for π type circuit of V_{CC} line.

Notes on evaluation board (common to TYPE1 and TYPE 2)

(1) 35-μm thick copper patterning on both sides of 35 × 42 × 0.4 mm polyimide board

(2) GND pattern on rear side

(3) Solder-plated patterning side

(4) ∘ ○: Through hole

Design the actual print pattern depending on the material of your board and frequency. For foot print and mount pad dimensions, refer to **Semiconductor Device Mounting Technology Manual (C10535E).**

5.4 Parameters for Matching Circuit Designing

The matching circuit constants shown in the Data Sheet are for the evaluation board also shown in the Data Sheet. This evaluation board is for simple evaluation only and it is considered to be impossible to apply this board in an actual system. For your reference for designing a matching circuit, Figure 5-3 shows the S parameter values (MAG and ANG) of the μPC8119T and μPC8120T (without matching) and an input/output Smith chart. It is recommended that matching be created based on the parameters at the maximum gain, so that the maximum gain of these ICs are ensured. For this reason, the parameters shown in Figure 5-3 are at the maximum gain (changes in the impedance at the minimum gain poses no problem to the actual application). Optimize the matching circuit constants by considering these parameters and the mounting board element.

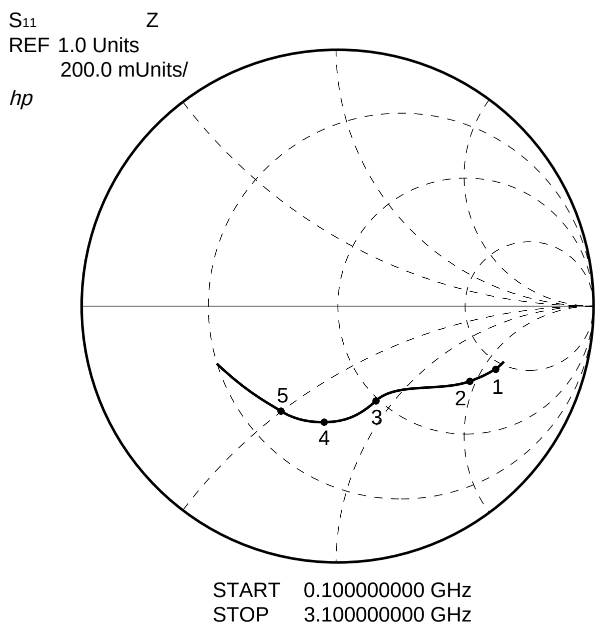
Figure 5-3. S Parameter Values (MAG, ANG) and Input/Output Smith Chart without Matching

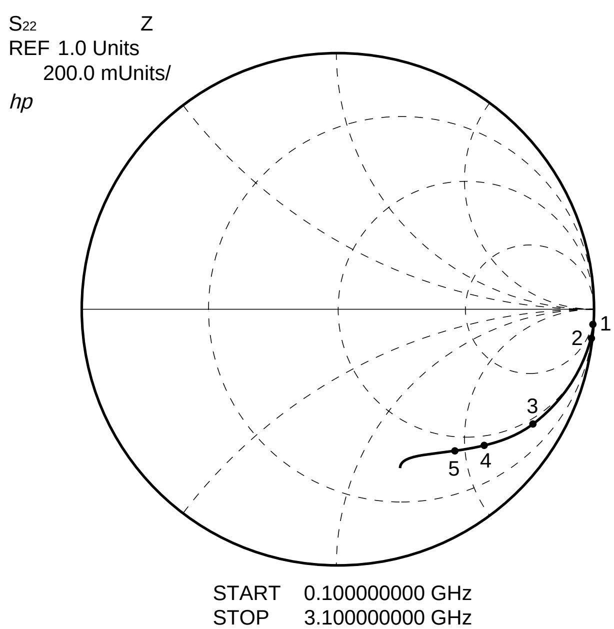
(a) μPC8119T

μPC8119T

Conditions: $V_{CC} = V_{out} = 3.0$ V, V_{AGC} = GND, T_A = +25°C

		S11		S22	
		MAG	ANG	MAG	ANG
1:	130 MHz	0.659	–22.1	0.996	–4.4
2:	240 MHz	0.560	–33.6	0.992	–8.2
3:	950 MHz	0.413	–67.7	0.890	–30.4
4:	1440 MHz	0.428	–94.2	0.788	–42.1
5:	1900 MHz	0.440	–116.0	0.728	–49.3





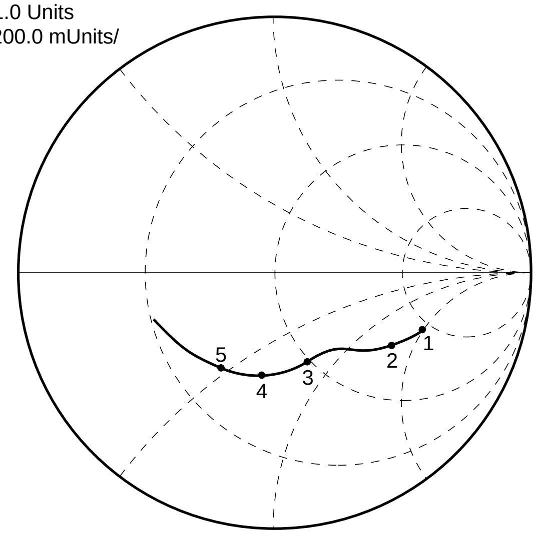
(b) μPC8120T

μPC8120T

Conditions: $V_{CC} = V_{out} = 3.0$ V, $V_{AGC} = V_{CC}$, $T_A = +25°C$

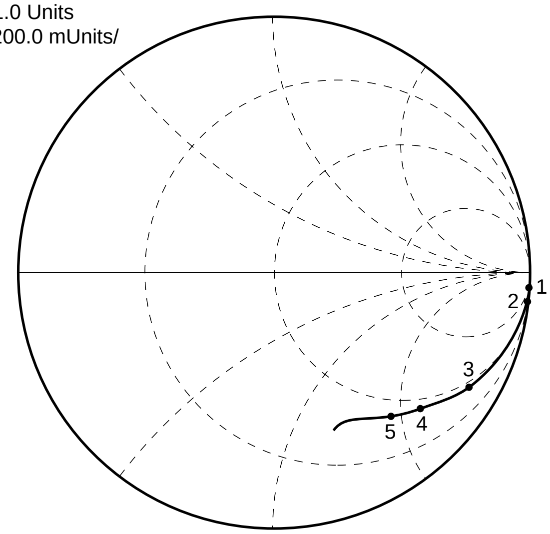
		S11		S22	
		MAG	ANG	MAG	ANG
1:	130 MHz	0.594	–22.8	0.987	–4.5
2:	240 MHz	0.500	–34.2	0.980	–8.3
3:	950 MHz	0.365	–68.5	0.882	–30.9
4:	1440 MHz	0.403	–96.0	0.784	–42.5
5:	1900 MHz	0.412	–117.9	0.726	–50.8

S_{11} Z
REF 1.0 Units
200.0 mUnits/
hp



START 0.100000000 GHz
STOP 3.100000000 GHz

S_{22} Z
REF 1.0 Units
200.0 mUnits/
hp



START 0.100000000 GHz
STOP 3.100000000 GHz

5.5 Supplement on Application

Because these ICs do not have a power save pin in limitation of the total number of pins, they must be turned ON/OFF by the V_{CC} voltage for intermittent operation. Turning ON/OFF the V_{CC} voltage poses no problem to the internal transistor of durability, as long as the voltage applied to the V_{AGC} pin does not exceed 3 V.

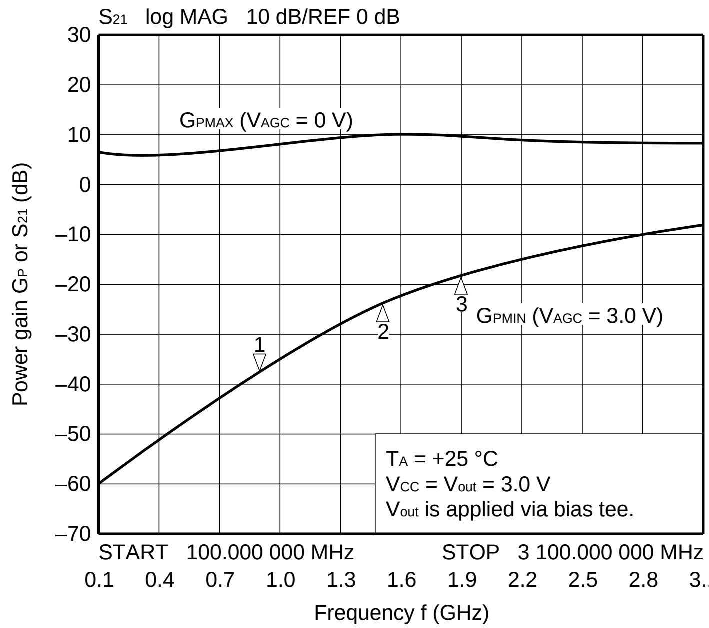
Although the recommended operating range of the input level is specified to be P_{in}: –18 dBm or less, this is under the condition that the adjacent channel interference power (APC) is –60 dBc or less at $\Delta f = \pm 50$ kHz in the case of the modulation signal of PDC. In the case of the modulation signal of PHS, it is P_{in}: –10 dBm or less where the APC is –60 dBc or less at $\Delta f = \pm 600$ kHz. Under conditions other than above, confirm the characteristics of the set to determine the input level.

6. OTHER APPLICATION EXAMPLES

Although the application of the ICs at the narrow band has been explained so far, these ICs can be also used at a wide band with a high-impedance load. In this case, the output pin is operated with an inductor load, instead of frequency matching. Although the values of external components L1 and C2 of the output pin are small in Figure 5-2 according to the frequency for impedance matching in a narrow band, increase the values of these components in a wide band by employing a high pass type external configuration that does not have a frequency dependency. For example, L1 = 300 nH and C2 = 1000 pF (where the lower-limit frequency is 100 MHz) can be used. To cover a lower-frequency range, increase the values of L1 and C2 much more. Figure 6-1 shows the frequency vs. power gain characteristics in a wide band. The output port impedance at this time is close to S_{22} of these ICs themselves.

Figure 6-1. Power Gain vs. Frequency Characteristics at Wide Band Operation

(a) μPC8119T



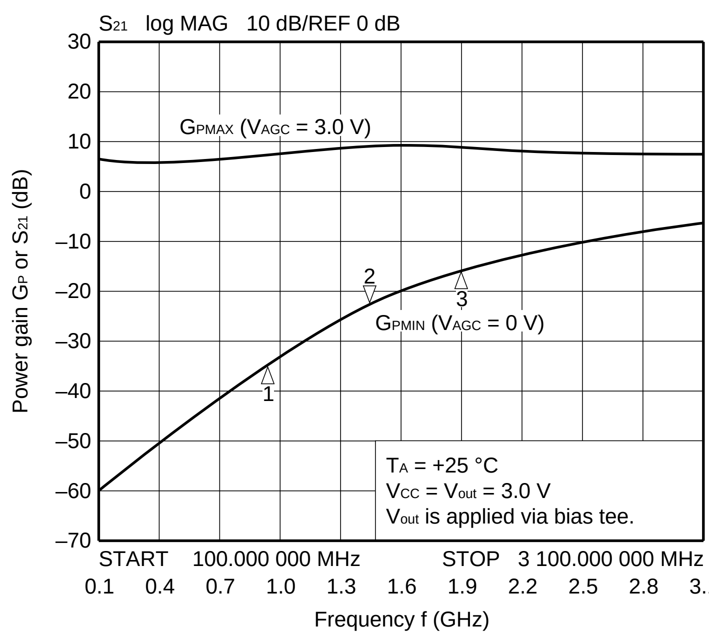
G_{PMIN} value

1: 900 MHz : –38.0 dB

2: 1500 MHz : –23.9 dB

3: 1900 MHz : –18.4 dB

(b) μPC8120T



G_{PMIN} Value

1: 950 MHz : –34.0 dB

2: 1440 MHz : –21.6 dB

3: 1900 MHz : –15.6 dB

7. CONCLUSION

These ICs are expected to be used in a variety of applications when the user determine the external circuit constants and optimize the characteristics depending on the operating conditions and in relation with the internal circuit.

Reference μPC8119T, μPC8120T Data Sheet (Document No.: P11027E)

Remark The external control circuit should be referred to the documents of your external control circuit devices.

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