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Renesas Electronics Corporation

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H8/300H Tiny Series

Unsigned 32-Bit Binary Division (DIV)

Introduction

Carries out division in this format:

dividend (unsigned, 32 bits)/divisor (unsigned, 32 bits) = quotient (unsigned, 32 bits) ... remainder (unsigned, 32 bits).

Division by 0 sets the Z flag.

Target Device

H8/300H Tiny Series

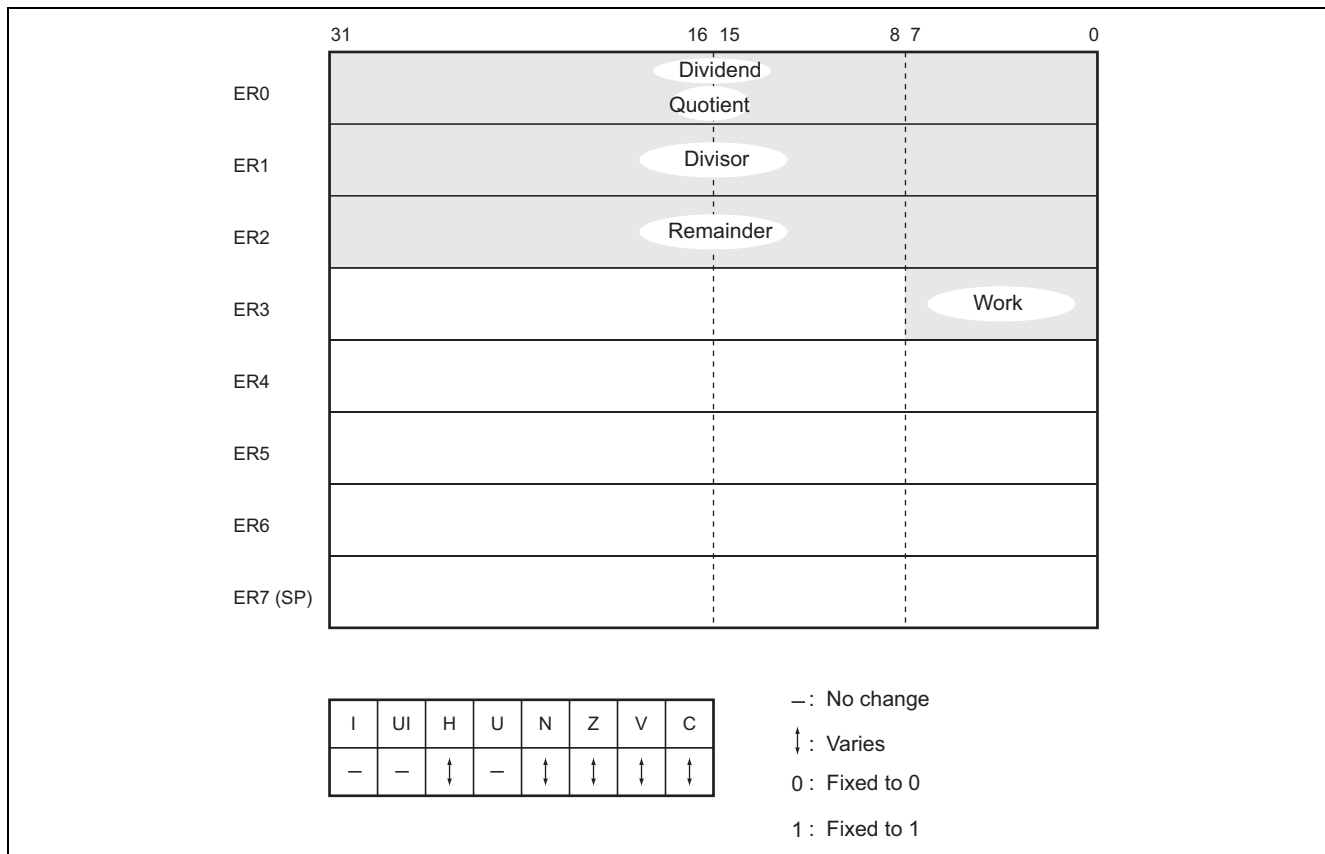
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1. Arguments

Description		Storage Location	Data Length (Bytes)
Input	Dividend (unsigned, 32 bits)	ER0	4
	Divisor (unsigned, 32 bits)	ER1	4
Output	Quotient (unsigned, 32 bits)	ER0	4
	Remainder (unsigned, 32 bits)	ER2	4
	Occurrence of error (division by 0) (Yes: Z = 1; No: Z = 0)	Z flag (CCR)	—

2. Changes to Internal Registers and Flags



3. Programming Specifications

Program memory (bytes)	30
Data memory (bytes)	0
Stack (bytes)	0
Number of cycles	762
Re-entrant	Yes
Relocatable	Yes
Interrupts during execution	Yes

4. Note

The number of cycles in the programming specifications is the value for calculation of $H'FFFFFFF/H'01$.

5. Description

5.1 Description of Functions

1. The arguments are as follows:

ER0: Set the dividend (unsigned, 32 bits) as an input argument. The quotient (unsigned, 32 bits) is also set here, as an output argument.

ER1: Set the divisor (unsigned, 32 bits) as an input argument.

ER2: The remainder (unsigned, 32 bits) is set here as an output argument.

Z flag (CCR): Indicates error status (division by 0) after execution of DIV.

Z flag = 1: The division was in error.

Z flag = 0: The division was completed without error.

2. The following figure illustrates the execution of the software DIV. When the input arguments are set as shown below, execution places the quotient in ER0 and the remainder in ER1.

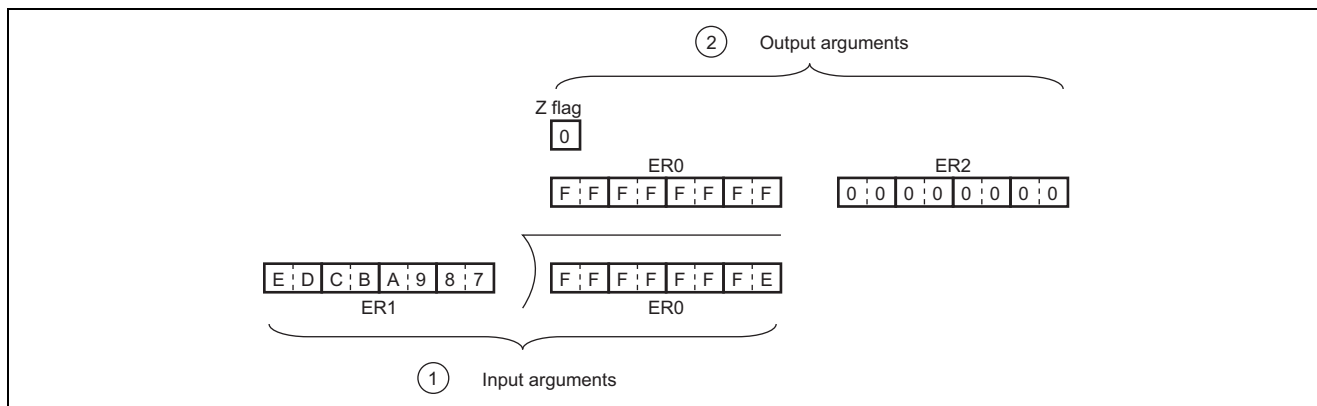


Figure 1 Example of DIV Execution

3. The DIV subroutine starts by determining whether the divisor is 0 or nonzero; if it is 0, DIV ends.

5.2 Usage Notes

Since the quotient is set in ER0, the dividend will be lost through execution of DIV. If you will still require the dividend, save it elsewhere in memory beforehand.

5.3 Description of Data Memory

No data memory is used by DIV.

5.4 Example of Usage

After setting the dividend and divisor, call the DIV subroutine.

```

WORK1 . RES. L 1      ..... Reservation of the data memory area for setting of the dividend (unsigned, 32 bits) by the user program.
WORK2 . RES. L 1      ..... Reservation of the data memory area for setting of the divisor (unsigned, 32 bits) by the user program.
      .
      .
MOV. L @WORK1, ER0    ..... Sets, as an input argument, the dividend (unsigned, 32 bits) specified by the user program.
MOV. L @WORK2, ER1    ..... Sets, as an input argument, the divisor (unsigned, 32 bits) specified by the user program.
JSR @DIV              ..... Subroutine call of DIV.
    
```

5.5 Principles of Operation

1. In binary division, the quotient and remainder are found through repeated subtraction. In the following figure, the division of H'0D by H'03 is given as an example of this operation.

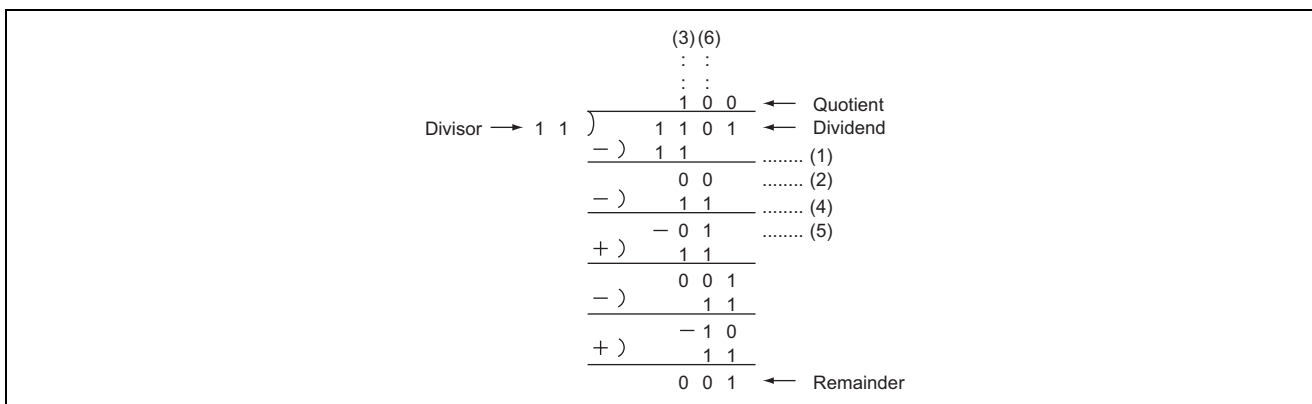
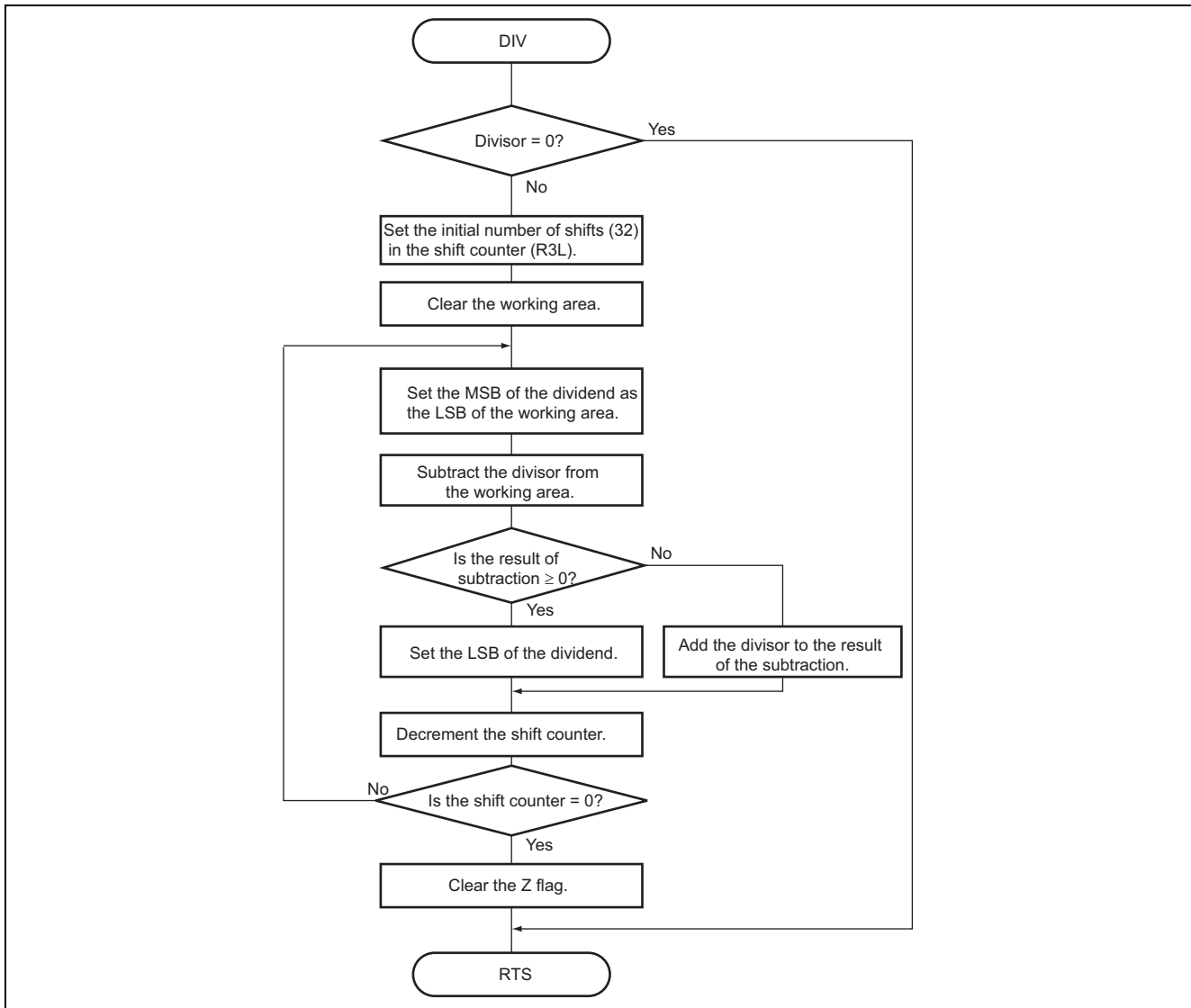


Figure 2 Division

2. Detailed description of the program:

- 1) The initial number of shifts is set in the counter R3L, which indicates the number of shifts.
- 2) The dividend is shifted 1 bit to the left and the MSB thus loaded to the C bit is set as the LSB of ER2, which will hold the remainder.
- 3) The divisor is subtracted from ER2. When the result of subtraction is positive, the LSB of ER0 is set ((1) → (2) → (3) in the figure). When the result of subtraction is negative, the LSB of ER0 is cleared and the divisor is added to the result of subtraction, returning it to the state prior to subtraction ((4) → (5) → (6) in the figure).
- 4) The shift counter set in step 1) above is decremented.
- 5) Steps 2) to 4) are repeated until the shift counter reaches -1.

6. Flowchart



7. Program Listing

```

1          1
2          2 ;*****
3          3 ;*
4          4 ;*      NAME      :   32 BIT DIVISION(DIV)
5          5 ;*
6          6 ;*****
7          7 ;*
8          8 ;*      ENTRY   :   ER0          (DIVIDEND)
9          9 ;*
10         10 ;*      RETURNS :   ER0          (QUOTIENT)
11        11 ;*
12        12 ;*
13        13 ;*****
14        14 ;
15        15          .CPU      300HA
16        16          .SECTION A, CODE, LOCATE=H'001000
17        17 DIV      .EQU      $          ;Entry point
18        18          MOV.L    ER1,ER1    ;
19        19          BEQ      DIV4      ;
20        20          MOV.B    #32,R3L    ;Set shift counter
21        21          SUB.L    ER2,ER2    ;Clear remainder
22        22 DIV1     SHLL.L    ER0      ;Shift dividend 1 bit left
23        23          ROTXL.L ER2      ;Set MSB of dividend to LSB of remainder
24        24          SUB.L    ER1,ER2    ;Sub divisor from remainder
25        25          BCC      DIV2      ;Branch if remainder >= divisor
26        26          ADD.L    ER1,ER2    ;Add divisor to remainder
27        27          BRA      DIV3      ;Branch always
28        28 DIV2     BSET     #0,R0L    ;Set 1 to dividend LSB
29        29 DIV3     DEC.B    R3L      ;Decrement shift counter
30        30          BNE      DIV1      ;Branch until shift counter = 0
31        31          ANDC    #B'11111011,CCR
32        32 DIV4     RTS
33        33          .END
***** TOTAL   ERRORS   0
***** TOTAL   WARNINGS  0

```

Note: The program listing included in this application note assumes compilation under the option for the advanced mode of H8/300H CPU. If you use this sample program with an H8/300H Tiny Series product, make the following change to the program code:

.CPU 300HA → .CPU 300HN

Revision Record

Rev.	Date	Description	
		Page	Summary
2.00	Feb.28.06	—	Format has been changed from Hitachi version to Renesas version.

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