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April 1st, 2010
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M32C/83, M32C/85 Groups

UART Bit-Rate Auto Setting

1. Abstract

This application note describes a procedure to set the UART bit rate automatically, utilizing serial interface.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M32C/83 Group and M32C/85 Group

The program on this application note can also be used when operating other microcomputers within the M16C Family, provided they have the same SFRs (Special Function Registers) as the M32C/83 and M32C/85 Groups. However, some functions may have been modified. Refer to each device's hardware manual for details. Use functions covered in this application note only after careful evaluation.

3. Detailed Description

Auto bit-rate setting

A) Figure 1 shows an example of circuit connection for UART auto bit-rate setting.

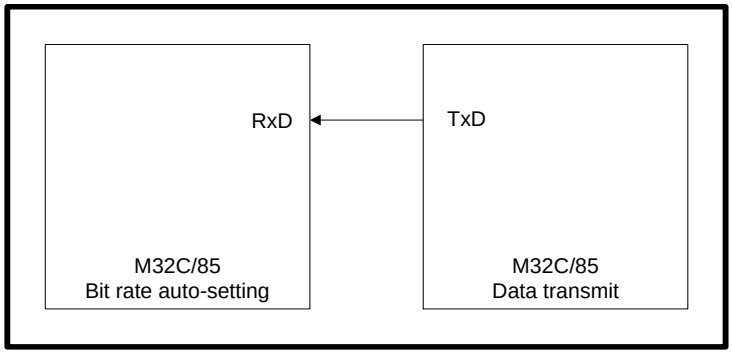

Figure 1. Circuit Connection for UART auto bit-rate setting

B) Measure the UART communication bit rate by the following transfer format.

- 8-bit transfer data
- no parity bit
- 2 stop bits
- CTS/RTS function disabled
- TxD and RxD I/O polarity inverse disabled
- LSB first

C) Set the UiBRG (i= 0 to 4) register to 80h as a default bit rate for the bit rate auto setting to wait for data to be received. Fix the count source of BRG at f8.

D) Sixteen negotiation data 00h are transmitted from the TxDi pin after setting the given bit rate. Figure 2 shows an example of the negotiation data transmit operation.

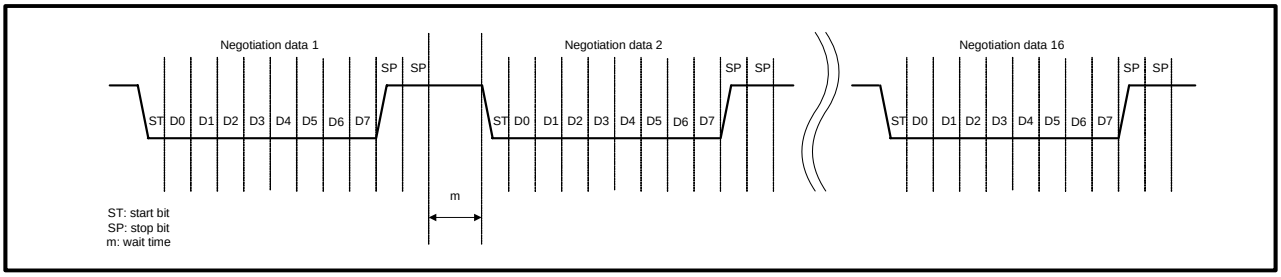

Figure 2. Negotiation Data Transmit Operation

E) When negotiation data 1 to 8 are transmitted to the RxDi pin, the FER flag in the UiRB is read for framing error and the UiBRG register is determined to either 0 or 1 from the high-order bit.

0: no framing error

1: framing error occurs

F) When negotiation data 9 to 16 are transmitted to the RxDi pin, the data is read for 00h and the UiBRG register is determined to either 1 or 0 from the high-order bit.

0: received data is other than 00h

1: received data is 00h

Determine the mean value of the above results as the UiBRG register value.

Figure 3 and 4 show the UiBRG register setting.

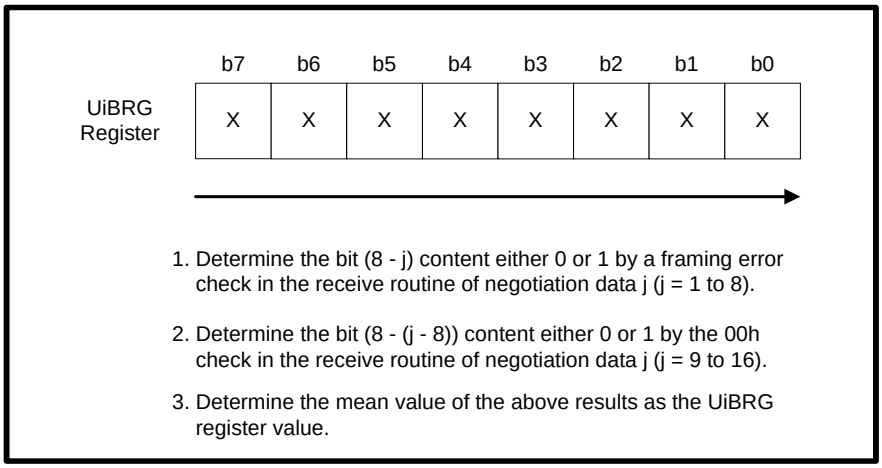

Figure 3. UiBRG Register Setting

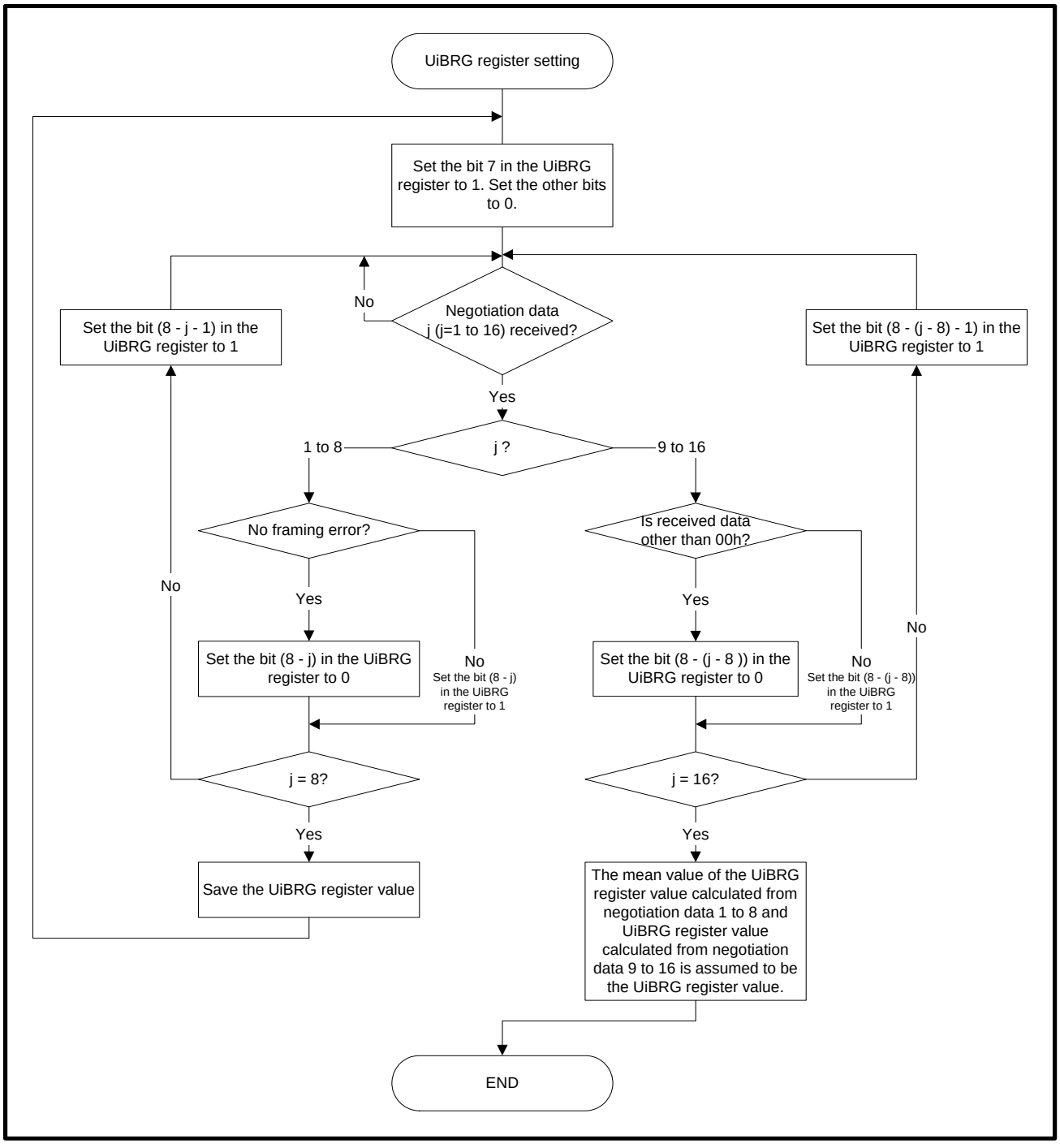

Figure 4. UiBRG Register Setting

Figure 5 shows an example for normal reception timing of negotiation data.

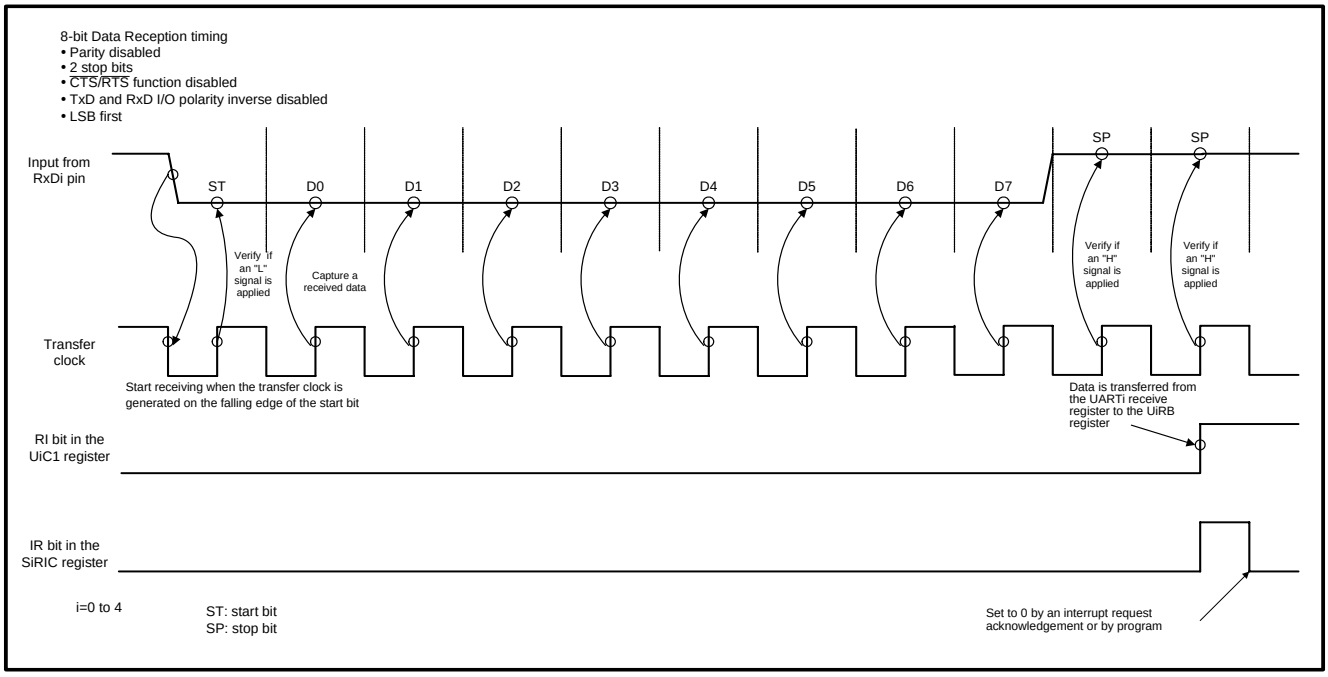

Figure 5. Normal Reception Timing of Negotiation Data

Figure 6 shows an example for framing error timing in the negotiation data receive routine. (RxD bit rate > TxD bit rate)

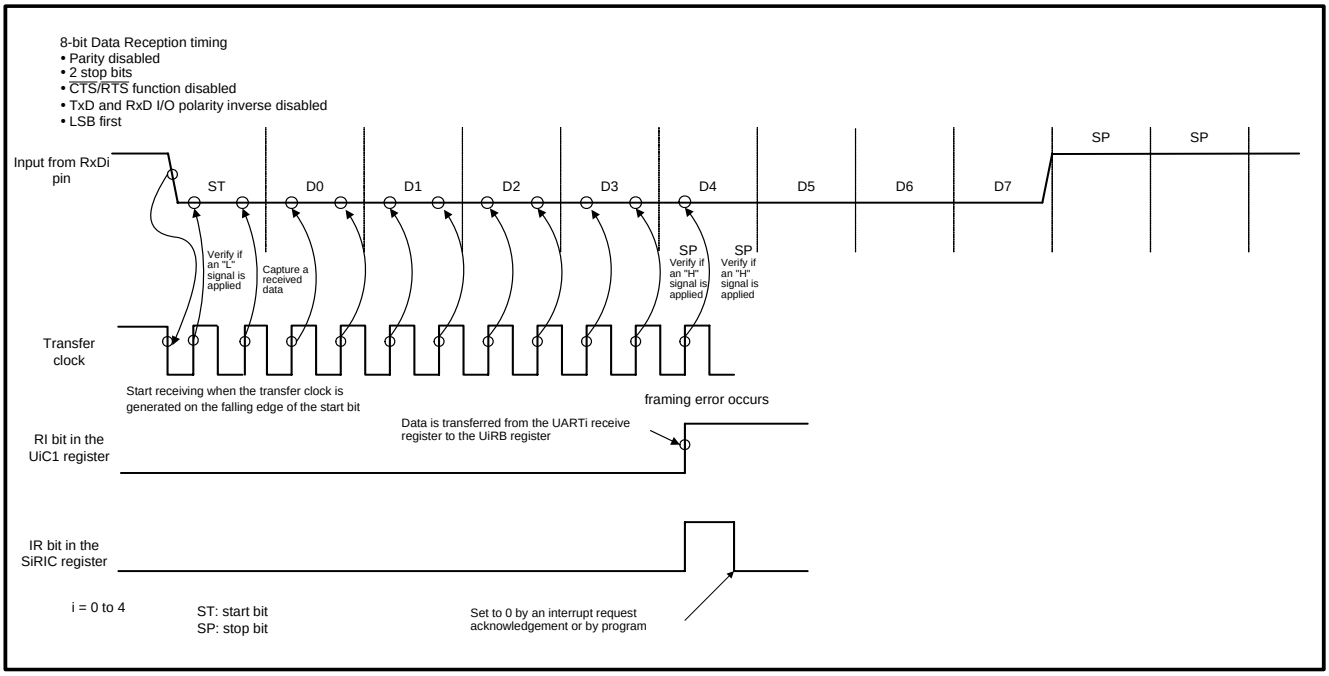

Figure 6. Framing Error Timing

Figure 7 shows an example of unsuccessful reception timing of negotiation data.
(RxD bit rate < TxD bit rate)

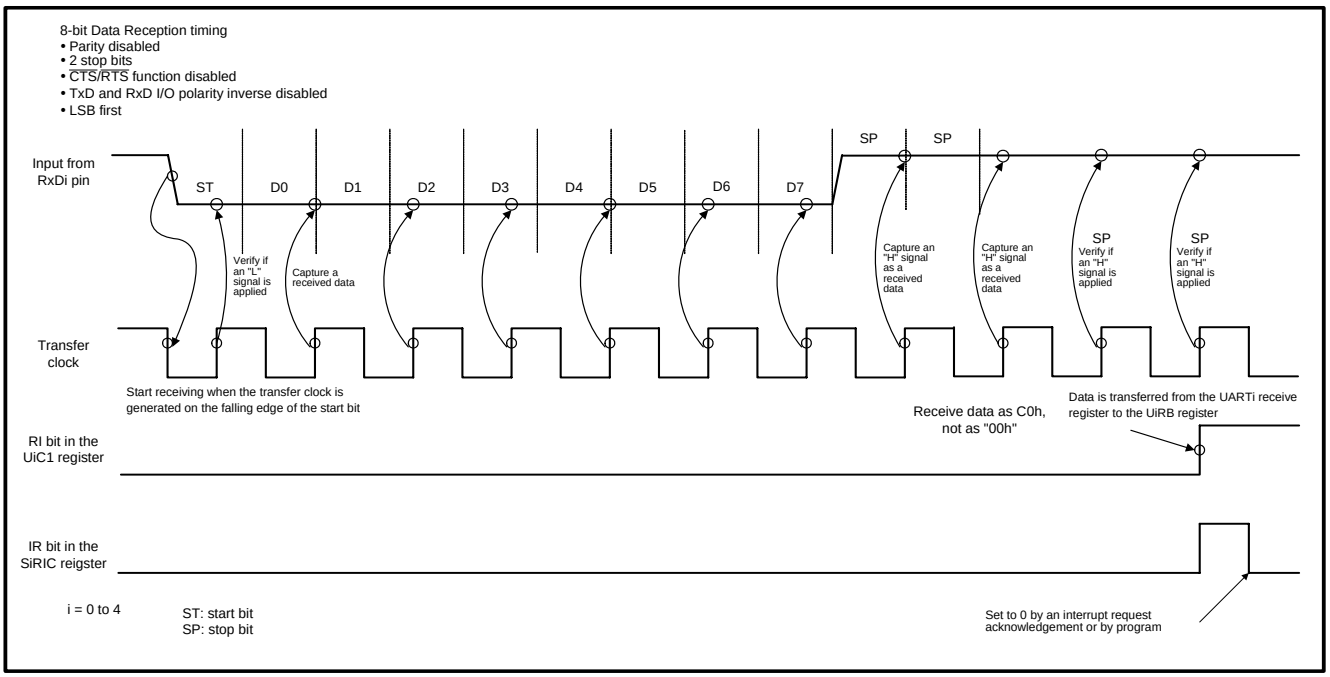

Figure 7. Unsuccessful Reception of Negotiation Data

3.1 Bit Rate Detection Range

When the clock source of RxD serial interface is x and the bit rate is y, the bit rate detection range is calculated from the following equation.

- Minimum bit rate(y) = $\dfrac{x}{(255 + 1) \times 16}$

  Maximum value of the UiBR register: 255

- Maximum bit rate(y) = $\dfrac{x}{(0 + 1) \times 16}$

  Minimum value of the UiBRG register: 0

For example, if the system clock frequency for RxD is 30 MHz, internal clock is selected, and theCLK1 and CLK0 bits in the UiC0 (i = 0 to 4) register are set to 01 (selects f8), the range will be:

- Minimum bit rate(y) = $\dfrac{\dfrac{30\ \text{MHz}}{8}}{4096}$ = approx. 915 bps

- Maximum bit rate(y) = $\dfrac{\dfrac{30\ \text{MHz}}{8}}{16}$ = 234375 bps

However, as to the maximum bit rate of this sample program must be less than the value calculated from the equation in the **3.2 Start Bit Detection Range**.

3.2 Start Bit Detection Range

In the sample program, the initial value of the UiBRG register is set to 80h. If the clock source of RxD serial I/O is x, initial bit rate is y, its cycle is z, start bit verify time is h, negotiation data minimum "L" cycle is i, TxD bit rate is j, the maximum TxD bit rate which can detect the start bit is calculated from the following equations.

- Initial bit rate(y) = $\frac{x}{(128 + 1) \times 16}$

  Initial value of the UiBRG register: 128

- Cycle(z) = $\frac{1 \text{ sec}}{y}$

- Start bit verify time(h) = z / 2

  Data starts being received when the transfer clock is generated on the falling edge of the start bit and the start bit "L" on the next rising edge is verified, therefore, divide by 2.

- Negotiation data minimum "L" cycle(i): h / 9

  Sum of start bit and 8 bit data: 9

- TxD bit rate(j) = 1 sec / i

For example, if a system clock frequency for RxD is 30 MHz, internal clock is selected, and the CLK1 and CLK0 bits in the UiC0 (i = 0 to 4) register are set to 01b (selects f8), the range will be:

- Initial bit rate(y) = $\frac{\frac{30 \text{ MHz}}{8}}{2064}$ = approx. 1816 bps

- Cycle(z) = 1 sec/1816 = approx. 550 μs
- Start bit verify time (h) = 550 μs / 2 = 275 μs
- Negotiation data minimum "L" cycle(i) = 275 μs / 9 = approx. 31 μs
- Maximum TxD bit rate (j) = 1 sec / 31 μs = approx. 32258 bps

Maximum TxD bit rate will be approx. 32258 bps.

Figure 8 shows an example of the start bit undetected timing for negotiation data.
(RxD bit rate < TxD bit rate)

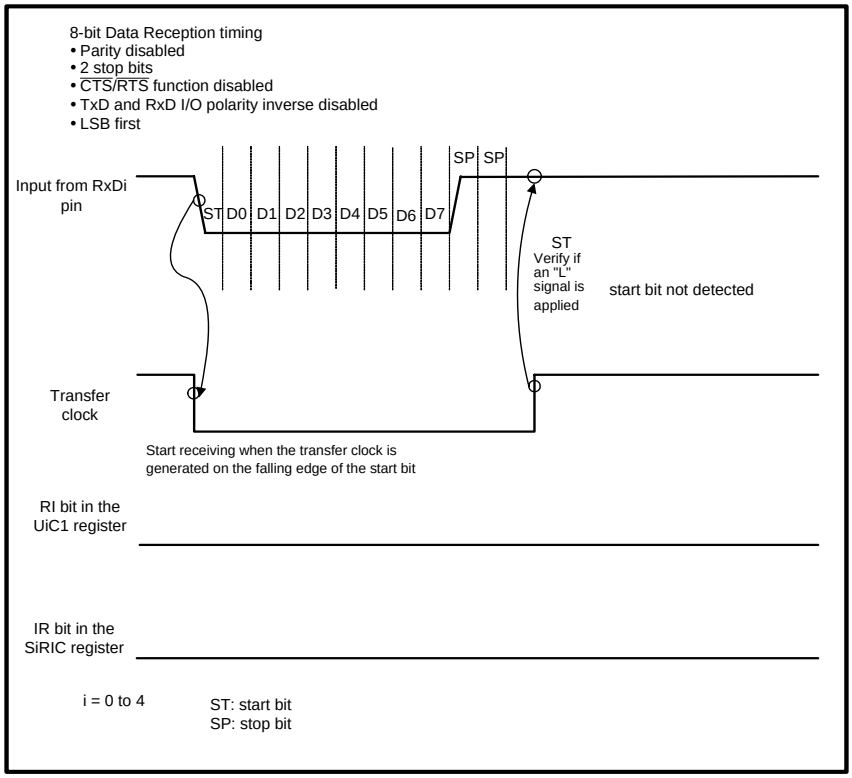

Figure 8. Negotiation Data Start Bit Undetected Timing

3.3 Minimum Wait Time Among Negotiation Data To Detect Start Bit

If a clock source of RxD serial I/O is x, minimum bit rate is y, its cycle is z, minimum wait time among negotiation data is m, and software processing time to set the UiBRG register again is α, the minimum wait time among negotiation data to detect start bit is calculated from the following equations.

- Minimum bit rate(y) = $\dfrac{x}{(255 + 1) \times 16}$

  Maximum value of the UiBRG register: 255

- Cycle(z) = $\dfrac{1 \text{ sec}}{y}$

- Minimum wait time between negotiation data (m) = z × 11 + α

  Sum of start bit, 8 bit data, and 2 stop bits: 11

For example, if a system clock frequency for RxD is 30 MHz, internal clock is selected, and bits CLK1 and CLK0 in the UiC0 (i = 0 to 4) register are set to 01(selects f8), the range will be:
(The software processing time to reset the UiBRG register is approximately 4μs at CPU clock frequency of 30 MHz.)

- Minimum bit rate(y) = $\dfrac{\dfrac{30 \text{ MHz}}{8}}{4096}$ = approx. 915 bps
- Cycle(z) = 1 sec / 915 = approx. 1.1 ms
- Minimum wait time between negotiation data (m) = 1.1 ms × 11 + 4 μs
  = approx. 13 ms

Wait time of no less than approximately 13 ms is required between negotiation data.

4. Sample Program

Figure 9 and 10 show flow charts of sample program.

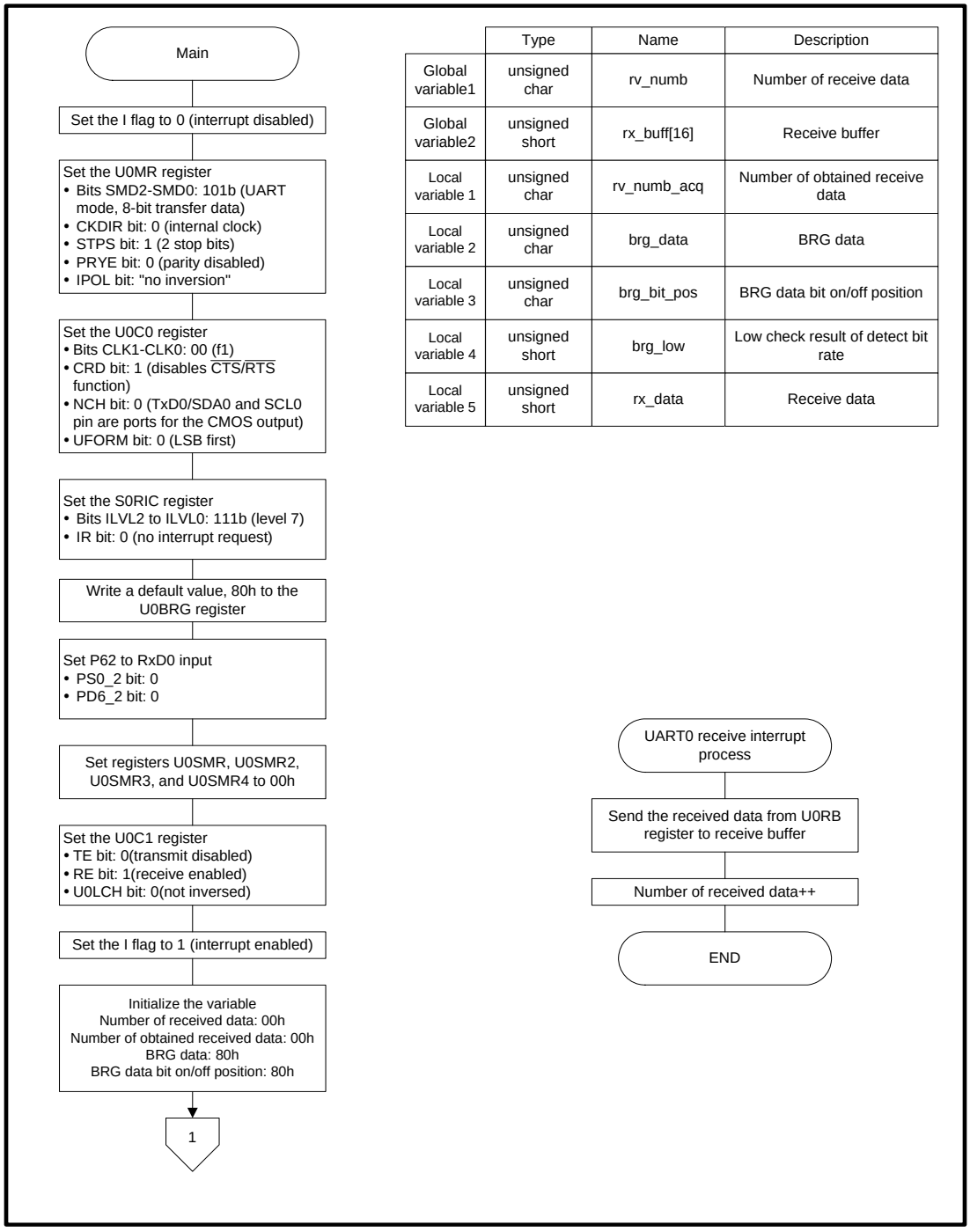

Figure 9. Sample Program Setting for UART Bit Rate(1)

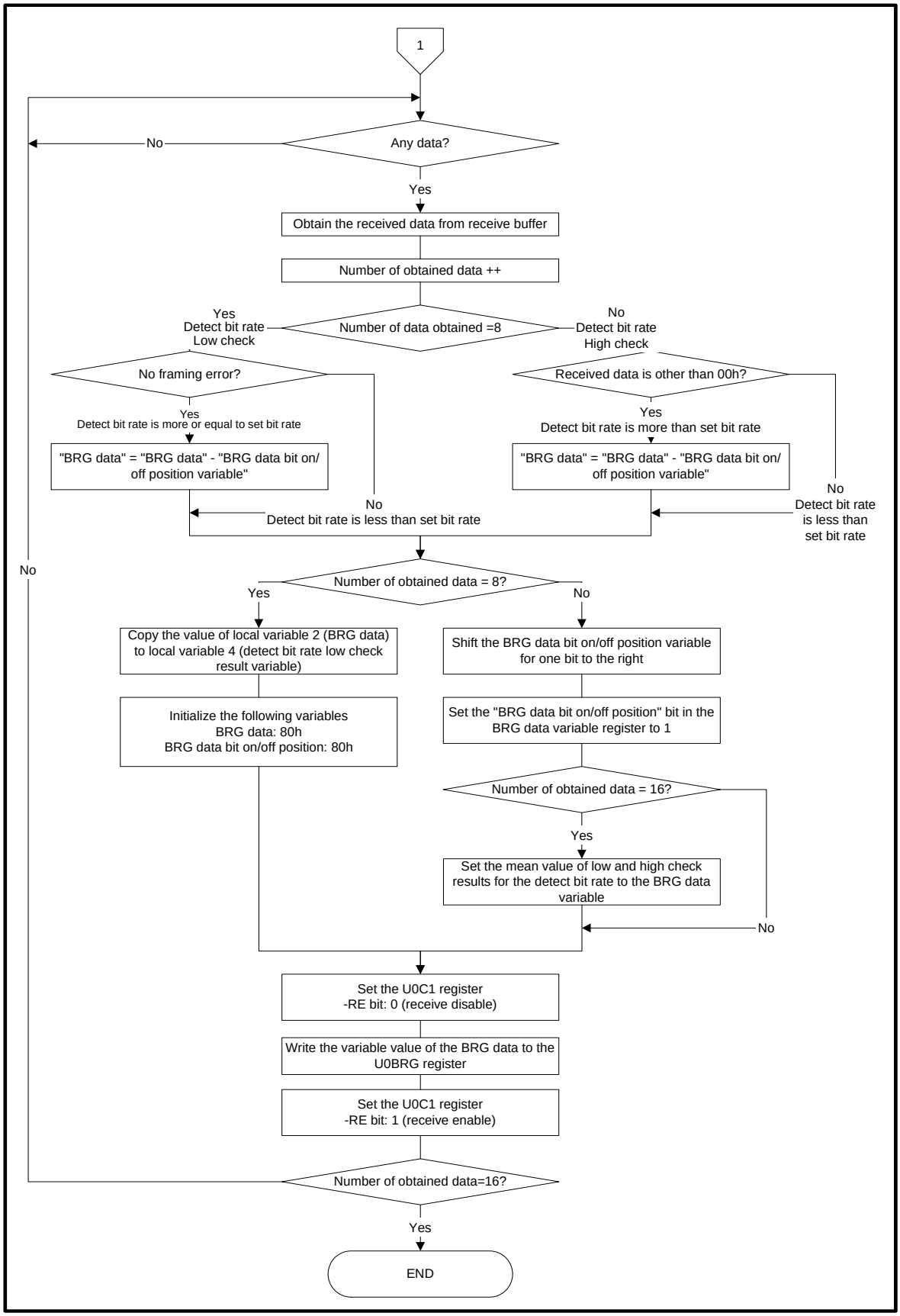

Figure 10. Sample Program Setting for UART Bit Rate (2)

5. Reference Program

Please find the reference program from the Renesas Technology Web site.
Click Application Note in the left menu of the M32C/80 Series top page.

6. Reference Documents

Hardware manual
M32C/83Group Hardware Manual
M32C/85Group Hardware Manual
(Use the most recent version of the document on the Renesas Technology Web site.)

Technical news/Technical update
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REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
1.00	2006.03.15	-	First edition issued

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