IDT® Tsi568A and Tsi578

Device Differences

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1. Tsi568A and Tsi578 Device Differences

This document describes the differences between the Tsi568A and Tsi578 devices. It was created to help system designers understand differences between the two devices and provide an easy migration path for board designers.

The following differences topics are discussed:

1.1 Functional Differences

The functional differences between the Tsi568A and Tsi578 are summarized in Table 1.

Table 1: Functional Differences between Tsi568A and Tsi578

Function/Feature	Used in Device	
	Tsi568A	Tsi578
Packet Time To Live feature		✓
Forwarding of Multicast Control Symbols		✓
Packet Multicast • Implementation of the Multicast Engines		✓
Lane Swap • Changing the endianness of the Rx and Tx SerDes lanes		✓
Enhanced I^2C • I^2C slave capability • Support multiple I^2C masters • Load more than 256 registers from EEPROM		✓
Performance Statistics		✓

Table 1: Functional Differences between Tsi568A and Tsi578

Function/Feature	Used in Device	
	Tsi568A	Tsi578
Error Management Extensions		✓
Hierarchical Look-up Table		✓
IEEE 1149.6 Compliant		✓

1.2 Register Differences

The register differences between the Tsi568A and Tsi578 are extensive. IDT recommends reviewing the Tsi578 documentation and reference the new features listed in Section 1.1 on page 3.

1.3 Physical Differences

The Tsi568A and Tsi578 devices are forward compatible, however the Tsi578 is not a drop-in replacement for the Tsi568A. Forward compatibility means that a board can be designed to accommodate both devices with a change in the bill of materials.

IDT recommends the hardware manuals and device errata for both devices be consulted when designing. The the hardware manuals and device errata are available at www.IDT.com.

1.3.1 Pin List Changes

Table 2 highlights the differences between digital signals for the Tsi568A and the Tsi578.

Table 2: Digital Signal Changes[a]

Digital Signals		
Changed Ball Numbers	**Tsi568A Pin Name**	**Tsi578 Pin Name**
B24	S_CLK_1_p Maximum clock speed 312.5 MHz	S_CLK_p Maximum clock speed 156.25 MHz
B25	S_CLK_1_n Maximum clock speed 312.5 MHz	S_CLK_n Maximum clock speed 156.25 MHz
D24	S_CLK_2_p Provide SCLK_1_P through a 0 ohm resister	VSS[b]

Table 2: Digital Signal Changes[a]

Digital Signals		
Changed Ball Numbers	**Tsi568A Pin Name**	**Tsi578 Pin Name**
D25	S_CLK_2_n Provide SCLK_1_N through an 0 ohm resister	VSS[b]
Y18	VSS	VSS_IO
V19	VSS	BCE Boundary Scan compatibility enable pin. This input is used to aid 1149.6 testing.The pin can either be pulled up or pulled down, depending on the functionality required.
AD24	VSS_IO	MCES Support for Multicast Event Control Symbol
W20	VSS	I2C_SEL Support for I^2C functionality
T19	VSS	I2C_SA[0] Support I^2C slave functionality
U19	VSS	I2C_SA[1] Support I^2C slave functionality
AE3	N/C	VSS[b]
AE22	SP0_PWRDN SP0_PWRDN pin not required because port 0 must always remain powered up	I2C_MA Support I^2C slave functionality
C24	SP_VDD	REF_AVDD
C26	SP_VDD	REF_AVDD
Y19	N/C	SP_RX_SWAP
Y20	N/C	SP_TX_SWAP

a. Refer to the Tsi568A *User Manual* and the Tsi578 documentation for a full description of all the pins listed in the table.

b. For backwards capability between Tsi568A and Tsi578, this pin can be left as a No Connect. This enables the design of boards that support both devices.

Table 2 highlights the differences between analog signals for the Tsi568A and the Tsi578.

Table 3: Analog Signal Changes[a]

Analog Signals		
Changed Ball Numbers	**Tsi568A Pin Name**	**Tsi578 Pin Name**
F4	SP0_RREF (Referenced to AVDD)	SP0_REXT (Referenced to VSS)
F5	SP0_AVDD (AVDD = 1.2 V)	SP0_AVDD (AVDD = 3.3 V)
H5	SP0_VTT (1.04 V to 1.8 V)	SP0_AVDD (AVDD = 3.3 V)
P4	SP8_RREF (Referenced to AVDD)	SP8_REXT (Referenced to VSS)
T5	SP8_VTT (1.04 V to 1.8 V)	SP8_AVDD (AVDD = 3.3 V)
AB9	AVDD = 1.2 V	AVDD = 3.3 V
AB11	SP2_VTT (1.04 V to 1.8 V)	SP2_AVDD (AVDD = 3.3 V)
AC17	SP10_RREF (Referenced to AVDD)	SP10_REXT (Referenced to VSS)
AB17	AVDD = 1.2 V	AVDD = 3.3 V
AB19	SP10_VTT (1.04 V to 1.8 V)	SP10_AVDD (AVDD = 3.3 V)
V23	SP4_RREF (Referenced to AVDD)	SP4_REXT (Referenced to VSS)
V22	SP4_AVDD (AVDD = 1.2 V)	SP4_AVDD (AVDD = 3.3 V)
T22	SP4_VTT (1.04 V to 1.8 V)	SP4_AVDD (AVDD = 3.3 V)
K23	SP12_RREF (Referenced to AVDD)	SP12_REXT (Referenced to VSS)
K22	SP12_AVDD (AVDD = 1.2 V)	SP12_AVDD (AVDD = 3.3 V)
H22	SP12_VTT (1.04 V to 1.8 V)	SP12_AVDD (AVDD = 3.3 V)

Table 3: Analog Signal Changes[a]

Analog Signals		
Changed Ball Numbers	**Tsi568A Pin Name**	**Tsi578 Pin Name**
D18	SP6_RREF (Referenced to AVDD)	SP6_REXT (Referenced to VSS)
E16	SP6_VTT (1.2 V)	SP6_AVDD (AVDD = 3.3 V)
E18	SP6_AVDD (AVDD = 1.2 V)	SP6_AVDD (AVDD = 3.3V)
D10	SP14_RREF (Referenced to AVDD)	SP14_REXT (Referenced to VSS)
E8	SP14_VTT (1.2 V)	SP14_AVDD (AVDD = 3.3 V)
E10	SP14_AVDD (AVDD = 1.2 V)	SP14_AVDD (AVDD = 3.3 V)

a. Refer to the Tsi568A *User Manual* and the Tsi578 documentation for a full description of all the pins listed in the this table.

1.3.1.1 Schematic Lay-out of Pin Changes

The following figures are a set of reference diagrams taken from the Tsi578 evaluation board (which also supports the Tsi568A device). These diagrams also apply to the Tsi574, however the pin numbers are different.

The pop_Tsi568 notation means the given component is populated for the Tsi568A, while the pop_reserved notation means the given component is populated for the Tsi578 device.

Figure 1: BCE Resistor Option

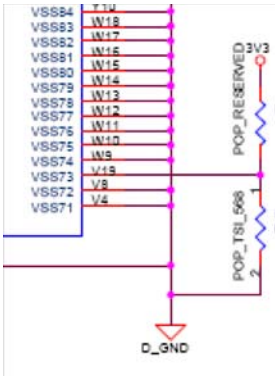


Figure 2: I²C Resistor Population Option

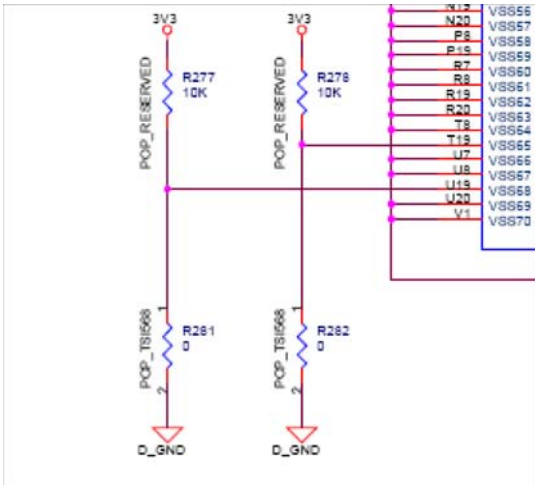


Figure 3: MCES Resistor Population Option

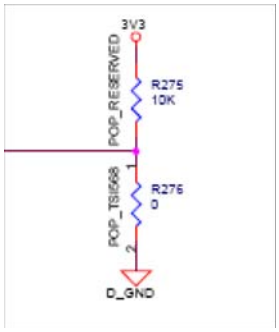


Figure 4: I2C_SEL Resistor Population Option

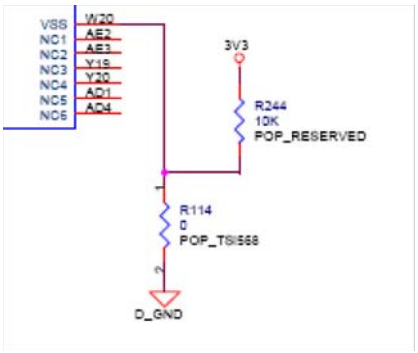
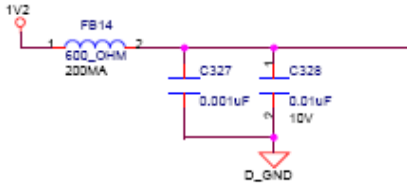
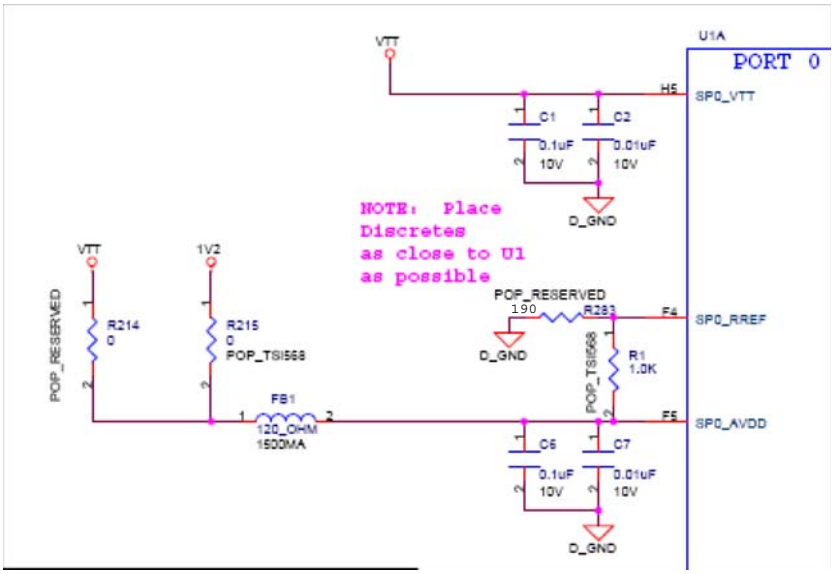


Figure 5: REF_AVDD Filter



The same circuitry can be used for the Tsi568A and Tsi578 devices.

Figure 6: Analog Resistor



In this design Vtt can be controlled to be between 1.2V and 3.3V. For the Tsi578 operation Vtt is set to be 3.3V which provides the required voltage for SPx_AVDD.

1.3.1.2 Board Layout Impact

A PCB designed to accommodate both Tsi568A and Tsi578 should be laid out in a manner that the noise level on the SPx_VTT and SPx_AVDD signals are within the limit required for both devices. Please refer to the Hardware Manuals for maximum ripple on supply rails.

SPx_VTT Signal

Based on the schematic of Figure 6, the VTT net can be implemented as a local plane located under the BGA. The supply to the VTT plane should be filtered (the filter is not shown in Figure 6). Ideally, the 0.1uF and 0.01uF capacitors (C1 and C2) for the SPx_VTT pins are located under the BGA within the breakout vias. If this is not possible, the capacitors should be very close to the edge of the package.

SPx_AVDD Signal

The net from the ferrite bead (FB1) of Figure 6 to the SPx_AVDD pin can be implemented as a trace from the ferrite bead to the SPx_AVDD pin breakout via, as long as the decoupling capacitors are located under the BGA and connected to the breakout via with short traces.

Another option for the Tsi568A SPx_AVDD pins is to regroup all the individual supply nets into a single net implemented as a power plane located under the BGA. The supply to that plane should be filtered. Ideally, the 0.1uF and 0.01uF capacitors (C6 and C7) are located under the BGA within the breakout vias. If this is not possible, the capacitors should be very close to the edge of the package.

1.4 Electrical Differences

The Tsi568A and the Tsi578 meet the electrical requirements of the *RapidIO Interconnect Specification (Revision 1.2)*. However, the Tsi578 also meets the *RapidIO Interconnect Specification (Revision 1.3)*.

1.5 Other Differences

1.5.1 Device ID

Device identifiers are unique for the Tsi568A and Tsi578 devices, as indicated in the following table.

Table 4: Tsi578 RIO Device Identity CAR

Bits	Name	Description	Type	Reset value
00:15	DEV_ID	Device Identifier This field contains the IDT-assigned part number of the device.	R	0x0578

1.5.2 Speed Signals

The default values for the SP_IO_SPEED signal has been changed from 01 in the Tsi568A to 10 in the Tsi578.

Table 5 describes the functionality and settings of the SP_IO_SPEED signal. For more information, please refer to the *Tsi578 Serial RapidIO Switch User Manual*.

Table 5: Tsi578 SP_IO_SPEED Description and Values

Pin Name	Pin Count	Type	Description	Recommended Termination
SP_IO_SPEED[1,0]	2	I/O, LVTTL, [PU,PD]	Serial Port Transmit and Receive operating frequency select. SP_IO_SPEED[1,0], these pin select the power-up serial port frequency for *all* ports. 00 - 1.25Gbit/s; 01 - 2.5Gbit/s; 10 - (default) 3.125Gbit/s; 11 - illegal These signals must remain stable for 10 P_CLK cycles after HARD_RST_b is de-asserted in order to be sampled correctly. These signals are ignored after reset and software will be able to over-ride the port frequency setting in the SRIO MAC x Digital Loopback and Clock Selection Register The SP_IO_SPEED[1:0] setting is equal to the SCLK_SEL field in the SRIO MAC x Clock Selection Register. Output capability of this pin is only used in test mode.	Pin must be tied off according to the required configuration. Either a 10K pull-up to VDD_IO or a 10K pull-down to VSS_IO. Internal pull-down may be used for logic 0.

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