



Tsi148/Universe II Differences Application Note

Formal Status
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Introduction

This document outlines the differences between the Tsi148 and the Universe II (CA91C142D) VME bridge devices. It is intended to aid designers with assessing the feasibility of migrating a Tsi148 based design to one that uses a Universe II.

Feature Comparison

Table 1: Feature Comparison

| Feature | Tsi148 | Universe IID (CA91C142D) |
|--|---|--|
| PCI/X Bus Standards | | |
| PCI Rev. 2.2 support | 33–66 MHz | 33 MHz |
| PCI-X Rev 1.0b support | 50–133 MHz | Not supported |
| PCI I/O voltage | 3.3V | 5V |
| PCI bus width | 64-bit | 64-bit |
| VMEbus Standards | | |
| Compliant with VME64 VITA 1-1994 | Yes | Yes |
| Compliant with VME64 Extensions VITA 1.1-1997 | Yes | No |
| Compliant with 2eSST Standard VITA 1.5-2003 | Yes | No |
| VME Slave Interface | | |
| Responds to address modes | A16, A24, A32, A64, CR/CSR | A16, A24, A32, CR/CSR, User AM codes |
| Responds to protocols | SCT, BLT, MBLT, 2eVME, 2eSST | SCT, BLT, MBLT |
| Supports data sizes | D8, D16, D32, D64 | D8, D16, D32, D64 |
| FIFO | Exclusive 4K buffer for posted writes, multi-transaction queuing Exclusive 2K buffer for reads | One 4K buffer for posted writes and prefetch read transactions from VME to PCI |
| Slave images | 8 images 16 bytes to 64K granularity | 8 images 4K to 64K granularity |
| Block read prefetching capability | Yes | Yes |
| Programmable Virtual FIFO size for inbound pre-fetch reads | Yes | No |
| VME64 RETRY capability | Fully compliant | No |

Table 1: Feature Comparison (Continued)

| Feature | Tsi148 | Universe IID (CA91C142D) |
|-----------------------------------|--|--|
| VME Master Interface | | |
| Generates address modes | A16, A24, A32, A64, CR/CSR, User AM Codes | A16, A24, A32, User AM Codes |
| Can generate protocols | SCT, BLT, MBLT, 2eVME, 2eSST | SCT, BLT, MBLT |
| Can generate data sizes | D8, D16, D32, D64 | D8, D16, D32, D64 |
| FIFO | Two exclusive 4K buffers for posted writes; Two exclusive 4K buffers for prefetch reads | One 4K buffer for posted writes and prefetch read transactions from PCI to VME |
| VME64 RETRY capability | Fully compliant | No |
| PCI Target Interface | | |
| Supports 32/64-bit addressing | Yes | No (only 32-bit addressing) |
| Supports 32/64-bit data transfers | Yes | Yes |
| FIFO | Exclusive 4K buffer for posted writes, multi-transaction queuing Exclusive 4K buffer for PCI-X reads, multi-transaction queuing. 512 byte buffer for conventional PCI reads | One 4K buffer for posted writes and prefetch reads for PCI to VME transactions |
| Slave images | 8 images, 64K granularity | 8 images, 4K to 64K granularity |
| Responds to PCI I/O cycles | No | Yes |
| PCI Master Interface | | |
| Supports 32/64-bit addressing | Yes | No (only 32-bit addressing) |
| Supports 32/64-bit data transfers | Yes | Yes |
| Supports 32/64-bit address/data | Yes | No (supports 64-bit data, 32-bit addressing) |
| FIFO | Exclusive 4K buffer for posted writes, multi-transaction queuing Exclusive 4K buffer for PCI-X reads, multi-transaction queuing. 512 byte buffer for conventional PCI reads | One 4K buffer for posted writes and prefetch read transactions from VME to PCI |
| Generates PCI I/O cycles | No | Yes |
| DMA Capabilities | | |
| Channels | Two, independent | One |
| Modes of operation | Two (direct, linked-list) | Two (direct, linked-list) |
| FIFO | Two exclusive 8K byte buffers, one for each channel | One 4K buffer |
| Transfer sizes supported | 1 byte to 4GB | 1 byte to (16MB-1byte) |

Table 1: Feature Comparison (Continued)

| Feature | Tsi148 | Universe IID (CA91C142D) |
|--|---|--|
| Capabilities to control VME bandwidth allocated to DMA | Yes | Yes |
| Interrupts | Done, Halted, Error conditions | Done, Halted, Error conditions |
| DMA direction | PCI-to-VME, VME-to-PCI, VME-to VME, PCI-to-PCI | PCI-to-VME, VME-to-PCI |
| System Controller Capabilities | | |
| Arbitration modes | PRI, RR | PRI, RR |
| Arbiter request modes | Fair, Normal (Demand) | Fair, Normal (Demand) |
| Arbiter release modes | RWD, ROR, ROC, RWD@REQ | ROR, RWD |
| Arbitration request levels | 4 | 4 |
| Bus timer | 8–2048 μ s | 16–1024 μ s |
| System clock driver (16MHz) | Yes | Yes |
| IACK daisy-chain driver | Yes | Yes |
| SYSRESET driver | Yes | Yes |
| Configuration | Power-up option, auto system controller method | Power-up option, auto system controller method |
| Register Access Support | | |
| PCI Configuration Space 0x0–0xFF • Access from PCI | PCI Configuration cycles, Memory cycles through PCI BAR image | PCI Configuration cycles, PCI Memory or I/O cycles |
| PCI Configuration Space 0x0–0xFF • Access from VME | Special combined register group image (any AM code), A24 CR/CSR AM code | A16/A24/A32 cycles through register image, or A24 CR/CSR AM code |
| Extended Register Space 0x100–0xFFF • Access from PCI | PCI Memory through PCI BAR | Two BARs allow access through both Memory and I/O space |
| Extended Register Space 0x100–0xFFF • Access from VME | Special Combined register group image (any AM code), A24 CR/CSR AM code | A16/A24/A32 cycles through register image, or A24 CR/CSR AM code |
| CR/CSR support | Yes | Yes |
| CR/CSR Base Address Configuration | Auto Slot ID, Geographical Addressing | Auto Slot ID |
| Exclusive Access Support | | |
| Generation of VMEbus RMW | Yes | Yes |
| Generation of VME LOCK | Yes (DWB/DHB) | Yes (VOWN bit) |
| Response to VMEbus RMW | Yes | Yes |
| Generation of PCI LOCK# | No | Yes |

Table 1: Feature Comparison (Continued)

| Feature | Tsi148 | Universe IID (CA91C142D) |
|---|--|--|
| Response to PCI LOCK# | No | Yes |
| Semaphores | 8 x 8-bit | 8 x 8-bit |
| VME Interrupt Generation Capabilities | | |
| Levels | IRQ[7:1] | IRQ[7:1] |
| Sources | Software - Register access | Software - Register access, Local interrupt inputs, various internal events |
| Release mode | ROAK | RORA, except software interrupts are ROAK |
| Can map VME interrupts to PCI | Yes (P_INTA-P_INTD) | Yes (8 local interrupts) |
| Can generate VMEbus interrupts via a PCI hardware interrupt | No | Yes |
| PCI Interrupt Generation Capabilities | | |
| PCI interrupts | 4 | 8 |
| Sources | ACFAIL, SYSFAIL on VMEbus, VMEbus IRQ[7:1], and various internal events | ACFAIL, SYSFAIL on VMEbus, VMEbus IRQ[7:1], and various internal events |
| VMEbus Interrupt Handler Capabilities | | |
| Interrupt acknowledge registers | 7 | 7 |
| IACK cycle support | 8, 16, and 32-bit IACK cycles | 8-bit IACK cycles |
| Additional Features | | |
| Error logging register for PCI and VME transactions | Yes | Yes |
| Mechanical/Electrical/Environmental Features | | |
| Packages | 27 X 27 mm 456 PBGA, 1.0 mm ball pitch | 35 x 35 mm 313 PBGA, 1.27 mm pitch |
| Power supplies | 1.8V Core 3.3V I/O | 5V |
| Power dissipation | 2.0W worst case | 3.2W worst case |
| I/O levels | PCI/X 3.3V (not 5V tolerant) VME 3.3V (not 5V tolerant with few exceptions) | 5V |
| Temperature | Commercial: 0°C to 70°C Industrial: -40°C to 85°C | Commercial: 0°C to 70°C Industrial: -40°C to 85°C Extended: -55°C to 125°C |

Performance Comparison

The following performance numbers were based on device-level simulation with the following system configuration:

- PCI Bus Configuration:
 - Bus arbiter was parked on the Tsi148 and Universe II
 - The target was configured for fast decode (that is, 1 clock cycle response)
- VME Bus Configuration:
 - VME slaves were configured to respond with the minimum response time
 - Arbitration delay in each system was ~80 ns (bus request assertion to bus busy assertion)
 - VME Transceiver delays of approximately 5 ns were accounted for in the simulation environment

VME Slave Access Measurement

- Write cycles – Initial VME AS assertion to final DTACK negation following the last data phase. Initial VME AS assertion to final PCI TRDY negation following the last data phase.
- Read cycles – Initial VME AS assertion to final DTACK negation following the last data phase
- Latency – Initial VME AS assertion to initial PCI FRAME assertion

Table 2: VME Slave Access Measurement

| VME Transaction | Device | PCI Bus (Freq, Mode) | AS to DTACK on VME (MB/s) | AS to TRDY on PCI (MB/s) | Latency (ns) |
|---|-------------|----------------------|---------------------------|--------------------------|--------------|
| 32-bit Single Cycle Write | Universe II | 33MHz PCI | 29 | 11.5 | 287 |
| | Tsi148 | 33MHz PCI | 58 | 13.1 | 240 |
| | Tsi148 | 66MHz PCI | 58 | 19.1 | 173 |
| | Tsi148 | 133MHz PCI-X | 62 | 23.1 | 139 |
| 32-bit Single Cycle Read | Universe II | 33MHz PCI | 14.2 | - | 143 |
| | Tsi148 | 33MHz PCI | 11.1 | - | 142 |
| | Tsi148 | 66MHz PCI | 16.1 | - | 105 |
| | Tsi148 | 133MHz PCI-X | 18.6 | - | 94 |
| Sustained Single Cycle Write Throughput - 32 Single Write Cycles (total 128 bytes) | Universe II | 33MHz PCI | 13.7 | 13.4 | - |
| | Tsi148 | 33MHz PCI | 24.2 | 14.8 | - |
| | Tsi148 | 66MHz PCI | 41.4 | 29.1 | - |
| | Tsi148 | 133MHz PCI-X | 41.5 | 40.1 | - |
| Sustained Single Cycle Read Throughput - 32 Single Read Cycles (total 128 bytes) | Universe II | 33MHz PCI | 11.3 | - | - |
| | Tsi148 | 33MHz PCI | 9.6 | - | - |
| | Tsi148 | 66MHz PCI | 13.4 | - | - |
| | Tsi148 | 133MHz PCI-X | 14.9 | - | - |

Table 2: VME Slave Access Measurement (Continued)

| VME Transaction | Device | PCI Bus (Freq, Mode) | AS to DTACK on VME (MB/s) | AS to TRDY on PCI (MB/s) | Latency (ns) |
|-----------------|-------------|----------------------|---------------------------|--------------------------|--------------|
| 2K MBLT Write | Universe II | 33MHz PCI | 108 | 105 | 1,583 |
| | Tsi148 | 33MHz PCI | 97 | 70 | 21,418 |
| | Tsi148 | 66MHz PCI | 97 | 81 | 21,380 |
| | Tsi148 | 133MHz PCI-X | 97 | 88 | 21,432 |
| 2K MBLT Read | Universe II | 33MHz PCI | 101 | - | 207 |
| | Tsi148 | 33MHz PCI | 71 | - | 132 |
| | Tsi148 | 66MHz PCI | 76 | - | 110 |
| | Tsi148 | 133MHz PCI-X | 78 | - | 96 |
| 2K 2eSST Write | Tsi148 | 66MHz PCI | 313 | 193 | 6,736 |
| | Tsi148 | 133MHz PCI-X | 313 | 235 | 6,777 |
| 2K 2eSST Read | Tsi148 | 66MHz PCI | 298 | - | 190 |
| | Tsi148 | 133MHz PCI-X | 301 | - | 180 |

PCI Target Access Measurements

- Write cycles – Initial PCI FRAME assertion to final TRDY negation following the last data phase. Initial PCI FRAME assertion to final VME DTACK negation following the last data phase.
- Read cycles – Initial PCI FRAME assertion to final TRDY negation following the last data phase
- Latency – Initial PCI FRAME assertion to initial VME AS assertion

Table 3: PCI Target Access Measurements

| PCI Transaction | VMEbus | PCI Bus (Freq, Mode) | Device | FRAME to TRDY on PCI (MB/s) | FRAME to DTACK on VME (MB/s) | Latency (ns) |
|---------------------------|--------------|----------------------|-------------|-----------------------------|------------------------------|--------------|
| 32-bit Single Cycle Write | Single Cycle | 33MHz PCI | Universe II | 58 | 13.2 | 258 |
| | | 33MHz PCI | Tsi148 | 52 | 9.0 | 337 |
| | | 66MHz PCI | Tsi148 | 103 | 11.4 | 278 |
| | | 133MHz PCI-X | Tsi148 | 154 | 13.0 | 235 |
| 32-bit Single Cycle Read | Single Cycle | 33MHz PCI | Universe II | 10 | - | 195 |
| | | 33MHz PCI | Tsi148 | 5.4 | - | 359 |
| | | 66MHz PCI | Tsi148 | 7.7 | - | 285 |
| | | 133MHz PCI-X | Tsi148 | 11.3 | x | 152 |

Table 3: PCI Target Access Measurements (Continued)

| PCI Transaction | VMEbus | PCI Bus (Freq, Mode) | Device | FRAME to TRDY on PCI (MB/s) | FRAME to DTACK on VME (MB/s) | Latency (ns) |
|---|--------------|----------------------|-------------|-----------------------------|------------------------------|--------------|
| Sustained Single Cycle Write Throughput - 32 Single Write Cycles (total 128 bytes) | Single Cycle | 33MHz PCI | Universe II | 33.8 | 16.6 | - |
| | | 33MHz PCI | Tsi148 | 33.6 | 31.5 | - |
| | | 66MHz PCI | Tsi148 | 67.4 | 35.8 | - |
| | | 133MHz PCI-X | Tsi148 | 77.4 | 36.2 | - |
| Sustained Single Cycle Read Throughput - 32 Single Read Cycles (total 128 bytes) | Single Cycle | 33MHz PCI | Universe II | 9 | - | - |
| | | 33MHz PCI | Tsi148 | 6.4 | - | - |
| | | 66MHz PCI | Tsi148 | 8.6 | - | - |
| | | 133MHz PCI-X | Tsi148 | 23.4 | - | - |
| 4K PCI Burst Write | MBLT | 33MHz PCI | Universe II | 75 | 68 | 1,187 |
| | | 33MHz PCI | Tsi148 | 266 | 64 | 17,632 |
| | | 66MHz PCI | Tsi148 | 532 | 73 | 9,863 |
| | | 133MHz PCI-X | Tsi148 | 1061 | 78 | 5,987 |
| | 2eSST | 66MHz PCI | Tsi148 | 532 | 176 | 9,863 |
| | | 133MHz PCI-X | Tsi148 | 1061 | 211 | 5,987 |
| 4K PCI Burst Read | MBLT | 33MHz PCI | Universe II | 11.4 | - | 194 |
| | | 33MHz PCI | Tsi148 | 46.7 | - | 405 |
| | | 66MHz PCI | Tsi148 | 53 | - | 285 |
| | | 133MHz PCI-X | Tsi148 | 62 | - | 227 |
| | 2eSST | 66MHz PCI | Tsi148 | 146 | - | 285 |
| | | 133MHz PCI-X | Tsi148 | 277 | - | 227 |

DMA Measurements

The bandwidth was measured as follows:

- PCI-X is the source bus: FRAME assertion to final DTACK negation
- VME is the source bus: VAS assertion to final TRDY negation
- Bandwidth numbers were measured with ideal targets/slave devices
- DMA performance numbers were generated for transferring 8 KB

Table 4: DMA Measurements

| Device | Source Bus | Destination Bus | FRAME on PCI to DTACK on VME (MB/s) | AS on VME to TRDY on PCI (MB/s) |
|-------------|--------------|-----------------|-------------------------------------|---------------------------------|
| Universe II | 33MHz PCI | VME: MBLT | 80 | - |
| Tsi148 | 33MHz PCI | | 79 | - |
| Tsi148 | 66MHz PCI | | 81 | - |
| Tsi148 | 133MHz PCI-X | | 82 | - |
| Tsi148 | 66MHz PCI | VME: 2eSST | 226 | - |
| Tsi148 | 133MHz PCI-X | | 234 | - |
| Universe II | VME: MBLT | 33MHz PCI | - | 55 |
| Tsi148 | | 33MHz PCI | - | 60 |
| Tsi148 | | 66MHz PCI | - | 61 |
| Tsi148 | | 133MHz PCI-X | - | 61 |
| Tsi148 | VME: 2eSST | 66MHz PCI | - | 242 |
| Tsi148 | | 133MHz PCI-X | - | 249 |

Conclusions

The Universe II and Tsi148 are both full-featured VME bridging solutions with VME master and slave capabilities, integrated DMA controllers, and complete VME system controller functionality. These devices provide similar performance when supporting legacy VME protocols (SCT, BLT, and MBLT) and operating at the same PCI bus frequency. The Tsi148 provides a significant performance advantage when the local bus is operating in PCI-X mode at 133 MHz and the VME 2eSST protocol is used in the system.

Another notable difference relates to the PCI bus signaling level. The Universe II supports 5V signalling whereas the Tsi148 supports 3.3V signaling. If all of the PCI bus components are not tolerant of a 5V PCI bus signalling level then additional logic (that is, voltage translation bus switches) will be required on the PCI bus when using the Universe II.

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