



# Tsi148™ VMEbus Test and Set Application Note

Formal Status  
September 6, 2012



# Tsi148 VMEbus Test and Set Application Note

This document details both the traditional mechanisms for implementing a VMEbus Test and Set (TAS) function, as well as additional Tsi148-specific solutions. Topics discussed include the following:

- [Overview](#)
- [Tsi148-specific Wrap-around RMW Solution](#)

## Revision History

September 6, 2012, Formal

This version includes several minor fixes. No technical changes were made.

October 2009, Formal

This version of the document was rebranded as IDT. No technical changes were made.

October 2008, Formal

General content update.

## Overview

The traditional methods for implementing a VMEbus test-and-set (TAS) function include the following:

### 1. A VME RMW cycle

The standard way to implement a TAS is to use the PCI- to-VME bridge device's RMW cycle to set the semaphore. This method is used by a board that does not host the semaphore in its own memory but needs to access the semaphore over the VMEbus. In order to guarantee indivisibility, both the processor host bridge as well as the PCI-to-VME bridge should support the PCI Lock feature.

### 2. Using bus locking capabilities in the PCI-to-VME bridge device

Locking of the VMEbus by using the bus locking capability of the PCI-to-VME bridge device can be used to complete the TAS function. When the VMEbus is locked, the semaphore can be read, tested, and, optionally, written. The same method is used by the board that hosted the semaphore and boards that must cross the VMEbus to access the semaphore.

### 3. Software TAS

The software TAS option continuously re-reads the address to obtain the semaphore. The number of times the address must be read is a configurable value which must be large enough to ensure that no other agent trying to acquire the semaphore could have written its own node-unique locking value to the semaphore. The number of times the address must be read is very system dependent and it is difficult to guarantee the desired locked condition in all circumstances and environments.





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