Tsi110™ Schematic Review Checklist

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1. Tsi110 Schematic Review Checklist

This document offers design and termination recommendations for Tsi110 applications. It is intended for designers who are in the process of completing their Tsi110 board schematics. IDT suggests using this document in conjunction with the Signal Description section of the *Tsi110 User Manual*. For this reason, it is beneficial to review the contents of the checklist information in this document as you develop your Tsi110-based schematic.

This document discusses the following topics:

Related Information

The following information and tools are useful when using this document:

- *Tsi110 User Manual (80E5000_MA001)*
- *Tsi110 Hardware Manual (80E5000_MA002)*
- *Tsi110 Device Errata and Design Notes (80E5000_ER001)*
- IBM PowerPC 750CL and Tsi110 Evaluation Kit Information (see IBM for information)

Revision History

80E5000_AN003_02, Formal, October 2009

This version of the document was rebranded as IDT. It does not include any technical changes.

80E5000_AN003_01, Formal, March 2007

This is the first version of the *Tsi110 Schematic Review Checklist.*

1.1 Processor Interface Signals

The Processor Interface provides the signals necessary to connect the Tsi110 to a PowerPC processor. In general, there should be a one-to-one connection between the Tsi110 and a PowerPC processor, unless otherwise noted.

Table 1: Processor Interface Connections

Tsi110 Signal	Freescale (MPC7447A, MPC7448, MPC7457) Signal Connections	IBM (PowerPC 750CL, 750CXr, 750GX/GL, 750FX/FL) Signal Connections	Additional Information
PB_A[0:35]	A[0:35]	A[0:31] to PB_A[4:35], Pull-down (4.7K) PB_A[0:3]	-
PB_AACKn	AACKn	AACK#	See Note 1
PB_ARTRYn	ARTRYn	ARTRY#	See Note 8
PB_BGn[0]	BGn to PB_BGn[0]	BG# to PB_BGn[0]	See Note 1
PB_BRn[0]	BRn to PB_BRn[0]	BR# to PB_BRn[0].	See Note 1
PB_D[0:63]	D[0:63]	DH[0:31] to PB_D[0:31], DL[0:31] to PB_D[32:63]	-
PB_DBGn[0]	DBGn to PB_DBGn[0]	DBG# to PB_DBGn[0]	See Note 1
PB_DBWO	No connect	DBWO#	-
PB_GBLn	GBLn	GBL#	See Note 1
PB_INTn[0:3]	INTn to PB_INTn[0], MCPn to PB_INTn[1], PB_INTn[2:3] are no connects	Connect INT# to PB_INTn[0], connect MCP# to PB_INTn[1], connect SMI# to PB_INT[2], PB_INTn[3] is a no connect	See Note 1 See Note 2 See Note 7
PB_QREQn[0]	QREQn to PB_QREQn[0]	QREQ# to PB_QREQn[0]	See Note 1 See Note 3
PB_QACKn[0]	QACKn to PB_QACKn[0]	QACK# to PB_QACKn[0]	See Note 1 See Note 3

Table 1: Processor Interface Connections *(Continued)*

Tsi110 Signal	Freescale (MPC7447A, MPC7448, MPC7457) Signal Connections	IBM (PowerPC 750CL, 750CXr, 750GX/GL, 750FX/FL) Signal Connections	Additional Information
PB_RSTn	HRESETn	For information, see IBM documentation and evaluation board schematics.	Pull-up (4.7K to VDD_PB) when open-drain mode is enabled See Note 4
PB_RSTOD	-	The 750GX and 750GL require a push-pull reset signal. The PB_RSTOD signal must be tied to ground.	See Note 4
PB_SYSCLK	CG_PB_CLKO[0]	CG_PB_CLK0[0]	See Note 5
PB_TAn	TAn	TA#	See Note 1
PB_TEAn	TEAn	TEA#	See Note 1
PB_TBSTn	TBSTn	TBST#	See Note 1
PB_TSn	TSn	TS#	See Note 8
PB_TSIZ[0:2]	TSIZ[0:2]	TSIZ[0:2]	-
PB_TT[0:4]	TT[0:4]	TT[0:4]	-
PB_SENSE	-	-	See Note 6

Note 1: There is an internal pull-up on this signal provided by the Tsi110.

Note 2: The 750CXr does not have the SMIn input so PB_INTn[2] will be a no-connect.

Note 3: For information on QACKn functionality in order to generate external logic for Freescale designs, see Freescale Semiconductor document AN2077.

Note 4: The HRESET# and SRESET# signals of the 750CL are to be gated with other reset signals based on system design. SRESET# must be released before HRESET# (for more information, see IBM documentation). HRESET# and SRESET# must be actively driven. Do not use open-drain outputs to drive those signals.

Note 5: This connection assumes the Tsi110 Clock Generator provides the clocks for the system. CG_PB_CLKO[1:0] are Tsi110 clock outputs and are used to clock the Tsi110 and processor when the Tsi110 Clock Generator is enabled. If the Clock Generator is not used, the PB_SYSCLK input must be provided such that it is synchronous with the clock(s) provided to the processor on the 60x bus.

Note 6: Connect this pin through a resistor to ground using a 200-210 Ohm resistor.

Note 7: Interrupt routing schemes are application-specific. The connection information in this document is based on how IDT designed the Tsi110 evaluation boards.

Note 8: When connecting the Tsi110 to a 750CL, this signal must be pulled up to 1.8v_PB with a 1K Ohm resistor.

1.2 Memory Controller Signals

The Memory Controller provides the signals necessary to connect the Tsi110 to external memory devices. The Memory Controller supports direct connection DDR2 SDRAM implemented either as soldered-down devices, or as DIMMs. Since there are many possibilities when designing in soldered-down devices, this section covers the most common use of the Memory Controller: connections to DIMM and SODIMM connectors. For an example of a connection to a DDR2 DIMM, see the IBM750GX and the IBM 750CL Evaluation Kit Reference Design Schematics.

Table 2: Memory Controller Connections

Tsi110 Signal	DIMM (Slot 0)	DIMM (Slot 1)	SODIMM (Slot 0)	SODIMM (Slot1)	Additional Information
SD_SYSCLK	-	-	-	-	See Note 9
SD_A[15:0]	A[15:0]	A[15:0]	A[15:0]	A[15:0]	See Note 8
SD_BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	See Note 8
SD_CASn	CAS#	CAS#	CAS#	CAS#	See Note 8
SD_CLK_P[5:0]	CK[2:0] to SD_CLK_P[2:0]	CK[2:0] to SD_CLK_P[5:3]	CK[1:0] to SD_CLK_P[1:0]	CK[1:0] to SD_CLK_P[4:3]	See Note 1 See Note 2 See Note 10
SD_CLK_N[5:0]	CK[2:0]N to SD_CLK_N[2:0]	CK[2:0]N to SD_CLK_N[5:3]	CK[1:0]N to SD_CLK_N[1:0]	CK[1:0]N to SD_CLK_N[4:3]	See Note 1 See Note 2 See Note 10
SD_CLKEN[1:0]	CKE[1:0]	CKE[1:0]	CKE[1:0]	CKE[1:0]	See Note 3 See Note 8
SD_CLKFBI_P	-	-	-	-	See Note 4
SD_CLKFBI_N	-	-	-	-	See Note 4
SD_CLKFBO_P	-	-	-	-	See Note 4
SD_CLKFBO_N	-	-	-	-	See Note 4
SD_CSn[3:0]	S[1:0]N to SD_CSn[1:0]	S[1:0]N to SD_CSn[3:2]	S[1:0]N to SD_CSn[1:0]	S[1:0]N to SD_CSn[3:2]	See Note 1 See Note 3 See Note 8
SD_DQ[63:0]	DQ[63:0]	DQ[63:0]	DQ[63:0]	DQ[63:0]	-
SD_DQS_P[16:0]	DQS[7:0] to SD_DQS_P[7:0] DM[7:0] to SD_DQS_P[16:9]	DQS[7:0] to SD_DQS_P[7:0] DM[7:0] to SD_DQS_P[16:9]	DQS[7:0] to SD_DQS_P[7:0] DM[7:0] to SD_DQS_P[16:9]	DQS[7:0] to SD_DQS_P[7:0] DM[7:0] to SD_DQS_P[16:9]	See Note 5
SD_DQS_N[16:0]	DQS[7:0]N to SD_DQS_N[7:0]	DQS[7:0]N to SD_DQS_N[7:0]	DQS[7:0]N to SD_DQS_N[7:0]	DQS[7:0]N to SD_DQS_N[7:0]	See Note 5

Table 2: Memory Controller Connections *(Continued)*

Tsi110 Signal	DIMM (Slot 0)	DIMM (Slot 1)	SODIMM (Slot 0)	SODIMM (Slot1)	Additional Information
SD_I2C_CLK	SCL	SCL	SCL	SCL	See Note 6
SD_I2C_SD	SDA	SDA	SDA	SDA	See Note 6
SD_RASn	RAS#	RAS#	RAS#	RAS#	See Note 8
SD_VREF[1:0]	-	-	-	-	See Note 7
SD_WEn	WE#	WE#	WE#	WE#	See Note 8
SD_ODT[3:0]	ODT[1:0] to SD_ODT[1:0]	ODT[1:0] to SD_ODT[3:2]	ODT[1:0] to SD_ODT[1:0]	ODT[1:0] to SD_ODT[3:2]	See Note 1 See Note 3 See Note 8
SD_DLL_TEST[1:0]	-	-	-	-	Leave unconnected

Note 1: When designs require only a single DIMM or SODIMM, the unused Tsi110 outputs can be left unconnected.

Note 2: For DIMMs and SODIMMs, place a compensation capacitor (5pf) between the positive and negative lines of the clock signal near the input of the DIMM. For more information, see “Board Layout Guidelines” in the *Tsi110 Hardware Manual*, and the IBM750GX and IBM 750CL Reference Designs.

Note 3: For DIMMs, place 5.1 ohm resistors in series from the Tsi110 pin to the DIMM connector pin (SODIMM designs do not require these resistors). For more information, see the IBM750GX and the IBM 750CL Reference Design.

Note 4: Connect SD_CLKFBI_N to SD_CLKFBO_N through a 22-ohm series resistor. Connect SD_CLKFBI_P to SD_CLKFBO_P through a 22-ohm series resistor. For more information about routing these signals, see “Board Layout Guidelines” in the *Tsi110 Hardware Manual*.

Note 5: All unused Tsi110 SD_DQS_P and SD_DQS_N signals should be left unconnected. SD_DQS_P[8] and SD_DQS_N[8] do not exist on the Tsi110.

Note 6: Place a pull-up (10K) to VDD_PC (3.3V) on this signal.

Note 7: For information on connection and de-coupling, see “Board Layout Guidelines” in the *Tsi110 Hardware Manual*, and the IBM750GX and IBM 750CL Reference Designs.

Note 8: For DIMMs and SODIMMs, these signals require a Stub termination resistor (47 ohm). For information on routing these signals, see “Board Layout Guidelines” in the *Tsi110 Hardware Manual*.

Note 9: SD_SYSCLK should be pulled up (4.7K) to VDD_PB if the Clock Generator is used or tie to ground.

Note 10: These signals do not have to be connected exactly as described. For example, the SD_CLK_P and SD_CLK_N outputs do not have to be connected exactly as indicated; the only restriction is that the connection is made point to point. The connection information in this document is based on the design of the Tsi110 evaluation board.

1.3 PCI/X Interface Signals

The PCI/X Interface provides the signals necessary to connect the Tsi110 to a PCI/X bus.

Table 3: PCI/X Interface Connections

Tsi110 Signal	PCI/X Bus Signal Connections	Additional Information
PCI_ACK64n	ACK64n	Pull-up (8.2K) to 3.3V (See Note 1)
PCI_AD[63:0]	AD[63:0]	Pull-up (8.2K) to 3.3V on PCI_AD[63:32] (See Note 1)
PCI_CBEn[7:0]	C/BE[7:0]#	Pull-up (8.2K) to 3.3V on PCI_CBEn[7:4] (See Note 1)
PCI_CLK	CLK	Point to Point to individual low-skew driver
PCI_DEVSELn	DEVSEL#	Pull-up (8.2K) to 3.3V (See Note 1)
PCI_FRAMEn	FRAME#	Pull-up (8.2K) to 3.3V (See Note 1)
PCI_GNTn[7:1]	-	Pull-up (8.2K) to 3.3V, If the Tsi110 internal arbiter is enabled, these signals are Tsi110 outputs used to grant access to the PCI/X bus. If an external arbiter is used, PCI_GNTn[1] is an input to the Tsi110.
PCI_IDSEL	IDSEL	Resistively coupled (2K) to AD line, Please refer to PCI/X Interface (IO and Configuration Operations) section of the *Tsi110 User Manual* (I/O and configuration operations) for additional detail.
PCI_INTAn	INTA#	Pull-up (8.2K) to 3.3V (See Note 2)
PCI_INTBn	INTB#	Pull-up (8.2K) to 3.3V (See Note 2)
PCI_INTCn	INTC#	Pull-up (8.2K) to 3.3V (See Note 2)
PCI_INTDn	INTD#	Pull-up (8.2K) to 3.3V (See Note 2)
PCI_IRDYn	IRDY#	Pull-up (8.2K) to 3.3V (See Note 1)
PCI_M66EN	M66EN	-
PCI_PAR	PAR	-
PCI_PAR64	PAR64	Pull-up (8.2K) to 3.3V (See Note 1)
PCI_PCIXCAP[1:0]	-	If the system includes slots for add-in cards, a circuit must be provided such that the PCIXCAP pin for all add-in cards be sampled. This logic must translate the PCIXCAP level into the 2 bit PCI_PCIXCAP[1:0] signals which latch on the rising edge of PCI_RSTn. Fully embedded systems can simply strap these signals to the desired PCI/X mode.
PCI_PERRn	PERR#	Pull-up (8.2K) to 3.3V (See Note 1)
PCI_PMEn	PME#	Pull-up (8.2K) to 3.3V (See Note 1)

Table 3: PCI/X Interface Connections *(Continued)*

Tsi110 Signal	PCI/X Bus Signal Connections	Additional Information
PCI_REQn[7:1]	-	Pull-up (8.2K) to 3.3V, If the Tsi110 internal arbiter is enabled these signals are Tsi110 inputs used by external masters to request access to the PCI/X bus. If an external arbiter is used, PCI_REQn[1] is an output used by the Tsi110 to request access to the PCI/X bus.
PCI_REQ64n	REQ64#	Pull-up (8.2K) to 3.3V (See Note 1)
PCI_RSTn	RST#	Pull-up (8.2K) to 3.3V
PCI_RSTDIR	-	Sets the Host/Agent status of the Tsi110. For more information, see the *Tsi110 User Manual*.
PCI_SERRn	SERR#	Pull-up (8.2K) to 3.3V (See Note 1)
PCI_STOPn	STOP#	Pull-up (8.2K) to 3.3V (See Note 1)
PCI_TRDYn	TRDY#	Pull-up (8.2K) to 3.3V (See Note 1)
PCI_ENUMn	ENUM#	Pull-up (8.2K) to 3.3V
PCI_ES	SWITCH	Pull-down (8.2K)
PCI_HEALTHYn	HEALTHY#	Pull-down (1K)
PCI_HS64ENn	64EN#	Pull-up (8.2K) to 3.3V
PCI_LEDn	LED#	Pull-up (8.2K) to 3.3V
PCI_SENSE	-	Pull-down (150ohm)

Note 1: These pull-ups must exist somewhere in the system; usually an add-in card can rely on the motherboard to provide these terminations.

Note 2: When PCI interrupts are configured as outputs, the interrupt outputs of the Tsi110 Interrupt Controller are driven to both the PCI_INTn and PB_INTn outputs of the Tsi110. Both the local processor connected to PB_INTn and an external PCI master connected to PCI_INTn should not handle the same interrupt. In systems that use the PCI_INTn outputs, the corresponding PB_INTn outputs should be left unconnected.

1.4 Ethernet Controller Signals

The Ethernet Controller provides the signals necessary to connect the Tsi110 to external PHY devices through two independent Gigabit Ethernet ports, E0 and E1. The Ethernet Controller supports direct connection to external PHYs operating in MII/GMII and TBI modes. For an example of a connection to an external PHY operating in GMII mode, see the IBM750GX and the IBM 750CL Reference Design schematics.

Designs using only one of the Tsi110 Ethernet ports, E0, must make sure all Tsi110 inputs for the unused port, E1, are connected on the board through (1K) pull-down resistors.

Table 4: Ethernet Controller Connections

Tsi110 Signal	MII Connection	GMII Connection	TBI Connection	Additional Information
E_0_TCG[9:0]	TXD[3:0] to E_0_TCG[3:0], TXEN to E_0_TCG[8], TXER to E_0_TCG[9]	TXD[7:0] to E_0_TCG[7:0], TXEN to E_0_TCG[8], TXER to E_0_TCG[9]	TXD[9:0]	See Note 1 See Note 2
E_0_RCG[9:0]	RXD[3:0] to E_0_RCG[3:0], RXDV to E_0_RCG[8], RXER to E_0_RCG[9]	RXD[7:0] to E_0_RCG[7:0], RXDV to E_0_RCG[8], RXER to E_0_RCG[9]	RXD[9:0]	See Note 3 See Note 4
E_0_PCRS_SDET	CRS	CRS	SDET	See Note 4
E_0_PCOL_RBCM	COL	COL	MODES See Note 5	See Note 1 See Note 4
E_0_ECMDT	-	-	EN_CDET	See Note 1 See Note 2
E_0_EWRAP	-	-	EWRAP	See Note 1 See Note 2
E_0_PRBSEN	-	-	PRBS_EN See Note 6	See Note 1 See Note 2
E_0_PRBS_PASS	-	-	PRBS_PASS See Note 6	See Note 3 See Note 4
E_0_RXCLK	RXC	RXC	PMA_RX_CLK[0] See Note 7	See Note 3
E_0_TXCLK	TXC	TXC	PMA_RX_CLK[1] See Note 7	See Note 3
E_1_TCG[9:0]	TXD[3:0] to E_1_TCG[3:0], TXEN to E_1_TCG[8], TXER to E_1_TCG[9]	TXD[7:0] to E_1_TCG[7:0], TXEN to E_1_TCG[8], TXER to E_1_TCG[9]	TXD[9:0]	See Note 1 See Note 2

Table 4: Ethernet Controller Connections *(Continued)*

Tsi110 Signal	MII Connection	GMII Connection	TBI Connection	Additional Information
E_1_RCG[9:0]	RXD[3:0] to E_1_RCG[3:0], RXDV to E_1_RCG[8], RXER to E_1_RCG[9]	RXD[7:0] to E_1_RCG[7:0], RXDV to E_1_RCG[8], RXER to E_1_RCG[9]	RXD[9:0]	See Note 3 See Note 4
E_1_PCRS_SDET	CRS	CRS	SDET	See Note 4
E_1_PCOL_RBCM	COL	COL	MODES See Note 5	See Note 1 See Note 4
E_1_ECMDT	-	-	EN_CDET	See Note 1 See Note 2
E_1_EWRAP	-	-	EWRAP	See Note 1 See Note 2
E_1_PRBSEN	-	-	PRBS_EN See Note 6	See Note 1 See Note 2
E_1_PRBS_PASS	-	-	PRBS_PASS See Note 6	See Note 3 See Note 4
E_1_RXCLK	RXC	RXC	PMA_RX_CLK[0] See Note 7	See Note 3
E_1_TXCLK	TXC	TXC	PMA_RX_CLK[1] See Note 7	See Note 3
E_MDC	MDC	MDC	MDC	See Note 1
E_MDIO	MDIO	MDIO	MDIO	See Note 1 See Note 8
E_REF125	CLK125	CLK125	CLK125	See Note 4
E_GTXCLK[1:0]	GTX_CLK for PHY0 to E_GTXCLK[0], GTX_CLK for PHY1 to E_GTXCLK[1]	GTX_CLK for PHY0 to E_GTXCLK[0], GTX_CLK for PHY1 to E_GTXCLK[1]	PMA_TX_CLK for PMA0 to E_GTXCLK[0], PMA_TX_CLK for PMA1 to E_GTXCLK[1]	See Note 1

Note 1: For G/MII, place 33-ohm resistors in series from the Tsi110 pin to the PHY pin. For more information, see the IBM750GX and the IBM 750CL Reference Design. For TBI, place 33-ohm resistors in series from the Tsi110 pin to the PMA.

Note 2: Unused Tsi110 outputs can be left unconnected.

Note 3: Unused Tsi110 inputs should have pull-downs on them (1K).

Note 4: To determine if a source termination resistor is required, see to the PHY vender specification.

Note 5: Some TBI PMAs allow for an external input to determine how the output clocks are driven. The Tsi110 drives the RBCM output based on a software setting. This output can be connected to PMAs that support this feature to determine whether it drives only the PMA_RX_CLK0 at 125MHz, or both PMA_RX_CLK0 and PMA_PX_CLK1 at 62.5MHz and 180 degrees out of phase. If the PMA does not support this feature this signal can be left unconnected.

Note 6: Some TBI PMAs contain an internal test mode that can be enabled by the Tsi110 through the E_x_PRBSEN output. When enabled, the PMA returns a status to the Tsi110 through the E_x_PRBS_PASS input. If the external PMA does not support this feature, E_x_PRBSEN should be left unconnected and E_x_PRBS_PASS should be pulled up (4.7K)to 3.3V.

Note 7: For TBI mode, E_x_RXCLK is connected to PMA_RX_CLK[0] and operates at either 125MHz or 62.5MHz depending on how the PMA is generating the clocks. E_x_TXCLK connects to PMA_RX_CLK[1].

Note 8: E_MDIO requires a pull-up to 3.3V; the resistor value is normally recommended by the PHY vendor. For more information, see the IBM750GX and the IBM 750CL Reference Design.

1.5 Interrupt Controller Signals

The Tsi110 provides four external interrupt request inputs.

Table 5: Interrupt Controller Connections

Tsi110 Signal	Additional Information
INT[3:0]	Pull-up (4.7K) unused inputs to 3.3V

1.6 I^2C Interface Signals

The I^2C Interface provides the signals necessary to connect the Tsi110 to an EEPROM for initializing device registers at power-up.

Table 6: I^2C Interface Connections

Tsi110 Signal	EEPROM	Additional Information
I2C_SCLK	SCL	Pull-up (10K) to 3.3V
I2C_SD	SDA	Pull-up (10K) to 3.3V

1.7 HLP Interface Signals

The HLP Interface provides the signals necessary to connect the Tsi110 to external peripherals, such as ROM, EEPROM, FLASH, SRAM, or SRAM/ROM-like devices, or more sophisticated peripherals that use the “READY” style handshake. The HLP Interface can be connected to 8-, 16-, and 32-bit devices with no, or minimal, discrete glue logic. Because there are many configuration options this interface is not discussed on a complete per pin basis.

Figures 1 and 2 show the basic connections for the HLP Interface’s most common usage: connection of Flash/ROMs in Latch and Non-Latch mode. For specific examples including connection to 8- and 32-bit memory devices, see the IBM750GX and the IBM 750CL Reference Design schematics.

Table 7: HLP Interface Connections

Tsi110 Signal	Additional Information
HLP_AD[31:0]	Many of these signals are multiplexed with power-up configuration signals (for more information, see Section 1.15 on page 18).
HLP_LE	If the HLP Interface is used in Non-latch mode, this signal can be left unconnected.
HLP_RDY	Pull-up (4.7K) to 3.3V

Figure 1: Connection of Flash/ROMs to the HLP Interface for Latch Mode

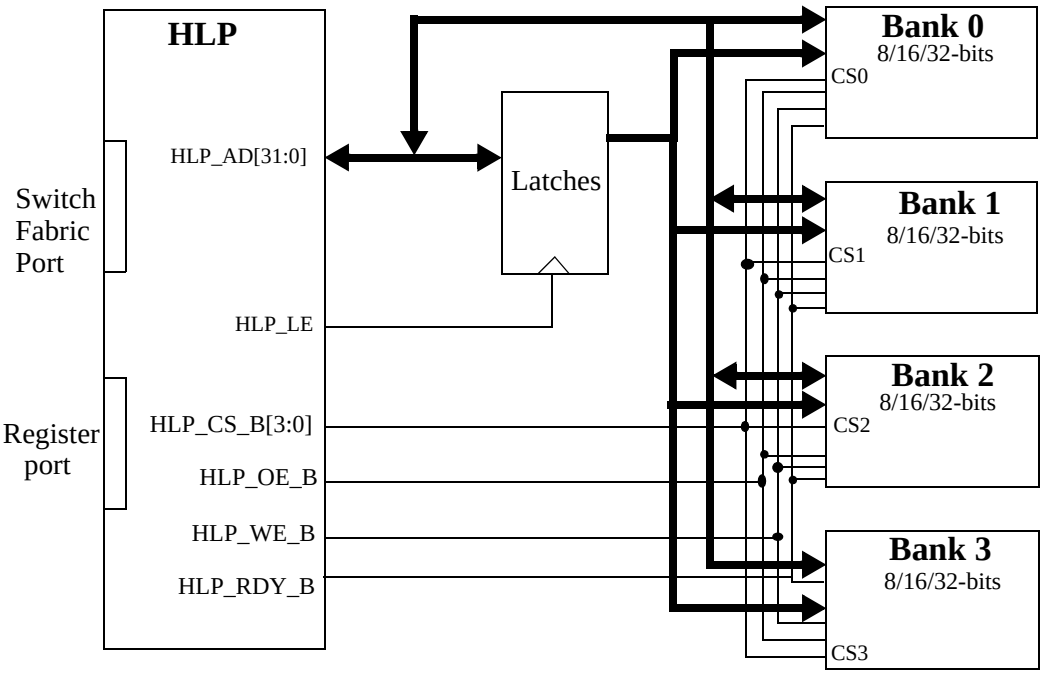
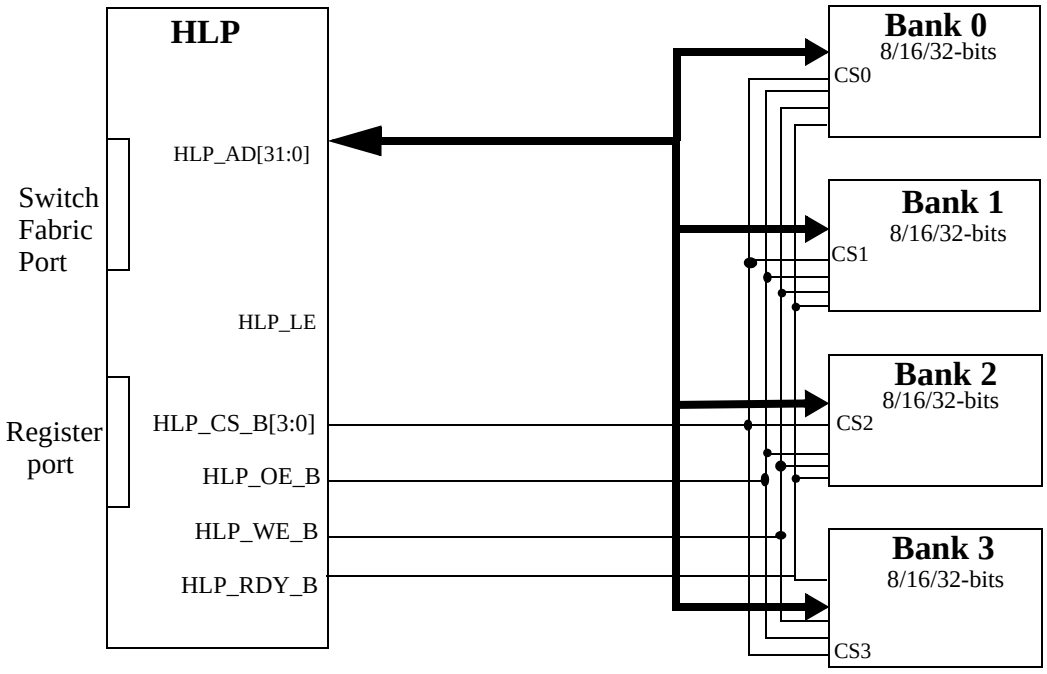


Figure 2: Connection of Flash/ROMs to HLP Interface for Non-Latch Mode



1.7.1 HLP Interface Address and Data Bus Mapping

The HLP Interface maps the address and data onto the HLP_AD pins for three data path width options. Tables 8 to 10 indicate how the address and data is presented over the HLP_AD pins for the various modes supported.

Table 8: HLP — 8-bit mode[a]

HLP_AD	31 - 24	23 - 16	15 - 8	7 - 4	3 - 0
Address Phase (Latch Mode only)	A27 - A20	A19 - A12	A11 - A4	A3 - A0	A23 - A20
Data Phase (Latch/Non-latch mode)	D7 - D0	A19 - A12	A11 - A4	A3 - A0	A23 - A20

a. “Ax - Ay” indicate address bits, “Dx - Dy” indicate data bits.

Table 9: HLP — 16-bit mode[a]

HLP_AD	31 - 24	23 - 16	15 - 8	7 - 5	4	3	2	1 - 0
Address Phase (Latch Mode only)	A27 - A20	A19 - A12	A11 - A4	A3 - A1	X	X	X	B1 - B0
Data Phase (Latch/Non-latch mode)	D15 - D8	D7 - D0	A11 - A4	A3 - A1	X	X	X	B1 - B0

a. “Ax - Ay” indicate address bits, “Dx - Dy” indicate data bits, “Bx” indicate byte enable bits, and “X” indicate undefined entries.

Table 10: HLP — 32-bit mode[a]

HLP_AD	31 - 24	23 - 16	15 - 8	7 - 6	5	4	3 - 0
Address Phase (Latch Mode only)	A27 - A20	A19 - A12	A11 - A4	A3 - A2	X	X	B3 - B0
Data Phase (Latch/Non-latch mode)	D31 - D24	D23 - D16	D15 - D8	D7 - D0			

a. “Ax - Ay” indicate address bits, “Dx - Dy” indicate data bits, “Bx” indicate byte enable bits, and “X” indicate undefined entries.

1.8 GPIO Interface Signals

The Tsi110 provides 16 general purpose input/outputs.

Table 11: GPIO Interface Connections

Tsi110 Signal	Additional Information
GPIO[15:0]	These signals can be configured as input, output and open-drain under program control. For more information, see the *Tsi110 User Manual*.

1.9 UART Interface Signals

The UART Interface contains two UARTS that can convert data from the Host processor to serial data for serial devices.

Table 12: UART Interface Connections

Tsi110 Signal	Serial Device	Additional Information
U_0_RX	To output of Serial device	Unused U_x_RX inputs should be pulled up (4.7K) to 3.3V.
U_0_TX	To input of Serial device	Unused U_x_TX outputs can be left unconnected.
U_1_RX	To output of Serial device	Unused U_x_RX inputs should be pulled up (4.7K) to 3.3V.
U_1_TX	To input of Serial device	Unused U_x_TX outputs can be left unconnected.

1.10 JTAG Interface and Test Signals

The JTAG Interface includes dedicated user-accessible test logic that is compliant with the IEEE1149.1 standard.

Table 13: JTAG Interface and Test Connections

Tsi110 Signal	IEEE1149.1 Connection	Additional Information
JTAG_TCK	TCK	Pull-up (10K) to 3.3V
JTAG_TMS	TMS	Pull-up (10K) to 3.3V
JTAG_TDI	TDI	Pull-up (10K) to 3.3V
JTAG_TDO	TDO	Pull-up (10K) to 3.3V
JTAG_TRSTn	TRSTn	Pull-down (2K)
TEST_ON	-	Pull-down (4.7K)
TEST_BIDR_CTL	-	Pull-down (4.7K)
TEST_TM[3:0]	-	Pull-down (4.7K)

1.11 Clock Generator Signals

The Clock Generator circuitry includes PLLs and dividers that can generate independent clocks for the Processor Interface, Memory Controller, PCI/X Interface, and internal logic.

Table 14: Clock Generator Connections

Tsi110 Signal	Additional Information
CG_REF	1.8V, 33.3MHz reference clock, Crystal Oscillators or PLL-based programmable clock devices can be used as the clock source.
CG_PB_CLK0[1:0]	See Note 1, Unused Tsi110 outputs can be left unconnected.
CG_PCI_CLK0[3:0]	See Note 1, Unused Tsi110 outputs can be left unconnected.
CG_PB_SELECT[2:0]	Pull these inputs to VDD_PB or ground depending on the required frequency setting.
CG_SD_SELECT[2:0]	Pull these inputs to VDD_PB or ground depending on the required frequency setting.

Note 1: Place 33-ohm resistors in series from the Tsi110 pin to the clock input pin. For more information, see the IBM750GX and the IBM 750CL Reference Design.

1.12 Switch Fabric Signals

The Tsi110 provides an asynchronous active-low reset for the Switch Fabric and the Tsi110.

Table 15: Switch Fabric Connections

Tsi110 Signal	Additional Information
OCN_RSTn	This signal should have a pull-up (4.7K) to 3.3V; however, some designs use an FPGA to control the resets. If this is the case, a pull-down on this signal can be used so that the reset is held active while the FPGA is being programmed. For more information about the functionality of this signal, see the *Tsi110 User Manual*.

1.13 PLL Power Signals

For recommended filtering information, see the *Tsi110 Hardware Manual*.

1.14 Power Supply Signals

For power supply sequencing requirements, see the *Tsi110 Hardware Manual*.

1.15 Power-up Configuration Signals

The Tsi110 provides a number of power-up options that are latched during a device reset. The Tsi110 HLP address/data lines are used as shared signals for these power-up options. IDT recommends placing both pull-up (4.7K to 3.3V) and pull-down (4.7K) resistors on the board, and populating one or the other based on the chosen power-up configuration.

For the Tsi110, HLP_AD[6] and HLP_AD[8] must be pulled high.

1.16 Reserved Signals

The Tsi110 has a number of reserved signals that require special termination, including:

- RESERVED[29:0] – Each signal requires a 4.7K pull-up resistor to VDD_PB.
- RIU (Reserved for internal use) – This signal must be connected to VSS_IO.

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