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Introduction

This application note describes transmission of serial data by using the clock-synchronous transfer function of the serial communications interface with FIFO (SCIF). This application note is a summary for quick reference of information required in the design of user software.

Target Device

SH7285

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1. Preface .............................................................................................................................................. 2
2. Description of the Sample Application ......................................................................................... 3
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1. Preface

1.1 Specifications

This sample application employs the clock-synchronous serial transfer function of the serial communications interface with FIFO (SCIF) to perform data transmission. Figure 1 shows an example of connection for transmission by the SCIF in clock-synchronous mode.

- SCIF3 is used.
- The communications format has a fixed 8-bit data length.
- The transmit trigger number is set to 8, and character strings are transmitted by using the transmit-FIFO-data-empty interrupt.
- Once 32 bytes of data have been transmitted, operation for transmission is halted.

![Figure 1](connection_example.png)

**Figure 1** Connection Example for Transmission by the SCIF in Clock-Synchronous Mode

1.2 Module Used

Serial communications interface with FIFO (SCIF)

1.3 Applicable Conditions

<table>
<thead>
<tr>
<th>MCU</th>
<th>SH7285</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating frequency</td>
<td>Internal clock: 100 MHz</td>
</tr>
<tr>
<td></td>
<td>Bus clock: 50 MHz</td>
</tr>
<tr>
<td></td>
<td>Peripheral clock: 50 MHz</td>
</tr>
<tr>
<td>C compiler</td>
<td>SuperH RISC Engine Family C/C++ Compiler Package Ver.9.11</td>
</tr>
<tr>
<td>(from Renesas Technology Corp.)</td>
<td></td>
</tr>
</tbody>
</table>
2. Description of the Sample Application

This sample application employs the transmit-FIFO-data-empty interrupt (TXI) source of the serial communications interface with FIFO (SCI) to transmit serial data in clock-synchronous mode. In clock-synchronous mode, the SCIF transmits serial data in synchronization with clock pulses.

2.1 Summary of MCU Module Used

In clock-synchronous mode, the SCIF transmits and receives data in synchronization with clock pulses. This mode is suitable for high-speed serial communications. An internal clock or an external clock from the SCK pin can be selected as the SCIF clock source. When an internal clock has been selected, a synchronizing clock is output from the SCK pin. When an external clock has been selected, a synchronizing clock is input into the SCK pin. The transmitting and receiving sections of the SCIF are independent, so full-duplex communication is possible while sharing the same clock.

Both the transmitter and receiver have a 16-stage FIFO buffered structure so that data can be read or written during transmission and reception, which enables high-speed continuous data transfer.

In clock-synchronous serial communications, each data bit is output on the communication line from one falling edge of the serial clock to the next. Data is guaranteed valid at the rising edge of the serial clock.

In each character, the serial data bits are transmitted in order from the LSB (first) to the MSB (last). After output of the MSB, the communication line remains in the state of the MSB.

For details on the SCIF, please refer to the section on serial communications interface with FIFO in the SH7280 Group Hardware Manual.

Table 1 gives an overview of serial communications in clock-synchronous mode. Figure 2 shows a block diagram of the SCIF.

Table 1 Overview of Serial Data Communications in Clock-Synchronous Mode

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of interfaces</td>
<td>1 (SCIF3)</td>
</tr>
</tbody>
</table>
| Clock sources       | For internal clock: Pφ, Pφ/4, Pφ/16, Pφ/64 (Pφ: peripheral clock)  
                       | For external clock: input clock on the SCK3 pin                           |
| Data format         | Transfer data length: Fixed at 8 bits                                       |
|                    | Order: LSB first and MSB first are selectable                               |
| Baud rate           | For internal clock: 1 kbps to 2 Mbps (Pφ = 50 MHz)                         |
|                    | For external clock: up to 8,333,333.3 bps (Pφ = 50 MHz, external input clock of 8.3333 MHz) |
| Error detection     | Overrun error                                                              |
| Interrupt requests  | Transmit-FIFO-data-empty interrupt (TXI)                                   |
|                    | Receive-FIFO-data-full interrupt (RXI)                                      |
|                    | Break interrupt (BRI)                                                      |
| Clock sources       | Internal and external clocks are selectable                                 |
|                    | • Internal clock                                                            |
|                    | When the internal clock has been selected, the SCIF operates using the clock from the baud-rate generator and outputs this clock to external devices as the synchronizing clock. |
|                    | • External clock                                                           |
|                    | When the external clock has been selected, the SCIF operates on the input synchronizing clock, not using the on-chip baud rate generator. |
Figure 2  Block Diagram of the SCIF

[Legend]
- SCRSR: Receive shift register
- SCFRDR: Receive FIFO data register
- SCTSR: Transmit shift register
- SCFTDR: Transmit FIFO data register
- SCSMR: Serial mode register
- SCSCR: Serial control register
- SCBRR: Bit rate register
- SCSPT: Serial port register
- SCFCR: FIFO control register
- SCFDR: FIFO data count register
- SCLSR: Line status register
- SCSEMR: Serial extended mode register

- RXD3
- TXD3
- SCK3
- SCIF
- TXI
- RXI
- ERI
- BRI
2.2 Description of the Sample Program

Table 2 gives the settings for SCIF communications function of this sample program, and figure 3 shows the operations in data transmission.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Module</td>
<td>SCIF3</td>
</tr>
<tr>
<td>Communications mode</td>
<td>Clock-synchronous mode</td>
</tr>
<tr>
<td>Interrupts</td>
<td>Transmit-FIFO-data-empty interrupt (TXI)</td>
</tr>
<tr>
<td>Transfer rate</td>
<td>100 kbps</td>
</tr>
<tr>
<td>Number of data to be received</td>
<td>32 bytes</td>
</tr>
<tr>
<td>Data length</td>
<td>8-bit data</td>
</tr>
<tr>
<td>Bit order</td>
<td>LSB-first</td>
</tr>
<tr>
<td>Synchronizing clock</td>
<td>Internal clock/ synchronizing clock on the SCK pin</td>
</tr>
<tr>
<td>FIFO data trigger number</td>
<td>Transmit FIFO data trigger: 8</td>
</tr>
<tr>
<td>Loop-back test function</td>
<td>Disabled</td>
</tr>
</tbody>
</table>

![Figure 3 Operations for Data Transmission](image-url)
2.3 Procedure for Setting Module Used

This section describes the procedure for setting up SCIF3 for clock-synchronous mode operation.

Figure 4 shows the flow of processing by the sample program, figure 5 shows the flow of settings for release from module-standby mode, figure 6 shows the flow for setting up the pin function controller. Furthermore, figure 7 shows the flow for initialization of data transmission in clock-synchronous mode, and figure 8 shows the flow for handling transmit interrupts in clock-synchronous mode. For details on the settings of individual registers, see the *SH7280 Group Hardware Manual*.

---

**Figure 4   Flow of Processing by the Sample Program**

```
main

Release from power-down mode
stbcr_init() [1] [1] Clock is supplied to SCIF3.

Initialization of SCIF3
scif_init() [2] [2] Initialization of the serial communication interface with FIFO SCIF3 is set.

Initialization of PFC
pfc_init() [3] [3] Initialization of the pin function controller Input and output pins of the SCIF are set.

Setting of the interrupt level
INTC.IPR14.BIT._SCIF3 = 0xF [4] [4] Setting of the SCIF interrupt level Interrupt level of the SCIF3 is set to D'15.

NO
Initialization of variables completed?

YES
Enable data transmission by the SCIF
SCIF3.SCFSR.BIT.TDFE &= 0x0 [5] [5] TDFE flag is cleared to enable transmission of data.

Change of interrupt mask level
set_imask(0) [6] [6] The interrupt mask level is set to D'0.

[7] [7] Loop processing
```
**Figure 5  Flow of Settings for Release from Module-Standby Mode**

```
| stbcr_init()          | [1] Enabling clock supply to SCIF3
|-----------------------|----------------------------------
| Set standby control 4 | SCIF3: MSTP44 bit is set to B'0. |
| (STBCR4)              |                                  |
```

**Figure 6  Flow for Setting up the Pin Function Controller**

```
| pfc_init()          | [1] Setting of multiplexed pins as SCIF input and output pins
|---------------------|--------------------------------------------------------------
| Set port E control  | SCK3: PE6MD is set to B'101.                               |
| register L2 (PECRL2) | TXD3: PE5MD is set to B'101.                               |
| END                 |                                                              |
scif_init()

Set serial control register (SCSCR_3)

[1] Setting to disable transmission and reception of data
  TE (Transmit enable) bit is set to B'0.
  RE (Receive enable) bit is set to B'0.

Set FIFO control register (SCFCR_3)

[2] Initialization of data held in the FIFO queue
  RFRST (Receive FIFO data register reset) bit is set to B'1.
  TFRST (Transmit FIFO data register reset) bit is set to B'1.

Set serial status register (SCFSR_3)

[3] Clearing of the error status
  ER (Receive error) bit is cleared to B'0.
  BRK (Break detection) bit is cleared to B'0.
  DR (Receive data ready) bit is cleared to B'0.

Set line status register (SCLSR_3)

[4] Clearing of the error status
  ORER (Overrun error) bit is cleared to B'0.

Set serial control register (SCSCR_3)

[5] Selection of clock source and setting of clock output
  CKE (clock enable) bit is set.

Set serial mode register (SCSMR_3)

[6] Setting of serial communications format
  C/A (communication mode) bit is set to B'1.
  CKS (clock select) bit is set.

Set bit-rate register (SCBRR_3)

[7] Setting of bit rate
  Bit rate is set to 100 kbps.

Set FIFO control register (SCFCR_3)

[8] Setting of data trigger number for the FIFO and release of the FIFO
  from the reset state
  TTRG (Transmit FIFO data trigger) is set.
  RFRST (Receive FIFO data register reset) bit is cleared to B'0.
  TFRST (Transmit FIFO data register reset) bit is cleared to B'0.

Set serial control register (SCSCR)

[9] Setting to enable transmission of data and reception of interrupt requests
  TIE (Transmit interrupt enable) bit is set to B'1, enabling interrupts.
  TE (Transmit enable) bit is set to B'1, enabling transmission of data.

Figure 7 Flow for Initialization of Data Transmission in Clock-Synchronous Mode
int_scif_txif()

Writing of data equivalent to the transmit FIFO data trigger number completed?

NO

Write the transmit data to the transmit FIFO data register (SCFTDR)

Transmission of 32-byte data completed?

YES

Disable transmit interrupts

Clear TEFE and TEND bits in the serial status register (SCFSR_3) to 0

END

Transmit interrupts are disabled after all of the data have been transmitted.

Figure 8  Flow for Handling of Transmit Interrupts in Clock-Synchronous Mode
2.4 Procedure for Processing by the Sample Program

In this sample program, character strings are transmitted after initialization of SCIF3 for data transmission in clock-synchronous mode.

2.4.1 Clock Pulse Generator (CPG)

Table 3 gives settings for the register of the clock pulse generator in the sample program.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency control register (FRQCR)</td>
<td>H'FFFE0010</td>
<td>H'0101</td>
<td>STC [2:0] = B'001: ( \times \frac{1}{2} (B\phi) )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IFC [2:0] = B'000: ( \times 1 (I\phi) )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PFC [2:0] = B'001: ( \times \frac{1}{2} (P\phi) )</td>
</tr>
</tbody>
</table>

2.4.2 Standby Control Register

Table 4 gives settings for the standby control register in the sample program.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby control register 4 (STBCR4)</td>
<td>H'FFFE040C</td>
<td>H'E6</td>
<td>MSTP44 = B'0: SCIF3 operates</td>
</tr>
</tbody>
</table>

2.4.3 Interrupt Controller (INTC)

Table 5 gives settings for the register of the interrupt controller in the sample program.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt priority register 14 (IPR14)</td>
<td>H'FFFE0C10</td>
<td>H'000F</td>
<td>IPR14 [3:0] = H'F: SCIF3 is at a level 15</td>
</tr>
</tbody>
</table>

2.4.4 Pin Function Controller (PFC)

Table 6 gives settings for the register of the pin function controller in the sample program.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port E control register L2 (PECRL2)</td>
<td>H'FFFE3A14</td>
<td>H'0550</td>
<td>PE6MD [2:0] = B'101: SCK3 input/output</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PE5MD [2:0] = B'101: TXD3 output</td>
</tr>
</tbody>
</table>
### 2.4.5 Serial Communications Interface with FIFO

Table 7 gives settings for the registers of the SCIF in the sample program.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial mode register (SCSMR)</td>
<td>H'FFFE8800</td>
<td>H'0080</td>
<td>C/A = B'1: Clock-synchronous mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CHR = B'0: 8-bit data</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PE = B'0: Disables adding and checking of parity bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>STOP = B'0: 1 stop bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CKS [1:0] = B'00: Pφ clock</td>
</tr>
<tr>
<td>Bit rate register (SCBRR)</td>
<td>H'FFFE8804</td>
<td>D'124</td>
<td>Clock-synchronous mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bit rate: 100k (bit/s) *1</td>
</tr>
<tr>
<td>Serial control register (SCSCR)</td>
<td>H'FFFE8808</td>
<td>H'0000</td>
<td>Initialization</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TIE = B'0: Disables transmit-FIFO-data-empty interrupt (TXI) request</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RIE = B'0: Disables receive-FIFO-data-full interrupt (RXI), receive-error-interrupt (ERI), and break interrupt (BRI) requests</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TE = B'0: Disables transmission of data</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RE = B'0: Disables reception of data</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>At the time of setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Clock-synchronous mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CKE [1:0] = B'00: Internal clock, SCK pin is used for synchronizing clock output</td>
</tr>
<tr>
<td></td>
<td>H'00C0</td>
<td></td>
<td>When transmitting operation is enabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TIE = B'1: Enables transmit-FIFO-data-empty interrupt (TXI) request</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TE = B'1: Enables transmission of data</td>
</tr>
<tr>
<td>Serial status register (SCFSR)</td>
<td>H'FFFE8810</td>
<td>H'0060</td>
<td>Initial value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TEND = B'1: Transmit end flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TDFE = B'1: Transmit-FIFO-data-empty flag</td>
</tr>
<tr>
<td></td>
<td>H'0000</td>
<td></td>
<td>At the time of setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>All flags are cleared to 0.</td>
</tr>
<tr>
<td>FIFO control register (SCFCR)</td>
<td>H'FFFE8818</td>
<td>H'0060</td>
<td>Initialization</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TFRST = B'1: Enables reset operation of transmitted data in the transmit-FIFO-data register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RFRST = B'1: Enables reset operation of received data in the receive-FIFO-data register</td>
</tr>
</tbody>
</table>
At the time of setting $TTRG[1:0] = B'00$: 8 (8) number of transmitted data

$TFRST = B'0$: Disables reset operation of transmitted data in the transmit-FIFO-data register

$RFRST = B'0$: Disables reset operation of received data in the receive-FIFO-data register

$LOOP = B'0$: Disables loop back test

Note: 1. For details on bit rate settings, see the table of bit rates and SCBRR settings in the section on the serial communication interface with FIFO of the **SH7280 Group Hardware Manual**.
3. Documents for Reference

- Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

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csc@renesas.com

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<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
<th>Page</th>
<th>Summary</th>
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</thead>
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<tr>
<td>1.00</td>
<td>Aug.27.08</td>
<td>—</td>
<td>—</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>

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