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April 1\textsuperscript{st}, 2010
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SH7280 Group
Transmission of Serial Data by the SCIF in Asynchronous Mode

Introduction
This application note describes transmission of serial data by using asynchronous transfer function of the serial communications interface with FIFO (SCIF). This application note is a summary for quick reference of information required in the design of user software.

Target Device
SH7285

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1. Preface.......................................................................................................................... 2
2. Description of the Sample Application......................................................................... 3
3. Documents for Reference............................................................................................. 11
1. Preface

1.1 Specifications

This sample application employs the asynchronous serial transfer function of the serial communications interface with FIFO (SCIF) to perform data transmission. Figure 1 shows an example of connection for transmission by the SCIF in asynchronous mode.

- SCIF3 is used.
- The communications format has a fixed 8-bit data length, 1 stop bit, and no parity bit.
- The transmit interrupt is used to conduct unidirectional communications via SCIF3. That is, the data-transfer controller (DTC) is activated by the transmit-FIFO-data-empty interrupt.
- Once 32 bytes of data have been transmitted, operation for transmission is halted.

![Figure 1](image.png)

**Figure 1  Connection Example for Transmission by the SCIF in Asynchronous Mode**

1.2 Module Used

Serial communications interface with FIFO (SCIF3)

1.3 Applicable Conditions

<table>
<thead>
<tr>
<th>MCU</th>
<th>SH7285</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating frequency</td>
<td>Internal clock: 100 MHz</td>
</tr>
<tr>
<td></td>
<td>Bus clock: 50 MHz</td>
</tr>
<tr>
<td></td>
<td>Peripheral clock: 50 MHz</td>
</tr>
<tr>
<td>C compiler</td>
<td>SuperH RISC engine Family C/C++ Compiler Package Ver.9.1.1 (from Renesas Technology Corp.)</td>
</tr>
</tbody>
</table>
2. Description of the Sample Application

This sample application employs the transmit-FIFO-data-empty interrupt (TXI) source of the serial communications interface with FIFO (SCIF) to transmit serial data in asynchronous mode.

2.1 Summary of MCU Module Used

In asynchronous mode, each transmitted or received character begins with a start bit and ends with a stop bit. Serial communication is synchronized in character units. The transmitting section has a 16-stage FIFO buffered structure so that data can be read or written during transmission, which enables high-speed continuous data transfer.

In asynchronous serial communications, the communication line is normally held in the mark (high) state. The SCIF monitors the line and starts serial communications when the line goes to the space (low) state, indicating a start bit.

One serial character consists of a start bit (low), data (LSB first), parity bit (high or low), and stop bit (high), in this order.

For details on the SCIF, please refer to the section on serial communications interface with FIFO in the SH7280 Group Hardware Manual (REJ09B0393).

Table 1 gives an overview of serial communications in asynchronous mode. Figure 2 shows a block diagram of the SCIF.

Table 1 Overview of Serial Data Communications in Asynchronous Mode

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of interfaces</td>
<td>1 (SCIF3)</td>
</tr>
<tr>
<td>Clock sources</td>
<td>For internal clock: Pφ, Pφ/4, Pφ/16, Pφ/64 (Pφ: peripheral clock) For external clock: input clock on the SCK3 pin</td>
</tr>
<tr>
<td>Data format</td>
<td>Transfer data length: Selectable from 7 or 8 bits Order: LSB first and MSB first are selectable</td>
</tr>
<tr>
<td>Baud rate</td>
<td>For internal clock: from 110 bps (Pφ = 50 MHz) For external clock: up to 781,250 bps (Pφ = 50 MHz, external input clock of 12.5000 MHz)</td>
</tr>
<tr>
<td>Error detection</td>
<td>Framing, parity and overrun errors</td>
</tr>
<tr>
<td>Interrupt requests</td>
<td>Transmit-FIFO-data-empty interrupt (TXI)</td>
</tr>
<tr>
<td>Clock sources</td>
<td>Internal and external clocks are selectable</td>
</tr>
<tr>
<td></td>
<td>• Internal clock When the internal clock has been selected, the SCIF operates using the clock from the baud-rate generator and a clock signal at 16 times the frequency of the bit rate can be output.</td>
</tr>
<tr>
<td></td>
<td>• External clock When the external clock has been selected, input of a clock signal at 16 times the frequency of the bit rate is required, not using the on-chip baud rate generator.</td>
</tr>
</tbody>
</table>
Figure 2   Block Diagram of the SCIF
2.2 Description of the Sample Program

Table 2 gives the settings for SCIF communications function of this sample program, and figure 3 shows the operations in data transmission.

Table 2   Settings for Communications Function of the Sample Program

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Module</td>
<td>SCIF3</td>
</tr>
<tr>
<td>Communications mode</td>
<td>Asynchronous mode</td>
</tr>
<tr>
<td>Interrupts</td>
<td>Transmit-FIFO-data-empty interrupt (TXI)</td>
</tr>
<tr>
<td>Transfer rate</td>
<td>38,400 bps</td>
</tr>
<tr>
<td>Number of data to be transmitted</td>
<td>32 bytes</td>
</tr>
<tr>
<td>Data length</td>
<td>8-bit data</td>
</tr>
<tr>
<td>Stop bit</td>
<td>1 stop bit</td>
</tr>
<tr>
<td>Parity</td>
<td>None</td>
</tr>
<tr>
<td>Bit order</td>
<td>LSB-first</td>
</tr>
<tr>
<td>FIFO data trigger number</td>
<td>Transmit FIFO data trigger: 8</td>
</tr>
</tbody>
</table>

Figure 3   Operations for Data Transmission
2.3 Procedure for Setting Module Used

This section describes the procedure for setting up SCIF3 for asynchronous mode operation.

Figure 4 shows the flow of processing by the sample program, figure 5 shows the flow of settings for release from module-standby mode, figure 6 shows the flow for initialization of data transmission in asynchronous mode, and figure 7 shows the flow for setting up the pin function controller. Furthermore, figure 8 shows the flow for handling transmit interrupts in asynchronous mode. For details on the settings of individual registers, see the *SH7280 Group Hardware Manual (REJ09B0393)*.

---

**Figure 4  Flow of Processing by the Sample Program**

1. [1] Clock is supplied to SCIF3.
2. [2] Initialization of the serial communication interface with FIFO SCIF3 is set.
3. [3] Initialization of the pin function controller
   Input and output pins of the SCIF3 are set.
4. [4] Setting of the SCIF interrupt level
   Interrupt level of the SCIF3 is set to 15.
5. [5] The transmit data empty flag is set to 0.
6. [6] The interrupt mask level is set to 0.
7. [7] Loop processing
stbc_init()  

Set standby control register 4 (STBCR4)  

[1] Enabling clock supply to SCIF3  
SCIF3: The MSTP44 bit is set to B’0.

END

---

scif_init()  

Set the serial control register (SCSCR_3)  

[1] Setting to disable transmission of data  
TE (Transmit enable) bit is set to B’0 to disable transmission of data.

Set the FIFO control register (SCFCR_3)  

[2] Initialization of data held in the FIFO queue  
TFRST (Transmit FIFO data register reset) bit is set to B’1.

Set the serial status register (SCFSR_3)  

[3] Clearing of the error status  
ER (Receive error) bit is cleared to B’0.  
BRK (Break detection) bit is cleared to B’0.  
DR (Receive data ready) bit is cleared to B’0.

Set the line status register (SCLSR_3)  

[4] Clearing of the error status  
ORER (Overrun error) bit is cleared to B’0.

Set the serial control register (SCSCR_3)  

[5] Selection of clock source and setting of clock output  
CKE (clock enable) bits are set to B’00, specifying the internal clock and input operation for the SCK pin.

Set the serial mode register (SCSMR_3)  

[6] Setting of serial communications format  
C/A (Communication mode) bit is set to B’0, specifying the asynchronous mode.  
CKS (Clock select) bits are set to B’00, specifying the internal clock source as Pφ.

Set the bit-rate register (SCBRR_3)  

[7] Setting of bit rate  
Bit rate is set to 38,400 bps.

Set the FIFO control register (SCFCR_3)  

[8] Setting of data trigger number for the FIFO and release of the FIFO from the reset state.  
TTRG (Transmit FIFO data trigger) bit is set to D’8.  
TFRST (Transmit FIFO data register reset) bit is cleared to B’0.

Set the serial control register (SCSCR_3)  

[9] Setting to enable transmission of data and reception of interrupt requests  
TIE (Transmit interrupt enable) bit is set to B’1, enabling interrupts.  
TE (Transmit enable) bit is set to B’1, enabling transmission of data.

END

---

Figure 5 Flow of Settings for Release from Module-Standby Mode

Figure 6 Flow for Initialization of Data Transmission in Asynchronous Mode
pfc_init()

Set port A control register L3 (PACRL3) [1]

END

---

[1] Setting of multiplexed pins as SCIF input and output pins
TXD3: The PA8MD[2:0] is set to B’101.

---

**Figure 7** Flow for Setting up the Pin Function Controller

---

int_scif_txf()

Yes

Writing of data equivalent to the transmit FIFO data trigger number completed?

No

Write the transmit data to the transmit FIFO data register (SCFTDR_3)

No

Specified number of transmitted data stored?

Yes

[1] Transmit interrupts are disabled after all of the data have been transmitted.

Disable transmit interrupts

END

---

**Figure 8** Flow for Handling of Transmit Interrupts in Asynchronous Mode
2.4 Procedure for Processing by the Sample Program

In this sample program, character strings are transmitted after initialization of SCIF3 in asynchronous mode.

2.4.1 Clock Pulse Generator (CPG)

Table 3 gives settings for the register of the clock pulse generator in the sample program.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency control register (FRQCR)</td>
<td>H'FFF0 0010</td>
<td>H'0101</td>
<td>STC [2:0] = B'001: × 1/2 (Bφ)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IFC [2:0] = B'000: × 1 (Iφ)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PFC [2:0] = B'001: × 1/2 (Pφ)</td>
</tr>
<tr>
<td>MTU2S clock frequency control register (MCLKCR)</td>
<td>H'FFF0 0410</td>
<td>H'41</td>
<td>MSSCS [1:0] = B'01: PLL output clock</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSDIVS [1:0] = B'01: × 1/2 (Mφ)</td>
</tr>
<tr>
<td>AD clock frequency control register (ACLKCR)</td>
<td>H'FFF0 0414</td>
<td>H'41</td>
<td>ASSCS [1:0] = B'01: PLL output clock</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ASDIVS [1:0] = B'01: × 1/2 (Aφ)</td>
</tr>
</tbody>
</table>

2.4.2 Low Power Consumption Mode

Table 4 gives settings for the standby control register in the sample program.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby control register 4 (STBCR4)</td>
<td>H'FFF0 040C</td>
<td>H'E4</td>
<td>MSTP44 = B'0: SCIF3 operates</td>
</tr>
</tbody>
</table>

2.4.3 Interrupt Controller (INTC)

Table 5 gives settings for the register of the interrupt controller in the sample program.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt priority register 14 (IPR14)</td>
<td>H'FFF0 0C10</td>
<td>H'000F</td>
<td>IPR14 [3:0] = H'F: SCIF3 is at a level 15</td>
</tr>
</tbody>
</table>

Note: The interrupt priority levels of RXI3 and TXI3 are in accord with the order of the corresponding address offsets in the vector table. For details on interrupt priority levels, see Interrupt Exception Handling Vector Table and Priority in the section on interrupt controller in the SH7280 Group Hardware Manual (REJ09B0393).
2.4.4 Pin Function Controller (PFC)

Table 6 gives settings for the register of the pin function controller in the sample program.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port A control register L3 (PACRL3)</td>
<td>H'FFFE 3812</td>
<td>H'0005</td>
<td>PA8MD [2:0] = B'101: TXD3 output</td>
</tr>
</tbody>
</table>

2.4.5 Serial Communications Interface with FIFO

Table 7 gives settings for the registers of the SCIF in the sample program.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial mode register_3 (SCSMR_3)</td>
<td>H'FFFE 9800</td>
<td>H'0000</td>
<td>C/A = B'0: Asynchronous mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CHR = B'0: 8-bit data</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PE = B'0: Disables adding and checking of parity bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>STOP = B'0: 1 stop bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CKS [1:0] = B'00: Pφ clock</td>
</tr>
<tr>
<td>Bit rate register_3 (SCBRR_3)</td>
<td>H'FFFE 9804</td>
<td>D'124</td>
<td>Asynchronous mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bit rate: 38,400 (bit/s) *1</td>
</tr>
<tr>
<td>Serial control register_3 (SCSCR_3)</td>
<td>H'FFFE 9808</td>
<td>H'0000</td>
<td>Initialization</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TIE = B'0: Enables transmit-FIFO-data-empty interrupt (TXI) request</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TE = B'0: Enables transmission of data</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>At the time of setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Asynchronous mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CKE [1:0] = B'00: Internal clock, SCK pin is used as an input pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td>H'00A0</td>
<td>When transmitting operation is enabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TIE = B'1: Enables transmit-FIFO-data-empty interrupt (TXI) request</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TE = B'1: Enables transmission of data</td>
</tr>
<tr>
<td>Serial status register_3 (SCFSR_3)</td>
<td>H'FFFE 9810</td>
<td>H'0060</td>
<td>Initialization</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TDFE = B'1: Enables transmit-FIFO-data-empty flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TEND = B'1: Enables transmit end flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td>H'0000</td>
<td>At the time of setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>All the flags are cleared</td>
</tr>
</tbody>
</table>

Note: 1. For details on bit rate settings, see the table of bit rates and SCBRR settings in the section on the serial communication interface with FIFO in the SH7280 Group Hardware Manual (REJ09B0393).
3. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual (REJ09B0051)
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- Hardware Manual
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<td>Jan. 19.09</td>
<td>—</td>
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