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__________________________

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April 1st, 2010
Renesas Electronics Corporation

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Introduction
This application note describes transmission by the I²C bus interface 3 module (IIC3) of the SH7263/SH7203 in the case of a single master on the I²C bus.

Target Device
SH7263/SH7203

Contents
1. Preface........................................................................................................................2
2. Description of the Sample Application.........................................................................3
3. Listing of the Sample Program........................................................................................12
4. Documents for Reference..............................................................................................18
1. Preface

1.1 Specifications

- In a single-master configuration with the SH7263/SH7203 as the master device and the EEPROM as the slave device, data are written to an EEPROM.
- The transfer rate is set at 397 kHz.

Note: Please adjust settings as required to match the specification of the EEPROM you are using.

1.2 Module Used

- I²C bus interface 3 (IIC3) channel 3

1.3 Applicable Conditions

- MCU: SH7263/SH7203
- Operating frequency: Internal clock 200 MHz
  Bus clock 66.67 MHz
  Peripheral clock 33.33 MHz
- C compiler: SuperH RISC engine Family C/C++ Compiler Package Ver.9.01 Release01 from Renesas Technology
- Compiler options: -cpu = sh2a -include = "$(WORKSPDIR)\inc"
  -object = "$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr = auto -chgincpath
  -errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0 -del_vacant_loop = 0
  -struct_alloc = 1 -nologo
- EEPROM: HN58X24128FPIE (128 Kbits) from Renesas Technology

1.4 Related Application Note

The operation of the sample program in this application note was confirmed with the configuration specified in the application note “Example of Initial Configuration” for the SH7263/SH7203 (REJ06B0740). Please refer to that document when setting up this sample task.
2. Description of the Sample Application

In this sample program, the SH7263/SH7203 (master device) transfers data to the EEPROM (slave device) by using I\textsuperscript{2}C bus interface 3 module (IIC3).

2.1 Operational Overview of Module Used

The I\textsuperscript{2}C bus interface 3 (IIC3) module conforms to and provides a subset of the Philips I\textsuperscript{2}C (Inter-IC) bus interface functions. However, the configuration of the registers that control the I\textsuperscript{2}C bus differs in some respects from the register configuration implemented by Philips.

The features of the I\textsuperscript{2}C bus interface 3 (IIC3) for the SH7263/SH7203 are described below.

- I\textsuperscript{2}C bus format and clock-synchronous serial format are selectable.
- Continuous transmission/reception
  - Since the shift register, transmit data register, and receive data register are independent of each other, continuous data transfer is possible.

Table 1 is a list of the features of the available formats, and figure 1 shows a block diagram of the IIC3 module.

<table>
<thead>
<tr>
<th>Format</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>I\textsuperscript{2}C bus format</td>
<td>• Start and stop conditions are generated automatically in master mode.</td>
</tr>
<tr>
<td></td>
<td>• Acknowledge output levels are selectable in data reception.</td>
</tr>
<tr>
<td></td>
<td>• Acknowledge bit is automatically loaded in data transmission.</td>
</tr>
<tr>
<td></td>
<td>• On-chip bit synchronization/wait function</td>
</tr>
<tr>
<td></td>
<td>In master mode, the state of SCL is monitored per bit, and the timing is</td>
</tr>
<tr>
<td></td>
<td>synchronized automatically. If transmission/reception is not yet</td>
</tr>
<tr>
<td></td>
<td>possible, set the SCL to low until preparations are completed.</td>
</tr>
<tr>
<td></td>
<td>• Six interrupt sources</td>
</tr>
<tr>
<td></td>
<td>1. Transmit data empty (including slave-address match)</td>
</tr>
<tr>
<td></td>
<td>2. Transmit end</td>
</tr>
<tr>
<td></td>
<td>3. Receive data full (including slave-address match)</td>
</tr>
<tr>
<td></td>
<td>4. Arbitration lost</td>
</tr>
<tr>
<td></td>
<td>5. NACK detection</td>
</tr>
<tr>
<td></td>
<td>6. Stop condition detection</td>
</tr>
<tr>
<td></td>
<td>• Data transfer by the direct memory access controller (DMAC) can be</td>
</tr>
<tr>
<td></td>
<td>activated by a transmit-data-empty or receive-data-full interrupt</td>
</tr>
<tr>
<td></td>
<td>request.</td>
</tr>
<tr>
<td></td>
<td>• Direct bus drive</td>
</tr>
<tr>
<td></td>
<td>Two pins, SCL and SDA pins, function as NMOS open-drain outputs when</td>
</tr>
<tr>
<td></td>
<td>the bus drive function is selected.</td>
</tr>
<tr>
<td>Clock-synchronous serial format</td>
<td>• Four interrupt sources</td>
</tr>
<tr>
<td></td>
<td>1. Transmit-data-empty</td>
</tr>
<tr>
<td></td>
<td>2. Transmit-end</td>
</tr>
<tr>
<td></td>
<td>3. Receive-data-full</td>
</tr>
<tr>
<td></td>
<td>4. Overrun error</td>
</tr>
<tr>
<td></td>
<td>• Data transfer by the direct memory access controller (DMAC) can be</td>
</tr>
<tr>
<td></td>
<td>activated by a transmit-data-empty or receive-data-full interrupt</td>
</tr>
<tr>
<td></td>
<td>request.</td>
</tr>
</tbody>
</table>

Note: For details on IIC3, see the section on I\textsuperscript{2}C Bus Interface 3 (IIC3) of the SH7263/SH7203 Group Hardware Manual (REJ09B0290/REJ09B0313).
Transmission by the \textsuperscript{2}C Bus Interface 3 Module in Single-Master Operation

(EEPROM Writing)

Figure 1   Overview of \textsuperscript{2}C Bus Interface 3
2.2 Procedure for Setting Module Used

This section describes the procedure for making initial settings for IIC3. The transfer rate must be set to meet the external specification. In this sample program, Pφ/84 is specified as the transfer rate. Figure 2 shows an example of the initialization sequence for IIC3. For details on the settings of individual registers, see the SH7263/SH7203 Group Hardware Manual (REJ09B0290/REJ09B0313).

![Diagram](image)

*Figure 2  Example of the Initialization Sequence for I²C Bus Interface 3*
2.3 Operation of the Sample Program

In this sample program, IIC3 is placed in master transmit mode, and transmits 10 bytes for writing to a page within the EEPROM.

The device code employed in this sample program is “B’1010”. Consult the datasheet of the EEPROM you are using for its device code.

The device address employed in this sample program is “B’000”. Consult the datasheet of the EEPROM you are using for its device address.

The memory address indicates the point where writing to the EEPROM starts. Each time a byte is written to the EEPROM, the address is incremented.

Figure 3 shows the operations for writing to a single page, and figure 4 shows the operating environment of this sample program.

![Figure 3 Page Write Operation](image)

![Figure 4 Operating Environment of the Sample Program](image)
2.4 Sequence of Processing by the Sample Program

Table 2 gives the register settings in the sample program. Table 3 shows macro definitions in the sample program. Figures 5 to 8 show the flow of processing by the sample program.

### Table 2  Register Settings Used in Sample Program

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby control register 5</td>
<td>H’FFFE 0410</td>
<td>H’00</td>
<td>MSTP54 = &quot;0&quot;: IIC3-3 operates.</td>
</tr>
<tr>
<td>( \text{I}^2\text{C} ) bus control register 1</td>
<td>H’FFFE EC00</td>
<td>H’B4</td>
<td>ICE = &quot;1&quot;: SCL and SDA pins are placed in bus-drive state. RCVD = &quot;0&quot;: Continuous reception is enabled. MST = &quot;1&quot;, TRS = &quot;1&quot;: Master transmit mode CKS = &quot;B’0100&quot;: transfer rate Pφ/84</td>
</tr>
<tr>
<td>( \text{I}^2\text{C} ) bus mode register</td>
<td>H’FFFE EC02</td>
<td>H’30</td>
<td>MLS = &quot;0&quot;: MSB-first BCWP = &quot;0&quot;: Allows the writing of values to the BC bits. BC = &quot;B’000&quot;:9 bits</td>
</tr>
</tbody>
</table>

### Table 3  Macro Definitions Used in Sample Program

<table>
<thead>
<tr>
<th>Macro Definition</th>
<th>Setting Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEPROM_MEM_ADDR</td>
<td>H’0000</td>
<td>EEPROM start address</td>
</tr>
<tr>
<td>DEVICE_CODE</td>
<td>H’A0</td>
<td>Device code</td>
</tr>
<tr>
<td>DEVICE_ADDR</td>
<td>H’00</td>
<td>Device address</td>
</tr>
<tr>
<td>IIC_DATA_WR</td>
<td>H’00</td>
<td>Write code</td>
</tr>
<tr>
<td>IIC_DATA_RD</td>
<td>H’01</td>
<td>Read code</td>
</tr>
<tr>
<td>IIC3_DATA</td>
<td>10</td>
<td>Data transfer size</td>
</tr>
</tbody>
</table>
Main (main)

START

initialize transfer source memory

IIC3 initialization
function io_iic3_init

EEPROM data writing
function io_iic3_eeprom_write

END

Note: See figure 2 "Example of the Initialization Sequence for I2C Bus Interface 3".

• The master transmit mode is selected, and data are written to EEPROM.

Figure 5  Flow of Processing by the Sample Program (1)
writing data to EEPROM  
(io_iic3_eeprom_write)

START

Place in master transmit mode

Issue the start condition

Transmit the slave device address  
function io_iic3_address_send

ACK response?  

Yes

No

Transmit data  
function io_iic3_data_send

ACK response?  

Yes

No

Transmission of specified number of bytes complete?  

No

Yes

Issue the stop condition,  
place in slave receive mode  
function io_iic3_mst_send_end

END

• 1st byte: device code, device address, write code  
• 2nd byte: memory address (higher-order byte)  
• 3rd byte: memory address (lower-order byte)

• Data transmission (10 bytes of data).

• Issue the stop condition  
• Place in slave receive mode

Figure 6  Flow of Processing by the Sample Program (2)
Transmission of the slave device address
(io_iic3_address_send)

START

Transmit Data
function io_iic3_data_send

ACK response?

No

Transmit data
function io_iic3_data_send

ACK response?

No

Transmit data
function io_iic3_data_send

ACK response?

No

return (E_ERR)

Yes

return (E_OK)

Yes

Yes

Yes

1st byte: device code, device address, write code

2nd byte: memory address (higher-order byte)

3rd byte: memory address (lower-order byte)

If no ACK response is received, return the error code.

Figure 7 Flow of Processing by the Sample Program (3)
Data transmission  
\( \text{(io\_iic3\_data\_send)} \)

START

- Transmit data register empty?  
  - Yes: Set the data to be transmitted  
  - No:  
    - Transmission complete?  
      - Yes: Confirm the ACK response after the data have been transmitted  
      - No:  
        - ACK response?  
          - Yes: IF no ACK response is received, return the error code  
          - No:  

return (E\_OK)  

Issuing a stop condition, and setting slave receive mode  
\( \text{(io\_iic3\_mst\_send\_end)} \)

START

- \( \text{I}^2\text{C} \) bus status register (ICSR\_3)  
  - TEND: Transmit end  
  - STOP: stop condition detection flag  
  - TDRE: Transmit data empty  

Clear the TEND bit to 0  
Clear the STOP bit to 0  
Issue the stop condition  

- Wait for the bus to be released after the stop condition has been issued  

Bus released?  
  - Yes: Place in slave receive mode  
  - No: Clear the TDRE bit to 0  

END

**Figure 8  Flow of Processing by the Sample Program (4)**
3. Listing of the Sample Program

1. Sample Program Listing: main.c (1)

```c
/*FILE COMMENT************************************************************
* System Name  : SH7263 Sample Program
* File Name  : main.c
* Contents : Sample program for transmission by IIC3 in master transmit mode
* Version : 1.00.00
* Model   : ROK572630D001BR
* CPU    : SH7263
* Compiler : SHC9.1.1.0
* note : Data are transmitted to EEPROM
*        by using IIC3 in master transmit mode.
* * The information described here may contain technical inaccuracies or
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* AND Renesas Solutions Corp. All Rights Reserved
* history : 2008.06.05 ver.1.00.00
*/
"FILE COMMENT END"************************************************************/
#include <machine.h>
#include "iodefine.h"    /* SH7263 iodefine */

/* ==== symbol definition ==== */
define EEPROM_MEM_ADDR 0x0000
#define DEVICE_CODE 0xA0   /* EEPROM device code :b'1010 */
define DEVICE_ADDR 0x00   /* EEPROM device address:b'000 */
define IIC_DATA_WR 0x00   /* Data write code :b'0 */
define IIC_DATA_RD 0x01   /* Data read code :b'1 */
define IIC3_DATA 10

define E_OK 0
#define E_ERR -1

/* ==== RAM allocation variable declaration ==== */
unsigned char WriteData[IIC3_DATA];

/* ==== prototype declaration ==== */
int io_iic3_eeprom_write(unsigned char d_code,unsigned char d_adr,...
void main(void);
int io_iic3_data_send(unsigned char data);
int io_iic3_mst_send_end(void);
int io_iic3_init(void);
```
2. Sample Program Listing: main.c (2)

```c
49 /*""FUNC COMMENT"***************
50 * Outline   : Sample program main
51 *---------------------------------------------------------------
52 * Include                :
53 *---------------------------------------------------------------
54 * Declaration : void main(void);
55 *---------------------------------------------------------------
56 * Function      : Sample program main
57 *---------------------------------------------------------------
58 * Argument      : void
59 *---------------------------------------------------------------
60 * Return Value : void
61 *---------------------------------------------------------------
62 * Notice        :
63 /*""FUNC COMMENT END""************************************************/  
64 void main(void)
65 {
66    int i;
67    /* ==== Prepare data to be written ==== */
68    for(i=0;i<IIC3_DATA;i++){
69        WriteData[i] = IIC3_DATA+i;
70    }
71    /* ==== IIC3 initialization setting ==== */
72    io_iic3_init();
73    /* ==== Transmission by IIC3 in master transmit mode ==== */
74    io_iic3_eeprom_write( DEVICE_CODE, /* Device code */
75        DEVICE_ADDR, /* Device address */
76        0x0000, /* Start address for data writing */
77        sizeof(WriteData), /* Amount of data to be written */
78        WriteData); /* Location for data storage */
79    while(1){
80        /* Loop */
81    }
82 }
83
```
3. Sample Program Listing: main.c (3)

```c
/* **FUNC COMMENT*********************************************************
* Outline   : IIC3 module initialization
*-----------------------------------------------------------------------
* Include   : #include "iodefine.h"
*-----------------------------------------------------------------------
* Declaration  : int io_iic3_init(void);
*-----------------------------------------------------------------------
* Function   : IIC3 module initialization
*-----------------------------------------------------------------------
* Argument    : void
*-----------------------------------------------------------------------
* Return Value : E_OK
*-----------------------------------------------------------------------
* Notice      :
*/

int io_iic3_init(void)
{
    CPG.STBCR5.BIT.MSTP54 = 0u;   /* Clear the IIC3_3 module standby mode */

    /* ---- PFC setting ---- */
    PORT.PBCRL2.BIT.PB6MD = 1u;   /* SCL3 selection */
    PORT.PBCRL2.BIT.PB7MD = 1u;   /* SDA3 selection */

    /* ----IIC31 module operation disabled ---- */
    IIC33.ICCR1.BIT.ICE = 0u;    /* IIC transfer disabled state */

    IIC33.ICCR1.BIT.RCVD = 0u;  /* Continuous reception is to proceed */
    IIC33.ICCR1.BIT.CKS = 4u;   /* Transfer rate: \( \Phi/84 \text{ (397 kHz) } \) */

    IIC33.ICCR1.BIT.CK0 = 0u;   /* Transfer rate: \( \Phi/84 \text{ (397 kHz) } \) */

    /* ----IIC bus mode register (ICMR) setting --- */
    IIC33.ICMR.BYTE = 0x30u;

    bit7 : MLS:0 --------------- MSB first
    bit6 : WAIT:0 ------------- No WAIT insertion
    bit5-4 : Reserve:1 ----------- Reserve bit
    bit3 : BCWP:0-------------- Unsetting
    bit2-0 : BC0:0, BC1:0,BC0:0------ IIC format 9-bit

    return(E_OK);
}
```
4. Sample Program Listing: main.c (4)

```c
/*""FUNC COMMENT"*******************************************************
* Outline : EEPROM data write
*-----------------------------------------------------------------------
* Include  : #include "iodefine.h"
*-----------------------------------------------------------------------
* Declaration : int io_iic3_mst_send(unsigned char d_code,
* :       unsigned char d_adr,
* :       unsigned short w_adr,
* :       unsigned int w_size,
* :       unsigned char* w_buf);
*-----------------------------------------------------------------------
* Function : The amount of data specified by "w_size"
* :       in the area specified by "w_buf" are written to the
* :       EEPROM specified by device code "d_code" and device address "d_adr".
* :       Memory addresses within the EEPROM are specified by "w_adr".
*-----------------------------------------------------------------------
* Argument : unsigned char d_code  : Device code
* :       unsigned char d_adr   : Device address
* :       unsigned short w_adr  : Address where writing is to start
* :       unsigned int w_size   : Amount of data to be written
* :       unsigned char* w_buf  : Location where data are to be written
*-----------------------------------------------------------------------
* Return Value : With ACK response  : E_OK
* :       With no ACK response  : E_ERR
*-----------------------------------------------------------------------
* Notice  :
**""FUNC COMMENT END"**************************************************/
int io_iic3_eeprom_write(unsigned char d_code,unsigned char d_adr,unsigned short w_adr,
unsigned int w_size,unsigned char* w_buf)
{
    int ack = E_OK;
    int i;
    unsigned char send[3];
    send[0] = (unsigned char)(d_code|((d_adr & 0x7)<<1)|IIC_DATA_WR);
    send[1] = (unsigned char)((w_adr>>8) & 0x00ff);
    send[2] = (unsigned char)(w_adr & 0x00ff);
    while(IIC33.ICCR2.BIT.BBSY == 1u){
        /* Waiting for bus release */
        }
    IIC33.ICCR1.BYTE |= 0x30u;    /* Set to master transmission mode */
    IIC33.ICCR2.BYTE = ((IIC33.ICCR2.BYTE & 0xbfu)|0x80u);  /* Issue the start condition */
    ack = io_iic3_address_send(send);  /* Transmit the first, second, and third bytes of data */
    if(ack == E_OK){
        /* ACK response is received from the specified device */
        for(i=0;i<w_size;i++)
            ack = io_iic3_data_send(*w_buf++);  /* Data transmission */
        if(ack == E_ERR){
            break;
        }
    }
    else{
        /* ACK response is not received from the specified device */
        io_iic3_mst_send_end();
    }
    return(ack);
}```
5. Sample Program Listing: main.c (5)

```c
/*""FUNC COMMENT"*******************************************************
* Outline   : Transmission of the slave device address
*-----------------------------------------------------------------------
* Include   :
*-----------------------------------------------------------------------
* Declaration  : int io_iic3_address_send(unsigned char* data);
*-----------------------------------------------------------------------
* Function    : Transmission of the slave device address specified by "data" (one byte)
*               : and the memory address (two bytes).
*-----------------------------------------------------------------------
* Argument    : unsigned char* data : Transmit data
*-----------------------------------------------------------------------
* Return Value : With ACK response : E_OK
*                : With no ACK response : E_ERR
*-----------------------------------------------------------------------
* Notice      :
*""FUNC COMMENT END"***************************************************/

int io_iic3_address_send(unsigned char* data)
{
    int ack;

    ack = io_iic3_data_send(*data++); /* Slave device address */
    if(ack == E_ERR)
    {
        return(ack);
    }
    ack = io_iic3_data_send(*data++); /* 1st part of memory address */
    if(ack == E_ERR)
    {
        return(ack);
    }
    ack = io_iic3_data_send(*data);    /* 2nd part of memory address */
    if(ack == E_ERR)
    {
        return(ack);
    }
    return(ack);
}

/*""FUNC COMMENT"*******************************************************
* Outline   : Transmission of one byte of data
*-----------------------------------------------------------------------
* Include   : #include "iodefine.h"
*-----------------------------------------------------------------------
* Declaration  : int io_iic3_data_send(unsigned char data);
*-----------------------------------------------------------------------
* Function    : Data are transmitted according to the following procedure.
*               : 1. Wait for ICDRT to become empty.
*               : 2. Set the data to be transmitted.
*               : 3. Check completion of data transmission.
*               : 4. Check the ACK response.
*-----------------------------------------------------------------------
* Argument    : unsigned char data : Transmit data
*-----------------------------------------------------------------------
* Return Value : With ACK response : E_OK
*                : With no ACK response : E_ERR
*-----------------------------------------------------------------------
* Notice      :
*""FUNC COMMENT END"***************************************************/
```

```c
int io_iic3_data_send(unsigned char data)
{
    int ack;

    if(ack == E_ERR)
    {
        return(ack);
    }
    if(ack == E_ERR)
    {
        return(ack);
    }
    if(ack == E_ERR)
    {
        return(ack);
    }
    return(ack);
}
```
```c
int io_iic3_data_send(unsigned char data)
{
    int ack;
    while(IIC33.ICSR.BIT.TDRE == 0u){
        /* Wait for ICDRT to become empty */
    }
    IIC33.ICDRT = data;
    while(IIC33.ICSR.BIT.TEND == 0u){
        /* Wait for completion of data transmission */
    }
    if(IIC33.ICIER.BIT.ACKBR == 0u){
        ack = E_OK;
    }
    else{
        ack = E_ERR;
    }
    return(ack);
}
```

```c
/***FUNC COMMENT********************************************************************************************************************************************
* Outline   : Issuing of a stop condition
*-----------------------------------------------------------------------
* Include   : #include "iodefine.h"
*-----------------------------------------------------------------------
* Declaration  : void io_iic3_mst_send_end(void);
*-----------------------------------------------------------------------
* Function    : A stop condition is issued and slave receive mode is set.
*-----------------------------------------------------------------------
* Argument    : void
*-----------------------------------------------------------------------
* Return Value : void
*-----------------------------------------------------------------------
* Notice      :
**"FUNC COMMENT END"******************************************************************************************************************************************/
```

```c
void io_iic3_mst_send_end(void)
{
    IIC33.ICSR.BIT.TEND = 0u;       /* Clear the TEND flag */
    IIC33.ICSR.BIT.STOP = 0u;       /* Clear the STOP flag */
    IIC33.ICCR2.BYTE &= 0x3fu;      /* Issue the stop condition */
    while(IIC33.ICSR.BIT.STOP == 0u){
        /* Wait for bus release */
    }
    IIC33.ICCR1.BYTE &= 0xcffu;     /* Slave receive mode */
    IIC33.ICSR.BIT.TDRE = 0u;      /* Clear bit TDRE */
}
/* End of File */
```
4. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual (REJ09B0051)
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manual
  SH7203 Group Hardware Manual (REJ09B0313)
  The most up-to-date version of this document is available on the Renesas Technology Website.
  SH7263 Group Hardware Manual (REJ09B0290)
  The most up-to-date version of this document is available on the Renesas Technology Website.
Website and Support

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