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SH7263/SH7203 Group

Transmission by the I²C Bus Interface 3 Module in Single-Master Operation (EEPROM Writing)

Introduction

This application note describes transmission by the I²C bus interface 3 module (IIC3) of the SH7263/SH7203 in the case of a single master on the I²C bus.

Target Device

SH7263/SH7203

Contents

1. Preface

1.1 Specifications

- In a single-master configuration with the SH7263/SH7203 as the master device and the EEPROM as a slave device, data are written to an EEPROM.
- The transfer rate is set at 397 kHz.

Note: Please adjust settings as required to match the specification of the EEPROM you are using.

1.2 Module Used

- I²C bus interface 3 (IIC3) channel 3

1.3 Applicable Conditions

- MCU: SH7263/SH7203
- Operating frequency: Internal clock 200 MHz
  Bus clock 66.67 MHz
  Peripheral clock 33.33 MHz
- C compiler: SuperH RISC engine Family C/C++ Compiler Package Ver.9.01 Release01
  from Renesas Technology
- Compiler options: -cpu = sh2a -include = "$(WORKSPDIR)\inc"
  -object = "$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr = auto -chgincpath
  -errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0 -del_vacant_loop = 0
  -struct_alloc = 1 -nologo
- EEPROM: HN58X24128FPIE (128 Kbits)
  from Renesas Technology

1.4 Related Application Note

The operation of the sample program in this application note was confirmed with the configuration specified in the application note “Example of Initial Configuration” for the SH7263/SH7203 (REJ06B0740). Please refer to that document when setting up this sample task.

2. Description of the Sample Application

In this sample program, the SH7263/SH7203 (master device) transfers data to the EEPROM (slave device) by using I²C bus interface 3 module (IIC3).

2.1 Operational Overview of Module Used

The I²C bus interface 3 (IIC3) module conforms to and provides a subset of the Philips I²C (Inter-IC) bus interface functions. However, the configuration of the registers that control the I²C bus differs in some respects from the register configuration implemented by Philips.

The features of the I²C bus interface 3 (IIC3) for the SH7263/SH7203 are described below.

- I²C bus format and clock-synchronous serial format are selectable.
- Continuous transmission/reception
  Since the shift register, transmit data register, and receive data register are independent of each other, continuous data transfer is possible.

Table 1 is a list of the features of the available formats, and figure 1 shows a block diagram of the IIC3 module.

Table 1 Features of the Formats

Format	Features
I²C bus format	• Start and stop conditions are generated automatically in master mode. • Acknowledge output levels are selectable in data reception. • Acknowledge bit is automatically loaded in data transmission • On-chip bit synchronization/wait function In master mode, the state of SCL is monitored per bit, and the timing is synchronized automatically. If transmission/reception is not yet possible, set the SCL to low until preparations are completed. • Six interrupt sources 1. Transmit data empty (including slave-address match) 2. Transmit end 3. Receive data full (including slave-address match) 4. Arbitration lost 5. NACK detection 6. Stop condition detection • Data transfer by the direct memory access controller (DMAC) can be activated by a transmit-data-empty or receive-data-full interrupt request. • Direct bus drive Two pins, SCL and SDA pins, function as NMOS open-drain outputs when the bus drive function is selected.
Clock-synchronous serial format	• Four interrupt sources 1. Transmit-data-empty 2. Transmit-end 3. Receive-data-full 4. Overrun error • Data transfer by the direct memory access controller (DMAC) can be activated by a transmit-data-empty or receive-data-full interrupt request.

Note: For details on IIC3, see the section on I²C Bus Interface 3 (IIC3) of the *SH7263/SH7203 Group Hardware Manual (REJ09B0290/REJ09B0313)*.

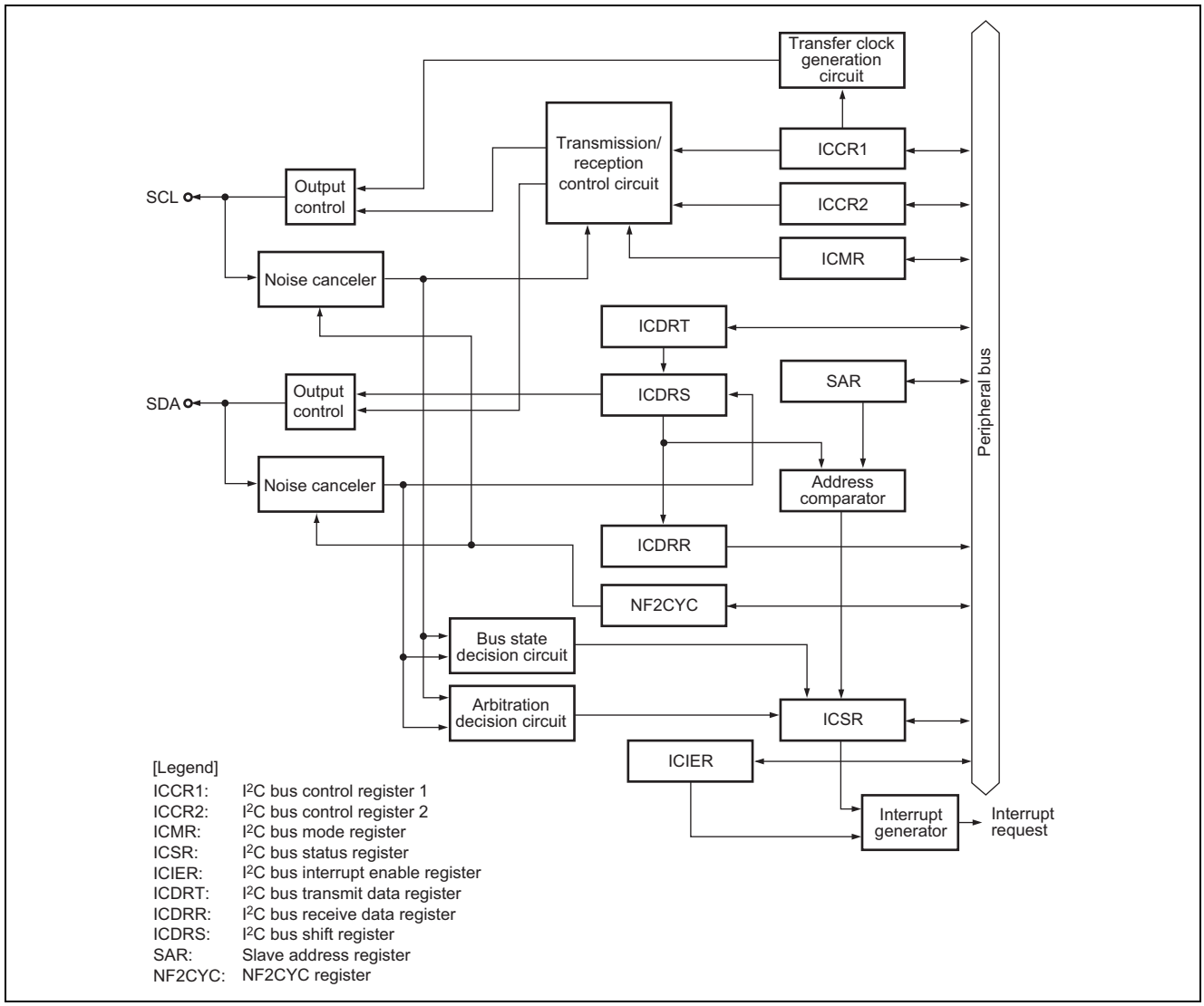

Figure 1 Overview of I²C Bus Interface 3

2.2 Procedure for Setting Module Used

This section describes the procedure for making initial settings for IIC3. The transfer rate must be set to meet the external specification. In this sample program, Pϕ/84 is specified as the transfer rate. Figure 2 shows an example of the initialization sequence for IIC3. For details on the settings of individual registers, see the *SH7263/SH7203 Group Hardware Manual (REJ09B0290/REJ09B0313).*

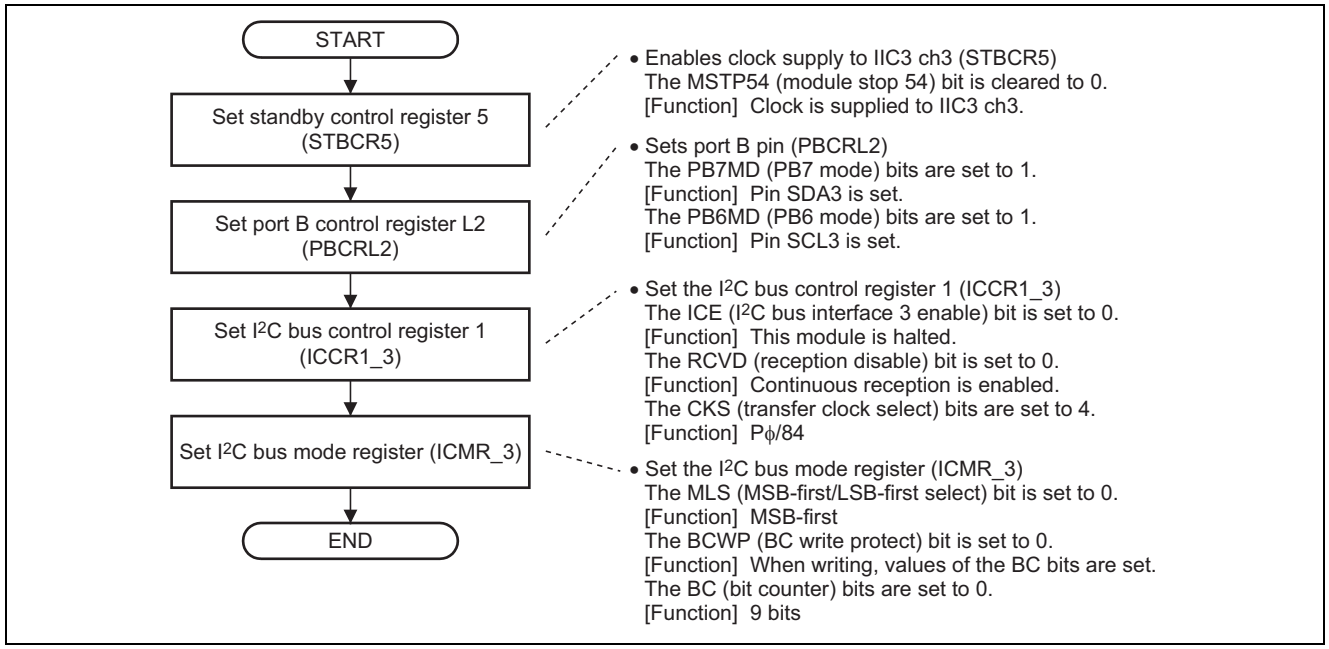

Figure 2 Example of the Initialization Sequence for I²C Bus Interface 3

2.3 Operation of the Sample Program

In this sample program, IIC3 is placed in master transmit mode, and transmits 10 bytes for writing to a page within the EEPROM.

The device code employed in this sample program is “B’1010”. Consult the datasheet of the EEPROM you are using for its device code.

The device address employed in this sample program is “B’000”. Consult the datasheet of the EEPROM you are using for its device address.

The memory address indicates the point where writing to the EEPROM starts. Each time a byte is written to the EEPROM, the address is incremented.

Figure 3 shows the operations for writing to a single page, and figure 4 shows the operating environment of this sample program.

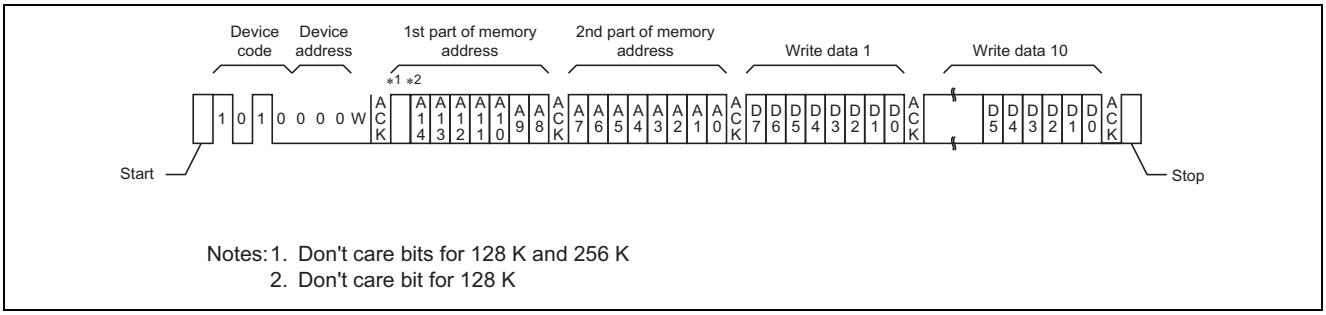

Figure 3 Page Write Operation

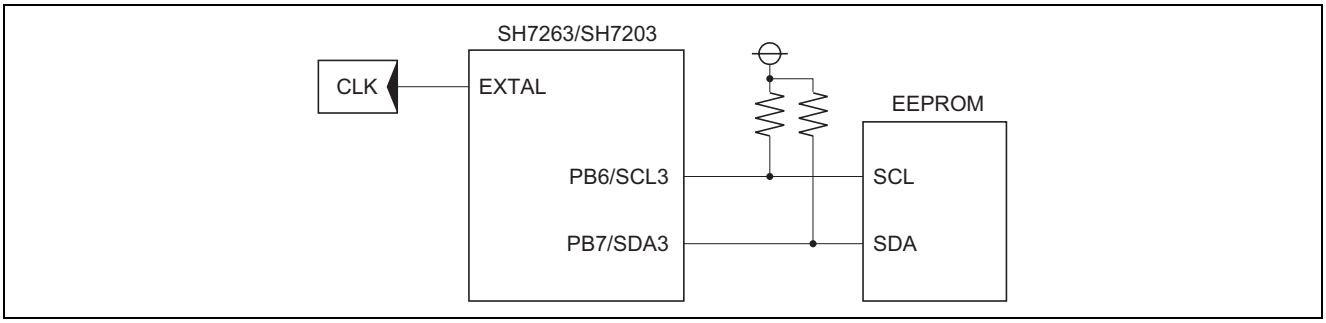

Figure 4 Operating Environment of the Sample Program

2.4 Sequence of Processing by the Sample Program

Table 2 gives the register settings in the sample program. Table 3 shows macro definitions in the sample program. Figures 5 to 8 show the flow of processing by the sample program.

Table 2 Register Settings Used in Sample Program

Register Name	Address	Setting Value	Description
Standby control register 5 (STBCR5)	H'FFFE 0410	H'00	MSTP54 = "0": IIC3-3 operates.
I²C bus control register 1 (ICCR1_3)	H'FFFE EC00	H'B4	ICE = "1": SCL and SDA pins are placed in bus-drive state. RCVD = "0": Continuous reception is enabled. MST = "1", TRS = "1": Master transmit mode CKS = "B'0100": transfer rate Pϕ/84
I²C bus mode register (ICMR_3)	H'FFFE EC02	H'30	MLS = "0": MSB-first BCWP = "0": Allows the writing of values to the BC bits. BC = "B'000":9 bits

Table 3 Macro Definitions Used in Sample Program

Macro Definition	Setting Value	Description
EEPROM_MEM_ADDR	H'0000	EEPROM start address
DEVICE_CODE	H'A0	Device code
DEVICE_ADDR	H'00	Device address
IIC_DATA_WR	H'00	Write code
IIC_DATA_RD	H'01	Read code
IIC3_DATA	10	Data transfer size

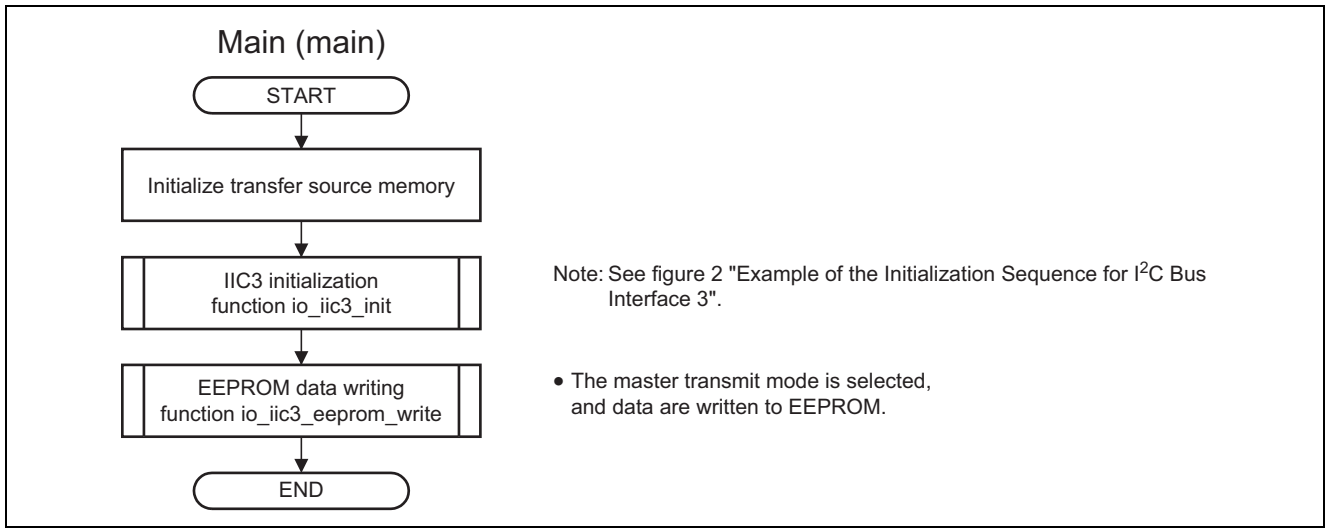

Figure 5 Flow of Processing by the Sample Program (1)

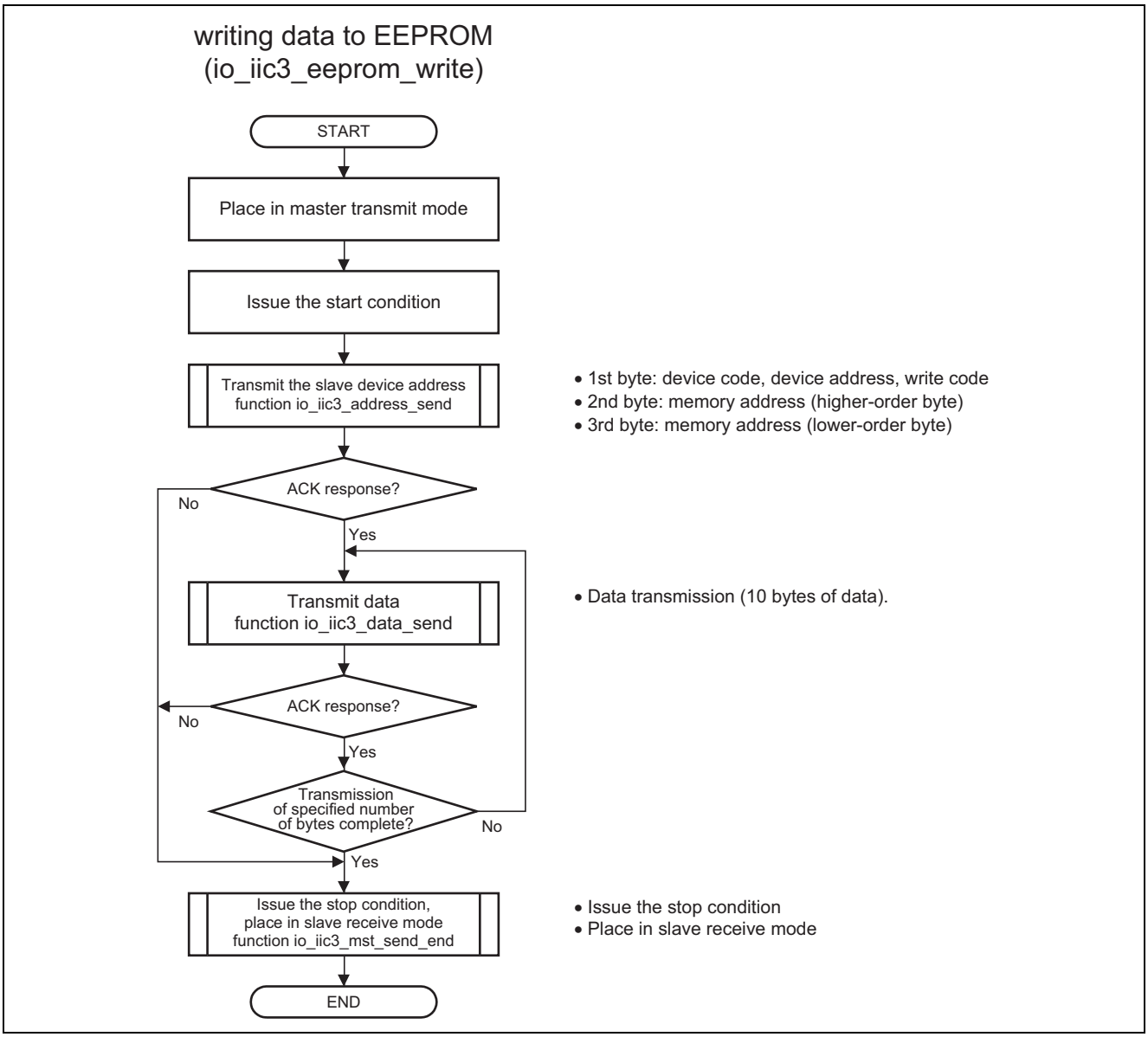

Figure 6 Flow of Processing by the Sample Program (2)

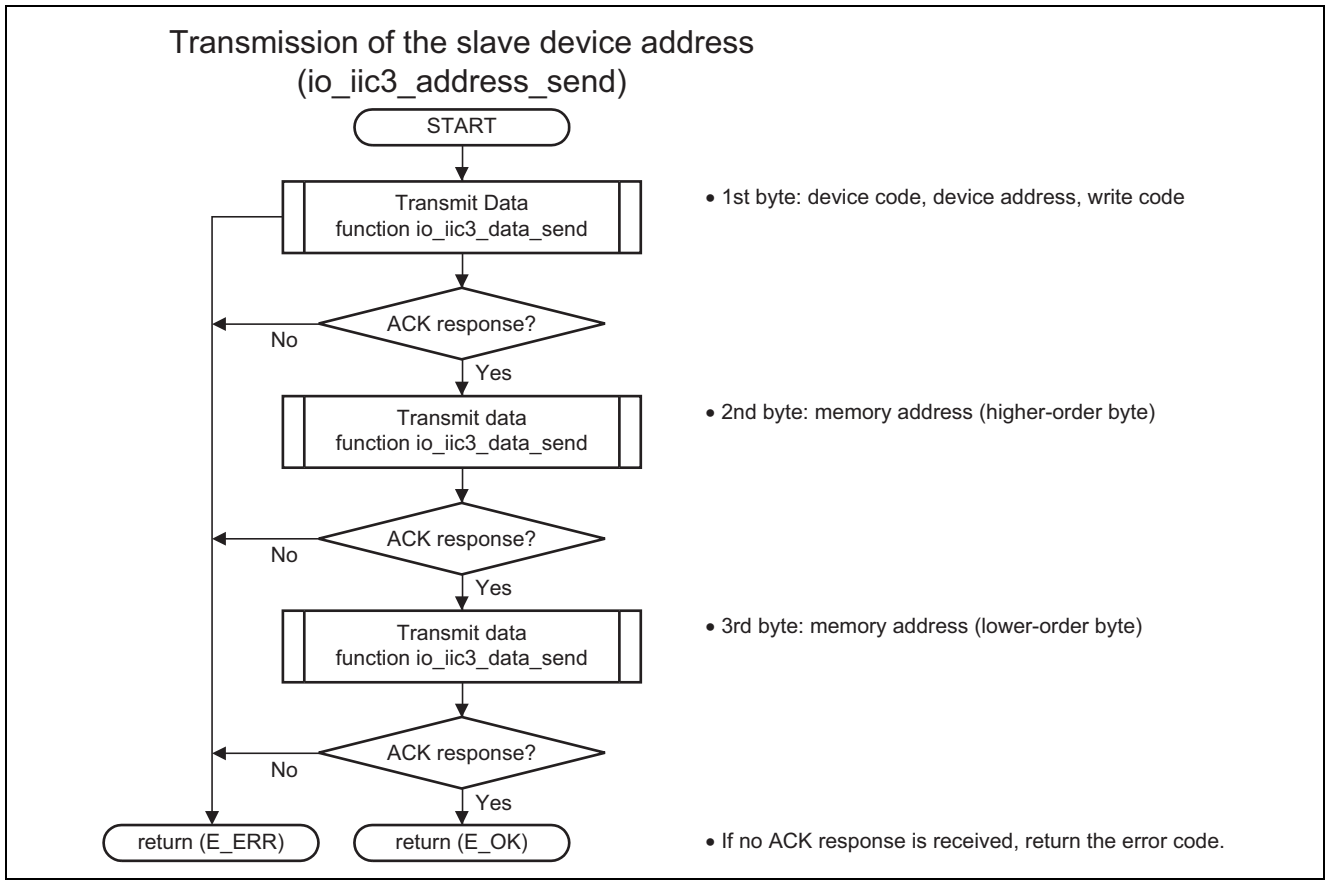

Figure 7 Flow of Processing by the Sample Program (3)

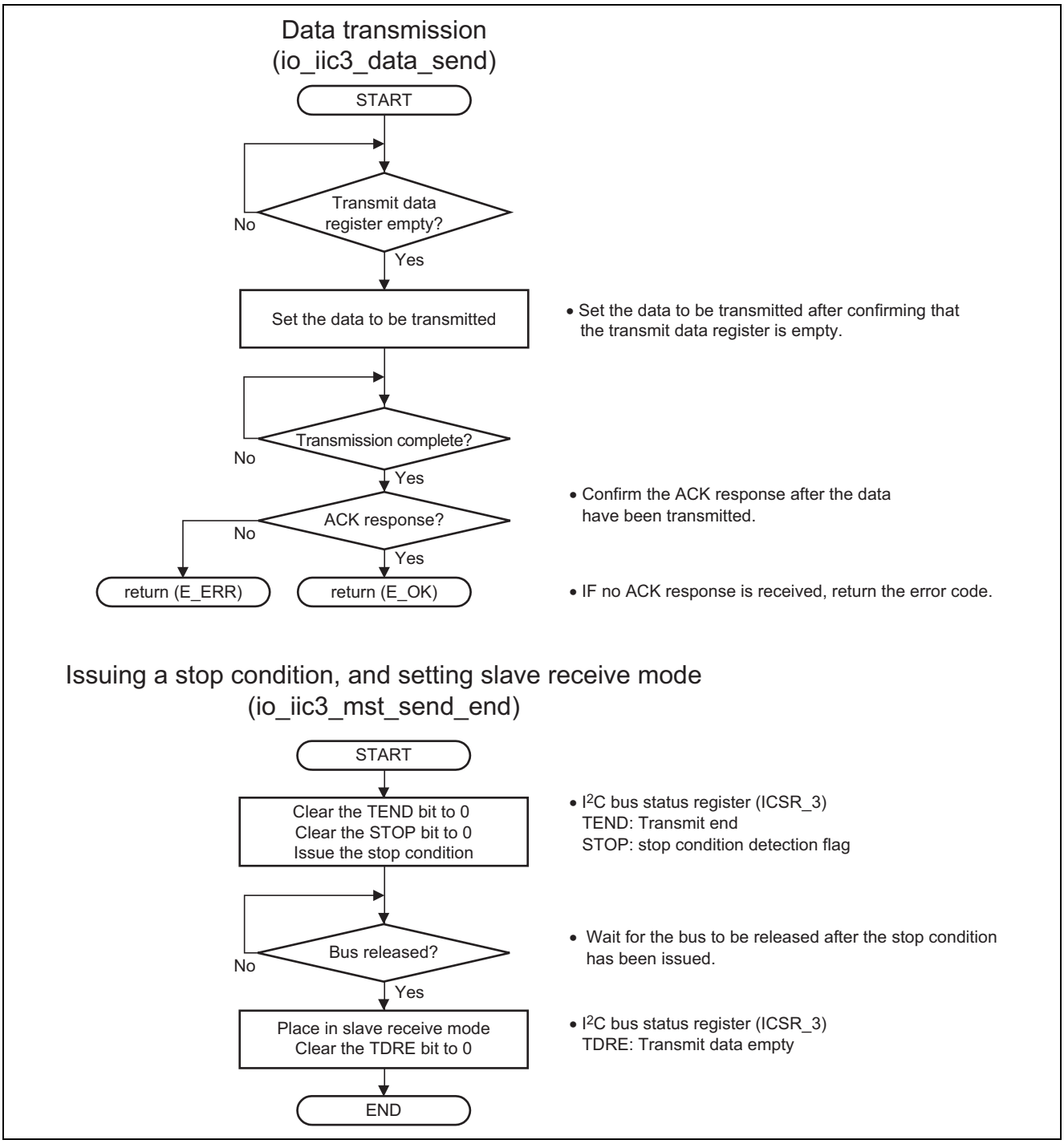

Figure 8 Flow of Processing by the Sample Program (4)

3. Listing of the Sample Program

1. Sample Program Listing: main.c (1)

```
/*""FILE COMMENT""*****************************************************************
*
* System Name  : SH7263 Sample Program
* File Name    : main.c
* Contents     : Sample program for transmission by IIC3 in master transmit mode
* Version      : 1.00.00
* Model        : R0K572630D001BR
* CPU          : SH7263
* Compiler     : SHC9.1.1.0
* note         : Data are transmitted to EEPROM
*                by using IIC3 in master transmit mode.
*
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*
* history : 2008.06.05 ver.1.00.00
*""FILE COMMENT END""*************************************************************/
#include <machine.h>
#include "iodefine.h"         /* SH7263 iodefine */

/* ==== symbol definition ==== */
#define EEPROM_MEM_ADDR 0x0000
#define DEVICE_CODE 0xA0      /* EEPROM device code :b'1010     */
#define DEVICE_ADDR 0x00      /* EEPROM device address:b'000    */
#define IIC_DATA_WR 0x00      /* Data write code :b'0           */
#define IIC_DATA_RD 0x01      /* Data read code :b'1            */
#define IIC3_DATA 10

#define E_OK 0
#define E_ERR -1

/* ==== RAM allocation variable declaration ==== */
unsigned char WriteData[IIC3_DATA];

/* ==== prototype declaration ==== */
void main(void);
int io_iic3_eeprom_write(unsigned char d_code,unsigned char d_adr,
                         unsigned short w_adr,unsigned int w_size,unsigned char* w_buf);
int io_iic3_data_send(unsigned char data);
int io_iic3_address_send(unsigned char* data);
void io_iic3_mst_send_end(void);
int io_iic3_init(void);

```

2. Sample Program Listing: main.c (2)

```
49    /*""FUNC COMMENT""*****************************************************
50    * Outline      : Sample program main
51    *-------------------------------------------------------------------------
52    * Include      :
53    *-------------------------------------------------------------------------
54    * Declaration  : void main(void);
55    *-------------------------------------------------------------------------
56    * Function     : Sample program main
57    *-------------------------------------------------------------------------
58    * Argument     : void
59    *-------------------------------------------------------------------------
60    * Return Value : void
61    *-------------------------------------------------------------------------
62    * Notice       :
63    *""FUNC COMMENT END""*************************************************/
64    void main(void)
65    {
66        int i;
67        /* ==== Prepare data to be written ==== */
68        for(i=0;i<IIC3_DATA;i++){
69        WriteData[i] = IIC3_DATA+i;
70        }
71        /* ==== IIC3 initialization setting ==== */
72        io_iic3_init();
73        /* ==== Transmission by IIC3 in master transmit mode ==== */
74        io_iic3_eeprom_write(  DEVICE_CODE,          /* Device code */
75                               DEVICE_ADDR,          /* Device address */
76                               0x0000,               /* Start address for data writing */
77                               sizeof(WriteData),    /* Amount of data to be written */
78                               WriteData);           /* Location for data storage */
79        while(1){
80               /* Loop */
81        }
82    }
83
```

3. Sample Program Listing: main.c (3)

```
 84    /*""FUNC COMMENT""*****************************************************
 85    * Outline      : IIC3 module initialization
 86    *-------------------------------------------------------------------------
 87    * Include      : #include "iodefine.h"
 88    *-------------------------------------------------------------------------
 89    * Declaration  : int io_iic3_init(void);
 90    *-------------------------------------------------------------------------
 91    * Function     : IIC3 module initialization
 92    *-------------------------------------------------------------------------
 93    * Argument     : void
 94    *-------------------------------------------------------------------------
 95    * Return Value : E_OK
 96    *-------------------------------------------------------------------------
 97    * Notice       :
 98    *""FUNC COMMENT END""*************************************************/
 99    int io_iic3_init(void)
100    {
101        CPG.STBCR5.BIT.MSTP54 = 0u;       /* Clear the IIC3_3 module standby mode */
102
103        /* ---- PFC setting ---- */
104        PORT.PBCRL2.BIT.PB6MD = 1u;       /* SCL3 selection */
105        PORT.PBCRL2.BIT.PB7MD = 1u;       /* SDA3 selection */
106        /* ----IIC31 module operation disabled ---- */
107        IIC33.ICCR1.BIT.ICE = 0u;     /* IIC transfer disabled state */
108        IIC33.ICCR1.BIT.ICE = 1u;     /* IIC3 module operation is enabled */
109        IIC33.ICCR1.BIT.RCVD = 0u;    /* Continuous reception is to proceed */
110        IIC33.ICCR1.BIT.CKS = 4u;     /* Transfer rate: Pϕ/84(397 kHz) */
111        /* ---IIC bus mode register (ICMR) setting --- */
112        IIC33.ICMR.BYTE = 0x30u;
113                                /*
114                                        bit7    : MLS:0 ------------------- MSB first
115                                        bit6    : WAIT:0 ------------------ No WAIT insertion
116                                        bit5-4  : Reserve:1 --------------- Reserve bit
117                                        bit3    : BCWP:0------------------- Unsetting
118                                        bit2-0  : BC0:0, BC1:0,BC0:0------- IIC format 9-bit
119                                */
120
121        return(E_OK);
122    }
123
```

4. Sample Program Listing: main.c (4)

```
124    /*""FUNC COMMENT""*****************************************************
125    * Outline      : EEPROM data write
126    *-------------------------------------------------------------------------
127    * Include      : #include "iodefine.h"
128    *-------------------------------------------------------------------------
129    * Declaration  : int io_iic3_mst_send(unsigned char d_code,
130    *              :                      unsigned char d_adr,
131    *              :                      unsigned short w_adr,
132    *              :                      unsigned int w_size,
133    *              :                      unsigned char* w_buf);
134    *-------------------------------------------------------------------------
135    * Function     : The amount of data specified by “w_size”
136    *              : in the area specified by “w_buf” are written to the
137    *              : EEPROM specified by device code “d_code” and device address “d_adr”.
138    *              : Memory addresses within the EEPROM are specified by “w_adr”.
139    *-------------------------------------------------------------------------
140    * Argument     : unsigned char d_code    : Device code
141    *              : unsigned char d_adr     : Device address
142    *              : unsigned short w_adr    : Address where writing is to start
143    *              : unsigned int w_size     : Amount of data to be written
144    *              : unsigned char* w_buf    : Location where data are to be written
145    *-------------------------------------------------------------------------
146    * Return Value : With ACK response       : E_OK
147    *              : With no ACK response    : E_ERR
148    *-------------------------------------------------------------------------
149    * Notice       :
150    *""FUNC COMMENT END""*************************************************/
151    int io_iic3_eeprom_write(unsigned char d_code,unsigned char d_adr,unsigned short w_adr,
152                             unsigned int w_size,unsigned char* w_buf)
153    {
154        int ack = E_OK;
155        int i;
156        unsigned char send[3];
157
158        send[0] = (unsigned char)(d_code|((d_adr & 0x7)<<1)|IIC_DATA_WR);
159        send[1] = (unsigned char)((w_adr>>8) & 0x00ff);
160        send[2] = (unsigned char)(w_adr & 0x00ff);
161
162        while(IIC33.ICCR2.BIT.BBSY == 1u){
163               /* Waiting for bus release */
164        }
165        IIC33.ICCR1.BYTE |= 0x30u;                          /* Set to master transmission mode */
166        IIC33.ICCR2.BYTE = ((IIC33.ICCR2.BYTE & 0xbfu)|0x80u);  /* Issue the start condition */
167
168        ack = io_iic3_address_send(send);     /* Transmit the first, second, and third bytes of data */
169
170        if(ack == E_OK){
171               /* ACK response is received from the specified device */
172               for(i=0;i<w_size;i++){
173                      ack = io_iic3_data_send(*w_buf++);    /* Data transmission */
174                      if(ack == E_ERR){
175                                 break;
176                      }
177               }
178               io_iic3_mst_send_end();
179        }
180        else{
181               /* ACK response is not received from the specified device */
182               io_iic3_mst_send_end();
183        }
184        return(ack);
185    }
186
```

5. Sample Program Listing: main.c (5)

```
187    /*""FUNC COMMENT""*************************************************************
188    * Outline      : Transmission of the slave device address
189    *-----------------------------------------------------------------------------
190    * Include      :
191    *-----------------------------------------------------------------------------
192    * Declaration  : int io_iic3_address_send(unsigned char* data);
193    *-----------------------------------------------------------------------------
194    * Function     : Transmission of the slave device address specified by “data” (one byte)
195    *              : and the memory address (two bytes).
196    *-----------------------------------------------------------------------------
197    * Argument     : unsigned char* data : Transmit data
198    *-----------------------------------------------------------------------------
199    * Return Value : With ACK response    : E_OK
200    *              : With no ACK response : E_ERR
201    *-----------------------------------------------------------------------------
202    * Notice       :
203    *""FUNC COMMENT END""*********************************************************/
204    int io_iic3_address_send(unsigned char* data)
205    {
206        int ack;
207
208        ack = io_iic3_data_send(*data++);         /* Slave device address */
209        if(ack == E_ERR){
210                   return(ack);
211        }
212        ack = io_iic3_data_send(*data++);         /* 1st part of memory address */
213        if(ack == E_ERR){
214                   return(ack);
215        }
216        ack = io_iic3_data_send(*data);           /* 2nd part of memory address */
217        if(ack == E_ERR){
218                   return(ack);
219        }
220        return(ack);
221    }
222    /*""FUNC COMMENT""*************************************************************
223    * Outline      : Transmission of one byte of data
224    *-----------------------------------------------------------------------------
225    * Include      : #include "iodefine.h"
226    *-----------------------------------------------------------------------------
227    * Declaration  : int io_iic3_data_send(unsigned char data);
228    *-----------------------------------------------------------------------------
229    * Function     : Data are transmitted according to the following procedure.
230    *              : 1. Wait for ICDRT to become empty.
231    *              : 2. Set the data to be transmitted.
232    *              : 3. Check completion of data transmission.
233    *              : 4. Check the ACK response.
234    *-----------------------------------------------------------------------------
235    * Argument     : unsigned char data : Transmit data
236    *-----------------------------------------------------------------------------
237    * Return Value : With ACK response    : E_OK
238    *              : With no ACK response : E_ERR
239    *-----------------------------------------------------------------------------
240    * Notice       :
241    *""FUNC COMMENT END""*********************************************************/
```

6. Sample Program Listing: main.c (6)

```
242    int io_iic3_data_send(unsigned char data)
243    {
244        int ack;
245
246        while(IIC33.ICSR.BIT.TDRE == 0u){
247                    /* Wait for ICDRT to become empty */
248        }
249        IIC33.ICDRT = data;
250        while(IIC33.ICSR.BIT.TEND == 0u){
251                    /* Wait for completion of data transmission */
252        }
253        if(IIC33.ICIER.BIT.ACKBR == 0u){
254        ack = E_OK;
255        }
256        else{
257                    ack = E_ERR;
258        }
259        return(ack);
260    }
261    /*""FUNC COMMENT""*****************************************************
262    * Outline      : Issuing of a stop condition
263    *---------------------------------------------------------------------
264    * Include      : #include "iodefine.h"
265    *---------------------------------------------------------------------
266    * Declaration  : void io_iic3_mst_send_end(void);
267    *---------------------------------------------------------------------
268    * Function     : A stop condition is issued and slave receive mode is set.
269    *---------------------------------------------------------------------
270    * Argument     : void
271    *---------------------------------------------------------------------
272    * Return Value : void
273    *---------------------------------------------------------------------
274    * Notice       :
275    *""FUNC COMMENT END""*************************************************/
276    void io_iic3_mst_send_end(void)
277    {
278        IIC33.ICSR.BIT.TEND = 0u;         /* Clear the TEND flag */
279        IIC33.ICSR.BIT.STOP = 0u;         /* Clear the STOP flag */
280        IIC33.ICCR2.BYTE &= 0x3fu;        /* Issue the stop condition */
281
282        while(IIC33.ICSR.BIT.STOP == 0u){
283                    /* Wait for bus release */
284        }
285
286        IIC33.ICCR1.BYTE &= 0xcfu;        /* Slave receive mode */
287        IIC33.ICSR.BIT.TDRE = 0u;         /* Clear bit TDRE */
288    }
289    /* End of File */
```

4. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual (REJ09B0051)
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manual
  SH7203 Group Hardware Manual (REJ09B0313)
  The most up-to-date version of this document is available on the Renesas Technology Website.
  SH7263 Group Hardware Manual (REJ09B0290)
  The most up-to-date version of this document is available on the Renesas Technology Website.

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