
SH7216 Group

REJ06B0904-0101

Rev.1.01

Transmission by the I²C Bus Interface 3 Module in Master Operation

Jun 25, 2010

Introduction

This application note describes transmission by the I²C bus interface 3 module (IIC3) of the SH7216 in the case of a single master on the I²C bus.

Target Device

SH7216

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1. Preface

1.1 Specifications

- Data are transferred from a master transmitter to a slave receiver, with SH7216 MCUs serving as both master and slave devices.
- The transfer rate is set at 403 kHz.

Note: Two SH7216 CPU boards (R0K572167) are used to run this sample program, and code included in the SH7216 Application Note *Reception by the I²C Bus Interface 3 Module in Slave Operation* (REJ06B0905) is used for the slave receiver software.

1.2 Module Used

- I²C bus interface 3 (IIC3)
- Clock pulse generator (CPG)
- Power-Down Modes
- Pin function controller (PFC)

1.3 Applicable Conditions

- MCU SH7216
- Operating frequency Internal clock: 200 MHz
Bus clock: 100 MHz
Peripheral clock: 50 MHz
- Integrated development environment High-performance Embedded Workshop Ver.4.05.01
(from Renesas Electronics Corp.)
- C compiler SuperH RISC Engine Family C/C++ Compiler Package Ver.9.03.00 Release01
from Renesas Electronics
- Compiler options Default settings of the High-performance Embedded Workshop
(-cpu=sh2afpu -pic=1 -object="\$(CONFIGDIR)¥\$(FILELEAF).obj"
-debug -gbr=auto -chgincpath -errorpath -global_volatile=0
-opt_range=all -infinite_loop=0 -del_vacant_loop=0
-struct_alloc=1 -nologo)
- Slave receive module SH7216 CPU board (R0K572167)

1.4 Related Application Note

- SH7216 Group Application Note: Reception by the I²C Bus Interface 3 Module in Slave Operation (REJ06B0905)

SH7216 Group Transmission by the I²C Bus Interface 3 Module in Master Operation

2. Overview

In this sample program, the SH7216 (master device) transfers data to the SH7216 (slave device) by using I²C bus interface 3 (IIC3) module.

2.1 Operational Overview of Module Used

The I²C bus interface 3 (IIC3) module conforms to and provides a subset of the Philips I²C (Inter-IC) bus interface functions. However, the configuration of the registers that control the I²C bus differs in some respects from the register configuration implemented by Philips.

The features of the SH7216's I²C bus interface 3 (IIC3) are described below.

- I²C bus format and clock-synchronous serial format are selectable.
- Continuous transmission/reception
Since the shift register, transmit data register, and receive data register are independent of each other, continuous data transfer is possible.

Table 1 is a list of the features of the available formats, and figure 1 shows a block diagram of the IIC3 module.

Table 1 Features of the Formats

Format	Features
I ² C bus format	<ul style="list-style-type: none">• Start and stop conditions are generated automatically in master mode.• Acknowledge output levels are selectable in data reception.• Acknowledge bit is automatically loaded in data transmission• On-chip bit synchronization/wait function In master mode, the state of SCL is monitored per bit, and the timing is synchronized automatically. If transmission/reception is not yet possible, set the SCL to low until preparations are completed.• Six interrupt sources<ol style="list-style-type: none">1. Transmit data empty (including slave-address match)2. Transmit end3. Receive data full (including slave-address match)4. Arbitration lost5. NACK detection6. Stop condition detection• Data transfer by the direct memory access controller (DMAC) can be activated by a transmit-data-empty or receive-data-full interrupt request.• Direct bus drive Two pins, SCL and SDA pins, function as NMOS open-drain outputs when the bus drive function is selected.
Clock-synchronous serial format	<ul style="list-style-type: none">• Four interrupt sources<ol style="list-style-type: none">1. Transmit-data-empty2. Transmit-end3. Receive-data-full4. Overrun error• Data transfer by the direct memory access controller (DMAC) can be activated by a transmit-data-empty or receive-data-full interrupt request.

Note: For details on IIC3, see the section on I²C Bus Interface 3 (IIC3) of the *SH7216 Group Hardware Manual (REJ09B0543)*.

SH7216 Group Transmission by the I²C Bus Interface 3 Module in Master Operation

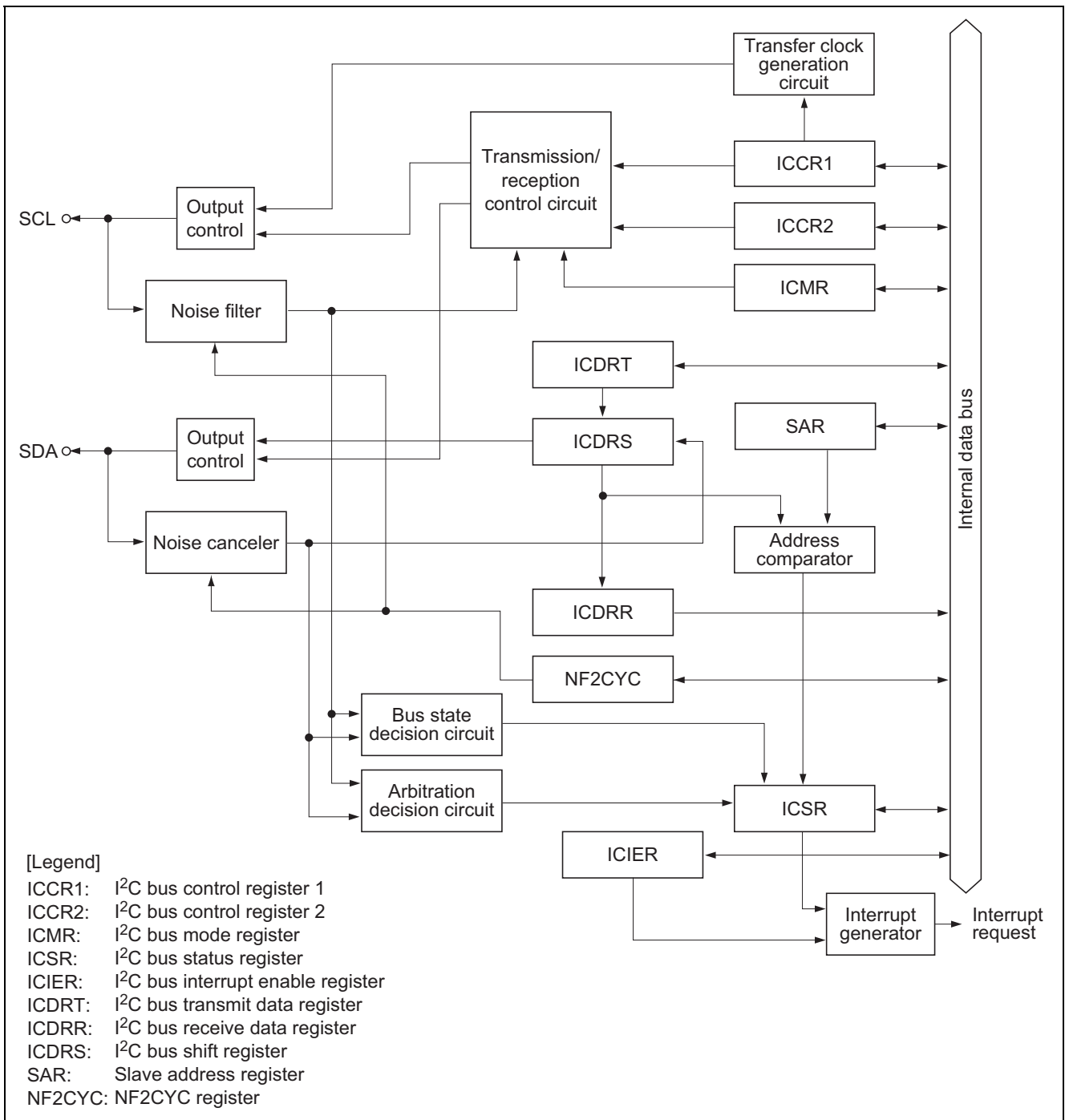


Figure 1 Overview of I²C Bus Interface 3

2.2 Procedure for Setting Module Used

This section describes the procedure for making initial settings for IIC3. The transfer rate must be set to meet the external specification. In this sample program, P ϕ /124 is specified as the transfer rate. Figure 2 shows an example of the initialization sequence for IIC3. For details on the settings of individual registers, see the *SH7216 Group Hardware Manual (REJ09B0543)*.

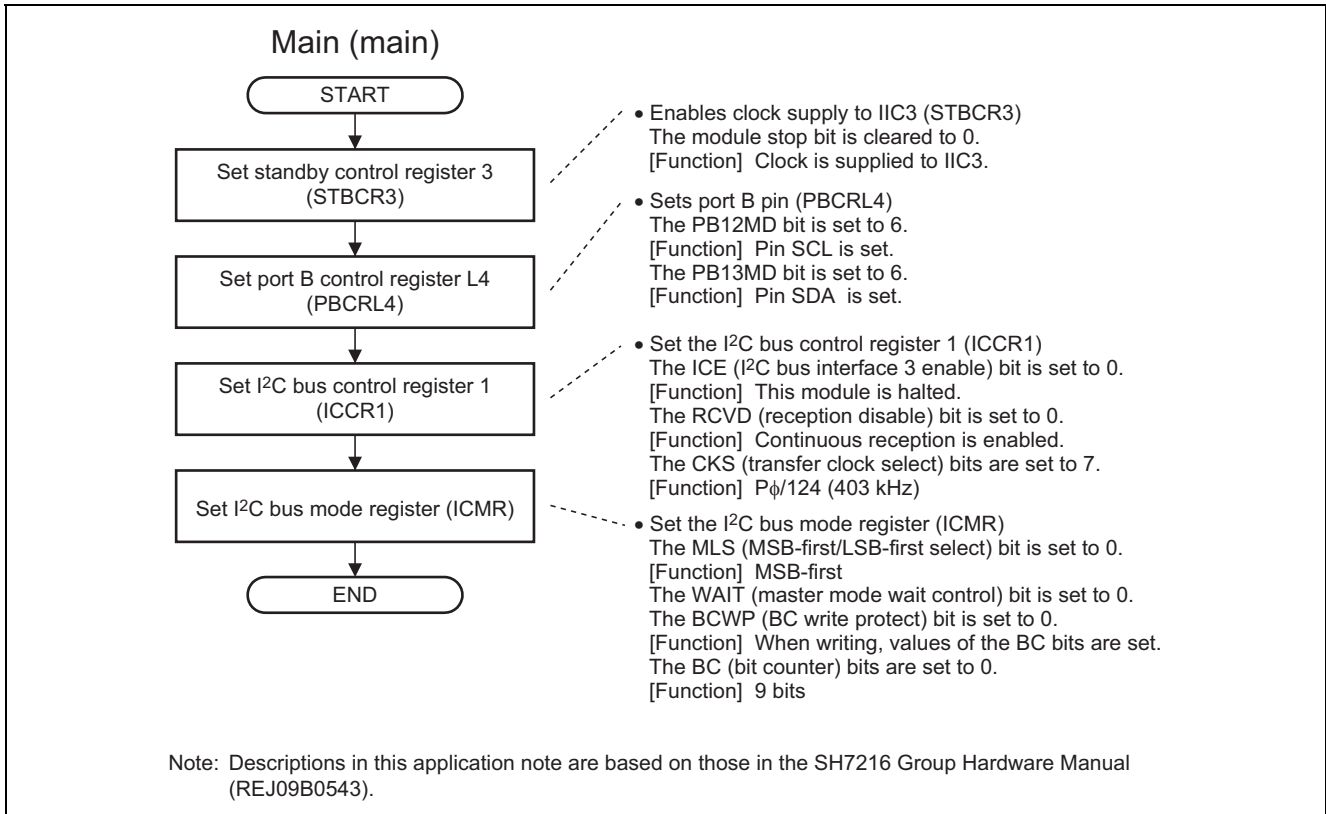


Figure 2 Example of the Initialization Sequence for I²C Bus Interface 3

SH7216 Group Transmission by the I²C Bus Interface 3 Module in Master Operation

2.3 Operation of the Sample Program

In this sample program, IIC3 is placed in master transmit mode, and transmits 10 bytes for writing to a page within the SH7216.

The device code b'1010 and the device address b'000 are used.

Figure 3 shows the operations for writing to a single page, and figure 4 shows the operating environment of this sample program.

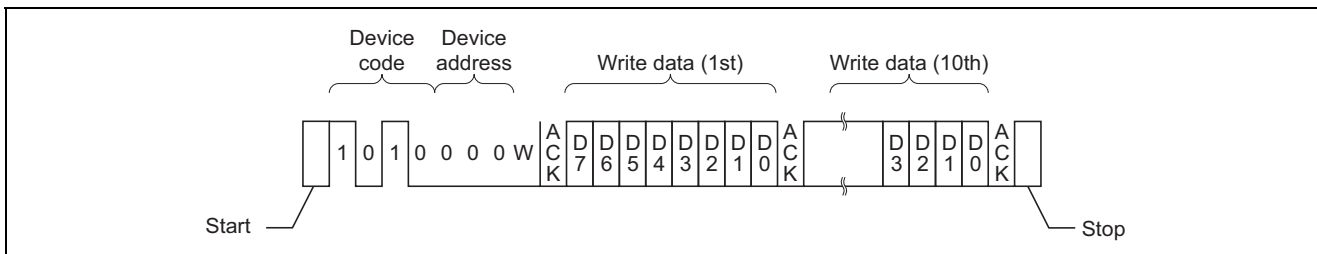


Figure 3 Page Write Operation

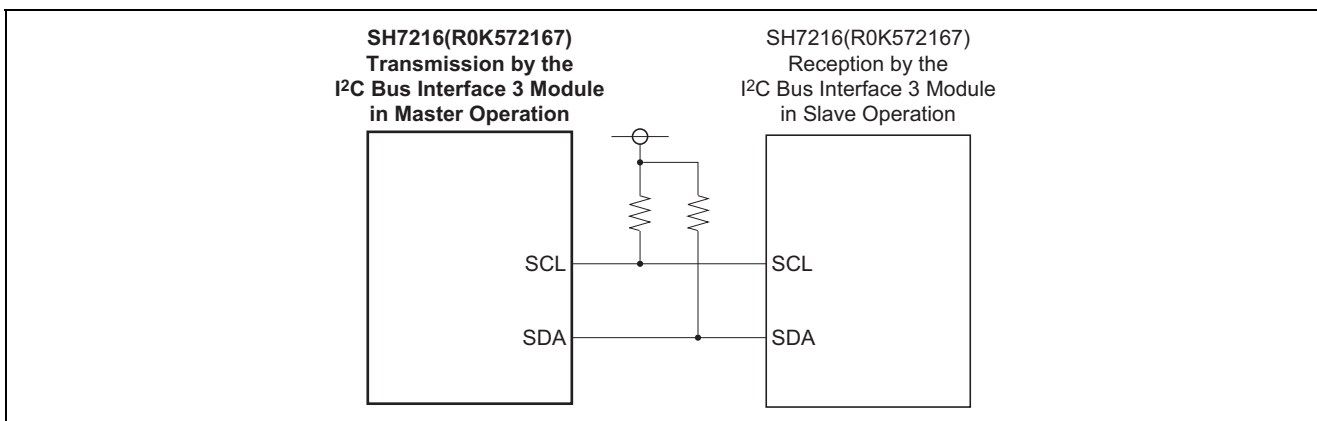


Figure 4 Operating Environment of the Sample Program

SH7216 Group Transmission by the I²C Bus Interface 3 Module in Master Operation

2.4 Sequence of Processing by the Sample Program

Table 2 gives the register settings in the sample program. Table 3 shows macro definitions in the sample program. Figures 5 to 8 show the flow of processing by the sample program.

Table 2 Register Settings Used in Sample Program

Register Name	Address	Setting Value	Description
Standby control register 3 (STBCR3)	H'FFFE0408	H'00	MSTP33 = "0": IIC3 operates.
I ² C bus control register 1 (ICCR1)	H'FFFEE000	H'B7	ICE = "1": SCL and SDA pins are placed in bus-drive state. RCVD = "0": Continuous reception is enabled. MST = "1", TRS = "1": Master transmit mode CKS = "B'0111": transfer rate P _φ /124
I ² C bus mode register (ICMR)	H'FFFEE002	H'30	MLS = "0": MSB-first BCWP = "0": Allows the writing of values to the BC bits. BC = "B'000": 9 bits

Table 3 Macro Definitions Used in Sample Program

Macro Definition	Setting Value	Description
DEVICE_CODE	H'A0	Device code
DEVICE_ADDR	H'00	Device address
IIC_DATA_WR	H'00	Write code
IIC_DATA_RD	H'01	Read code
IIC3_DATA	10	Data transfer size

SH7216 Group Transmission by the I²C Bus Interface 3 Module in Master Operation

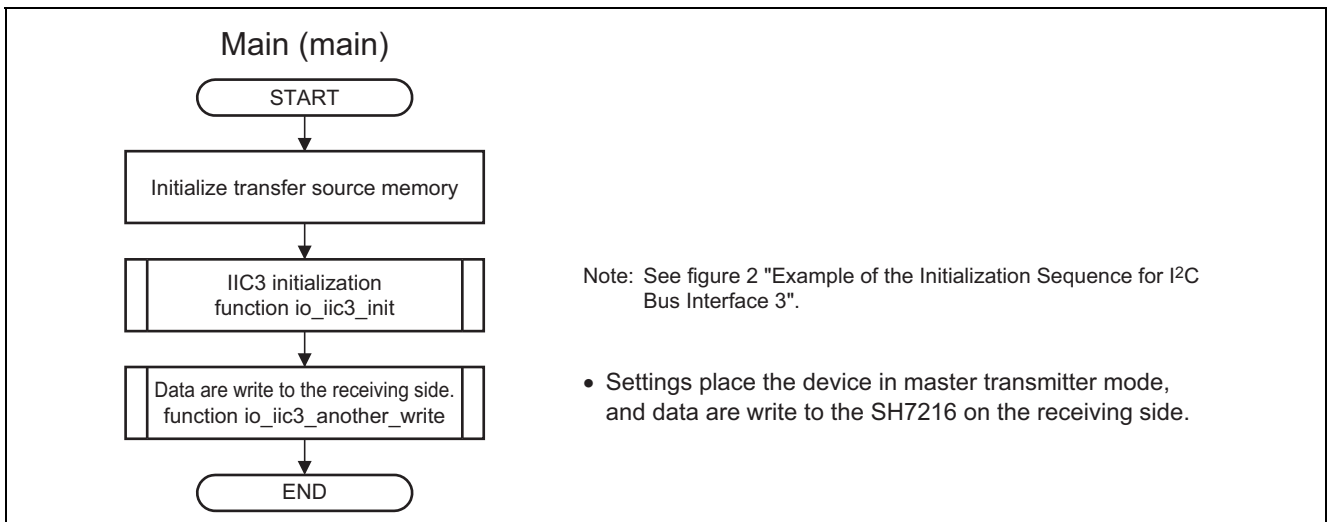


Figure 5 Flow of Processing by the Sample Program (1)

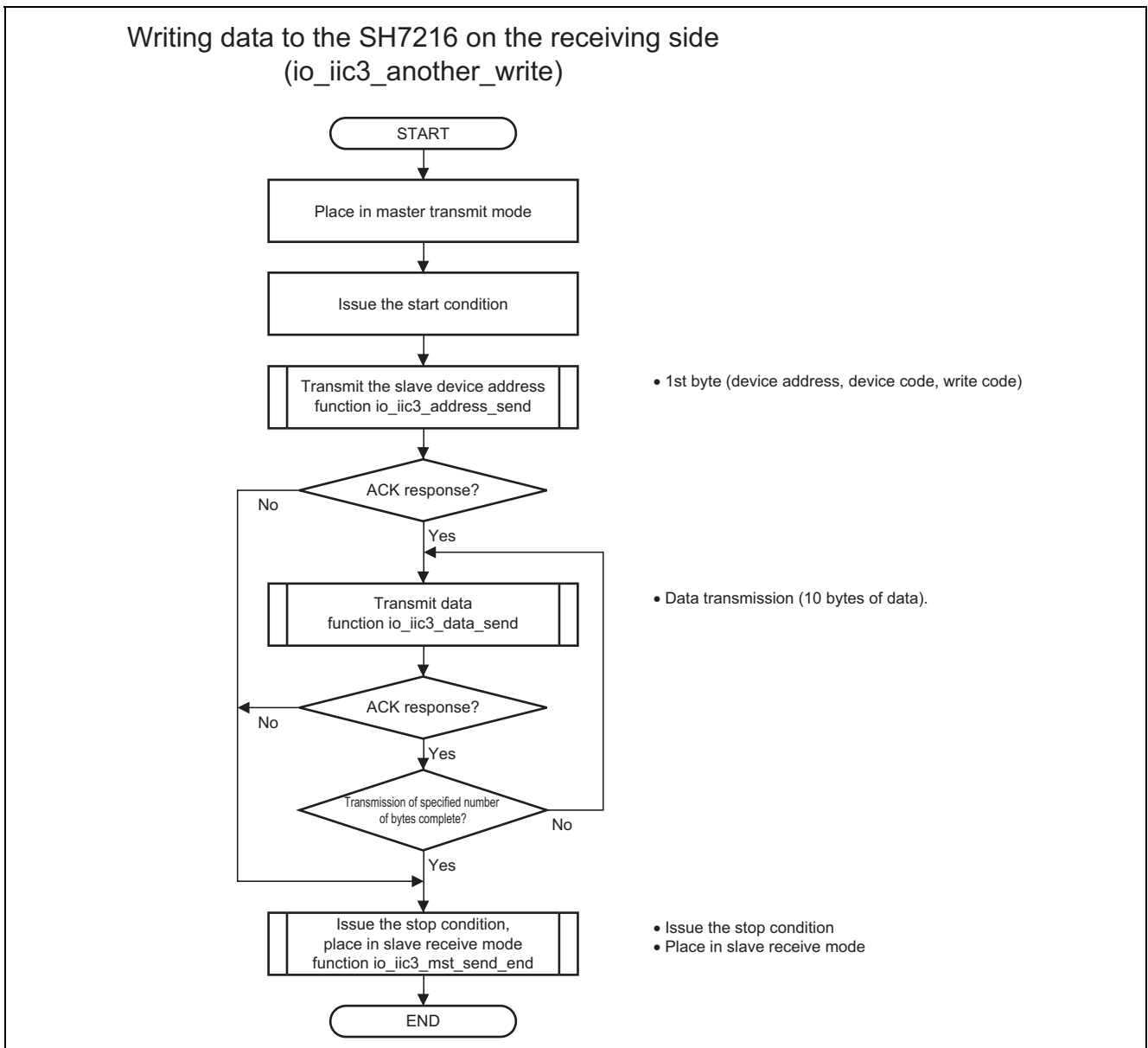


Figure 6 Flow of Processing by the Sample Program (2)

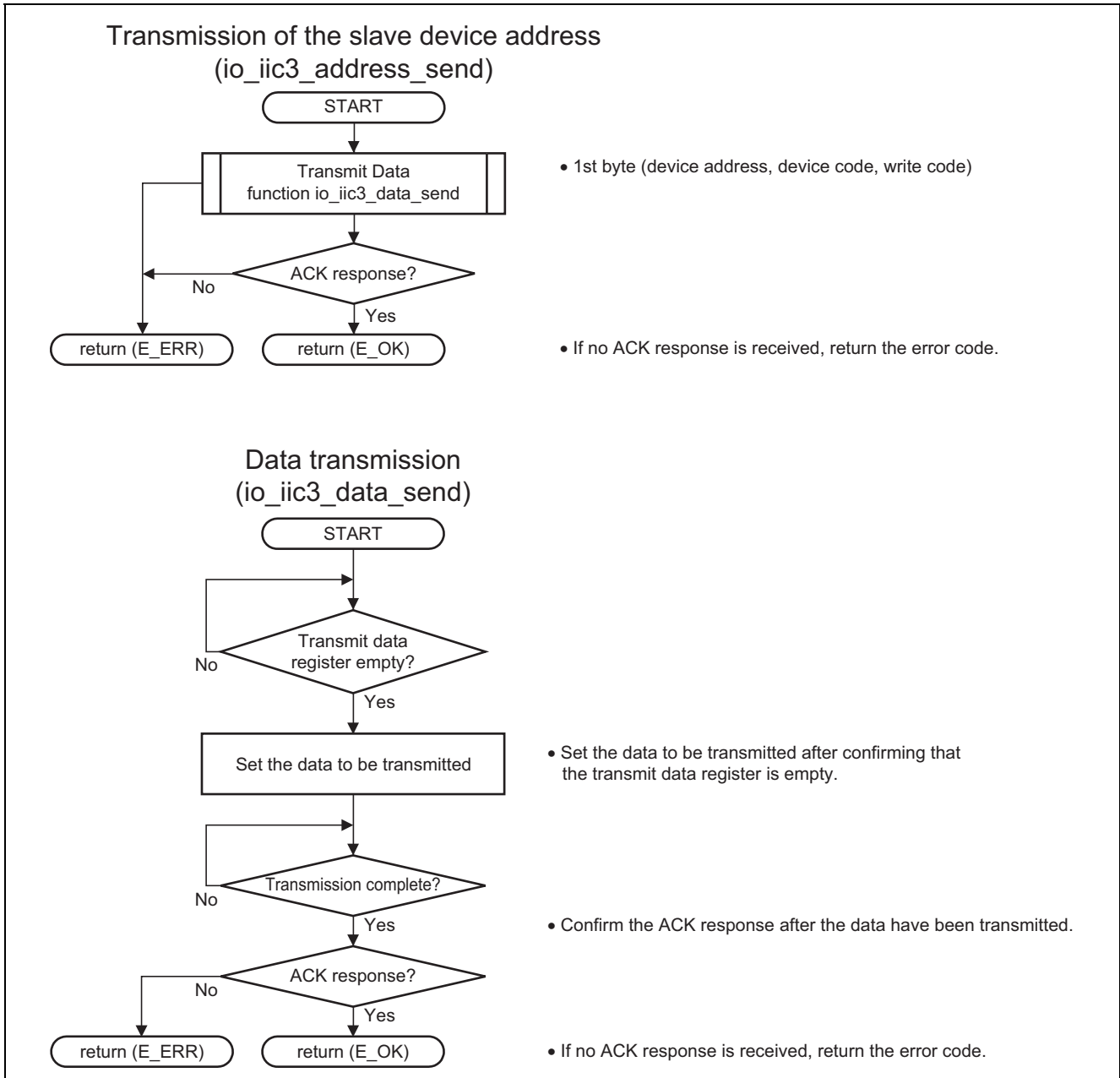


Figure 7 Flow of Processing by the Sample Program (3)

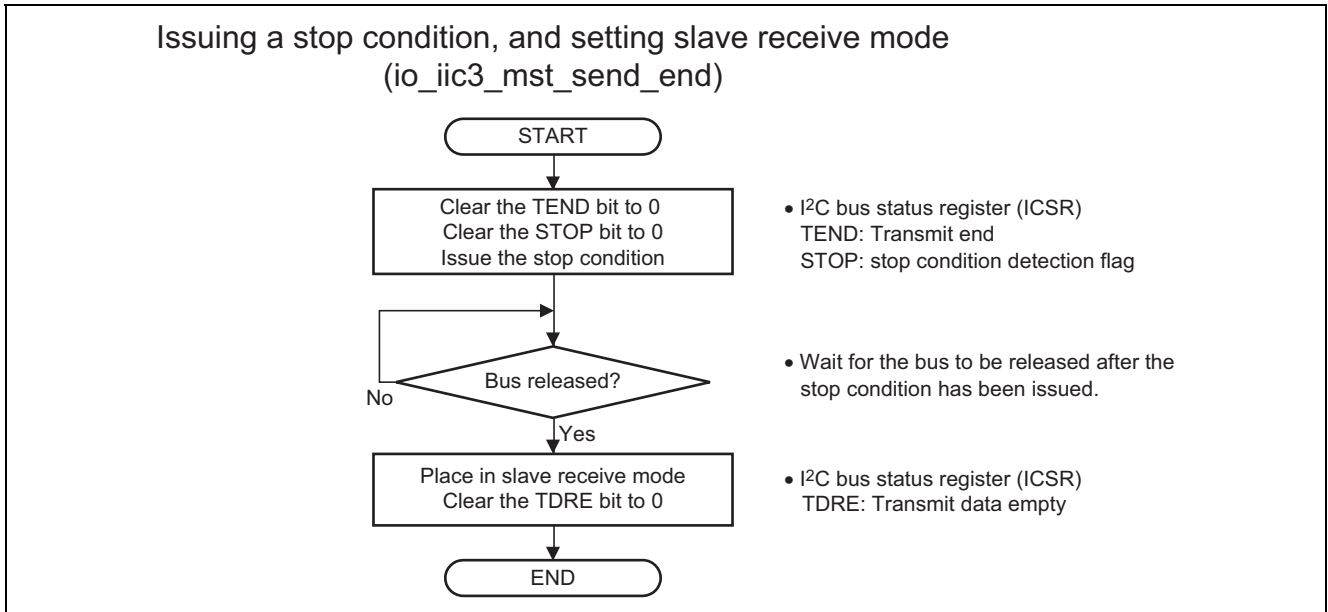


Figure 8 Flow of Processing by the Sample Program (4)

3. Listing of the Sample Program

```
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**"FILE COMMENT"***** Technical reference data *****  
*   System Name : SH7216 Sample Program  
*   File Name   : main.c  
*   Abstract    : Sample Program of Compare Match Timer  
*   Version     : 1.00.00  
*   Device      : SH7216  
*   Tool-Chain  : High-performance Embedded Workshop (Ver.4.05.01).  
*                : C/C++ compiler package for the SuperH RISC engine family  
*                :                               (Ver.9.03 Release01).  
*   OS          : None  
*   H/W Platform: R0K572167 (CPU board)  
*   Description :  
*   note       : This program sends data to the SH7211 base on the  
*               : slave-receive side by using the master-send mode of IIC3.  
*****  
*   History    : Jun.8,2009 Ver.1.00.00  
**"FILE COMMENT END"*****/  
#include <machine.h>  
#include "iodefine.h"      /* SH7216 iodefine */  
  
/* ==== symbol definition ==== */  
#define DEVICE_CODE 0xA0      /* another device code   : b'1010   */  
#define DEVICE_ADDR 0x00     /* another device address : b'000   */  
#define IIC_DATA_WR 0x00     /* Data write code       : b'0     */  
#define IIC_DATA_RD 0x01     /* Data read code        : b'1     */  
#define IIC3_DATA 10  
  
#define E_OK 0  
#define E_ERR -1  
  
/* ==== RAM allocation variable declaration ==== */  
unsigned char WriteData[IIC3_DATA];
```

Figure 9 Sample Program Listing: main.c (1)

```
/* ==== prototype declaration ==== */
void main(void);
int io_iic3_another_write(unsigned char d_code, unsigned char d_adr,
                          unsigned int w_size, unsigned char *w_buf);
int io_iic3_data_send(unsigned char data);
int io_iic3_address_send(unsigned char *data);
void io_iic3_mst_send_end(void);
int io_iic3_init(void);

void io_led_ini(void);
void io_init_cmt0(void);

/*"FUNC COMMENT"*****
 * Outline      : sumple program main
 *-----
 * Include      :
 *-----
 * Declaration  : void main(void);
 *-----
 * Function     : sumple program main
 *-----
 * Argument     : void
 *-----
 * Return Value : none
 *-----
 * Notice      :
 *"FUNC COMMENT END"*****/
void main(void)
{
    int i;

    /* ==== Writing data creation ==== */
    for(i = 0; i < IIC3_DATA; i++){
        WriteData[i] = IIC3_DATA+i;
    }

    /* ==== IIC3 initialization ==== */
    io_iic3_init();
    /* ==== IIC3 master-send mode ==== */
    io_iic3_another_write(DEVICE_CODE,          /* Device code */
                          DEVICE_ADDR,         /* Device address */
                          sizeof(WriteData),    /* Writing data's size */
                          WriteData);          /* Store the writing data */

    while(1){
        /* Loop */
    }
}
```

Figure 10 Sample Program Listing: main.c (2)

SH7216 Group Transmission by the I²C Bus Interface 3 Module in Master Operation

```
/*"FUNC COMMENT"*****
 * Outline      : IIC3-module initial setting
 *-----
 * Include      : #include "iodefine.h"
 *-----
 * Declaration  : int io_iic3_init(void);
 *-----
 * Function     : IIC3-module initial setting
 *-----
 * Argument     : void
 *-----
 * Return Value : E_OK
 *-----
 * Notice      :
 *"FUNC COMMENT END"*****/
int io_iic3_init(void)
{
    STB.CR3.BIT._IIC3 = 0x00;      /* Clear the IIC3 module standby mode */

    /* ---- PFC setting ---- */
    PFC.PBCRL4.BIT.PB12MD = 0x06; /* SCL selection */
    PFC.PBCRL4.BIT.PB13MD = 0x06; /* SDA selection */
    PFC.PBPCRL.BIT.PB12PCR = 1;   /* SCL pull-up */
    PFC.PBPCRL.BIT.PB13PCR = 1;   /* SDL pull-up */
    /* ----IIC31 module operation disabled ---- */
    IIC3.ICCR1.BIT.ICE = 0x00;    /* IIC3 transfer disabled state */
    IIC3.ICCR1.BIT.ICE = 0x01;    /* IIC3 transfer enabled */
    IIC3.ICCR1.BIT.RCVD = 0x00;   /* Continue the next receive data */
    IIC3.ICCR1.BIT.CKS = 0x07;    /* Transfer clock rate : Pφ/124(403kHz) */
    /* ---IIC bus mode register (ICMR) setting --- */
    IIC3.ICMR.BYTE = 0x30;
    /*
        bit7   : MLS:0 ----- MSB first
        bit6   : WAIT:0 ----- No WAIT insertion
        bit5-4 : Reserve:1 ----- Reserve bits
        bit3   : BCWP:0 ----- Unsetting
        bit2-0 : BC2:0, BC1:0, BC0:0 ----- IIC bus format: 9 bits
    */

    return(E_OK);
}
```

Figure 11 Sample Program Listing: main.c (3)

```

/*"FUNC COMMENT"*****
* Outline      : Write data for slave-side
*-----
* Include      : #include "iodefine.h"
*-----
* Declaration  : int io_iic3_mst_send(unsigned char d_code,
*                :                unsigned char d_adr,
*                :                unsigned int w_size,
*                :                unsigned char *w_buf);
*-----
* Function     : This master-send mode choose slave-side is specified
* : by d_code & d_adr.
* : Sending data to be written in slave-side is specified by w_buf,
* : and the data is "w_size"BYTE.
* : (DEVICE_CODE = d_code, DEVICE_ADDR = d_adr,
* : sizeof(WriteData) = w_size, WriteData = *w_buf)
*-----
* Argument     : unsigned char d_code ; Device code
* : unsigned char d_adr ; Device address
* : unsigned int w_size ; Writing data size
* : unsigned char* w_buf ; Store the writing data
*-----
* Return Value : E_OK ; ACK response
* : E_ERR ; No ACK response
*-----
* Notice      :
* "FUNC COMMENT END"*****/
int io_iic3_another_write(unsigned char d_code, unsigned char d_adr,
                          unsigned int w_size, unsigned char *w_buf)
{
    int ack = E_OK;
    int i;
    unsigned char send[1];

    send[0] = (unsigned char)(d_code | ((d_adr & 0x7) << 1) | IIC_DATA_WR);

    while(IIC3.ICCR2.BIT.BBSY == 0x01){
        /* It weits untill the bas is opened */
    }
    /* It sets it to the master send mode */
    IIC3.ICCR1.BYTE |= 0x30;
    /* Start condition is issued */
    IIC3.ICCR2.BYTE = ((IIC3.ICCR2.BYTE & 0xbf) | 0x80);

    ack = io_iic3_address_send(send); /* 1st BYTE send */

    if(ack == E_OK){
        /* When there is ack reaction from the specified device */
        for(i = 0; i < w_size; i++){
            ack = io_iic3_data_send(*w_buf++); /* Data send */
            if(ack == E_ERR){
                break;
            }
        }
        io_iic3_mst_send_end();
    }
    else{
        /* When there is ack reaction from the specified device */
        io_iic3_mst_send_end();
    }
    return(ack);
}

```

Figure 12 Sample Program Listing: main.c (4)

SH7216 Group Transmission by the I²C Bus Interface 3 Module in Master Operation

```
/*"FUNC COMMENT"*****
 * Outline      : Slave device address send
 *-----
 * Include      :
 *-----
 * Declaration  : int io_iic3_address_send(unsigned char *data);
 *-----
 * Function     : The address of the slave device specified with
 * : data (1byte) is sent.
 *-----
 * Argument     : unsigned char *data ; Sending data
 *-----
 * Return Value : E_OK ; ACK response
 *              : E_ERR ; No ACK response
 *-----
 * Notice      :
 *"FUNC COMMENT END"*****/
int io_iic3_address_send(unsigned char *data)
{
    int ack;

    ack = io_iic3_data_send(*data++); /* Address of slave device */
    if(ack == E_ERR){
        return(ack);
    }
    return(ack);
}
/*"FUNC COMMENT"*****
 * Outline      : 1byte data sending
 *-----
 * Include      : #include "iodefine.h"
 *-----
 * Declaration  : int io_iic3_data_send(unsigned char data);
 *-----
 * Function     : Data sending. The processing procedure is as follows.
 * : 1. ICDRT waits for even empty
 * : 2. Sending data set
 * : 3. Data sending completion confirmation
 * : 4. ACK response confirmation
 *-----
 * Argument     : unsigned char data ; Sending data
 *-----
 * Return Value : E_OK ; ACK response
 *              : E_ERR ; No ACK response
 *-----
 * Notice      :
 *"FUNC COMMENT END"*****/
int io_iic3_data_send(unsigned char data)
{
    int ack;
    while(IIC3.ICSR.BIT.TDRE == 0x0){
        /* 1. ICDRT waits for even empty */
    }
    IIC3.ICDRT = data; /* 2. Sending data set */
    while(IIC3.ICSR.BIT.TEND == 0x00){
        /* 3. Data sending completion confirmation */
    }
    /* 4. ACK response confirmation */
    if(IIC3.ICIER.BIT.ACKBR == 0){
        ack = E_OK;
    }
    else{
        ack = E_ERR;
    }
    return(ack);
}
}
```

Figure 13 Sample Program Listing: main.c (5)


```
/*"FUNC COMMENT"*****  
* Outline      : Stop condition issue  
*-----  
* Include      : #include "iodefine.h"  
*-----  
* Declaration  : void io_iic3_mst_send_end(void);  
*-----  
* Function     : The conditions stop is issued, and it switches to  
* : the slave-receive mode.  
*-----  
* Argument     : void  
*-----  
* Return Value : none  
*-----  
* Notice      :  
*"FUNC COMMENT END"*****/  
void io_iic3_mst_send_end(void)  
{  
    IIC3.ICSR.BIT.TEND = 0x00;    /* TEND Flag clear */  
    IIC3.ICSR.BIT.STOP = 0x00;   /* STOP Flag clear */  
    IIC3.ICCR2.BYTE &= 0x3f;     /* The conditions stop is issued */  
  
    while(IIC3.ICSR.BIT.STOP == 0x00){  
        /* It waits untill the bus is opened */  
    }  
  
    IIC3.ICCR1.BYTE &= 0xcf;     /* It switches to the slave-receive mode */  
    IIC3.ICSR.BIT.TDRE = 0x00;  /* TDRE clear */  
}  
/* End of File */
```

Figure 14 Sample Program Listing: main.c (6)

4. Documents for Reference

- Software Manual
SH-2A, SH2A-FPU Software Manual (REJ09B0051)
The most up-to-date version of this document is available on the Renesas Electronics Website.
- Hardware Manual
SH7216 Group Hardware Manual (REJ09B0543)
The most up-to-date version of this document is available on the Renesas Electronics Website.

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable.

When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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