SH7216 Group

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Transmission and Reception of Serial Data by the SCI in Asynchronous Mode

Introduction

This application note describes transmission and reception of serial data by the serial communications interface (SCI) in asynchronous mode.

Target Device

SH7216

Contents

1. Preface

1.1 Specifications

This sample application employs the asynchronous serial transfer function of the serial communications interface (SCI) to perform data transmission and reception. Figure 1 shows an example of connection for transmission and reception by the SCI in asynchronous mode.

- SCIF1 is used.
- The communications format has an 8-bit data length, 1 stop bit, and no parity bit.
- Once 8 bytes of data have been transmitted and received, each operation is halted.

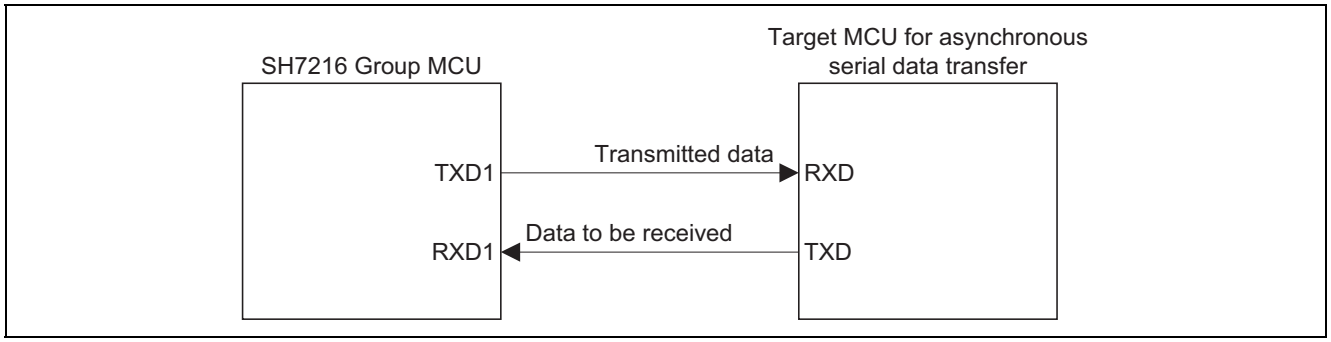


Figure 1 Connection Example for Transmission and Reception by the SCI in Asynchronous Mode

1.2 Module Used

- Serial communications interface (SCI1)
- Clock pulse generator (CPG)
- Power-Down Modes
- Pin function controller (PFC)

1.3 Applicable Conditions

- MCU SH7216
- Operating frequency Internal clock: 200 MHz
  Bus clock: 100 MHz
  Peripheral clock: 50 MHz
- Integrated development environment
  High-performance Embedded Workshop Ver.4.05.00
  (from Renesas Electronics Corp.)
- C compiler SuperH RISC Engine Family C/C++ Compiler Package Ver.9.03.00 Release00
  from Renesas Electronics Corp.
- Compiler options Default settings of the High-performance Embedded Workshop
  (-cpu=sh2afpu -pic=1 -object="$(CONFIGDIR)¥$(FILELEAF).obj"
  -debug -gbr=auto -chgincpath -errorpath -global_volatile=0
  -opt_range=all -infinite_loop=0 -del_vacant_loop=0
  -struct_alloc=1 -nologo)

1.4 Related Application Note

- SH7216 Group Application Note: Reception of Serial Data by the SCI in Asynchronous Mode (REJ06B0909)
- SH7216 Group Application Note: Transmission of Serial Data by the SCI in Asynchronous Mode (REJ06B0910)

2. Overview

The reference program employs the serial communications interface (SCI) of the SH7216 for the asynchronous transmission and reception of serial data from a target device.

2.1 Operational Overview of Module Used

In asynchronous mode, each transmitted or received character begins with a start bit and ends with a stop bit. Serial communications is synchronized in character units. The transmitting and receiving sections of the SCI are independent, so operations for transmission and reception can proceed simultaneously. Both the transmitter and receiver have a double-buffered structure so that data can be read or written during transmission or reception, which enables high-speed continuous data transfer.

In asynchronous serial communications, the communication line is normally held in the mark (high) state. The SCI monitors the line and starts serial communications when the line goes to the space (low) state, indicating a start bit.

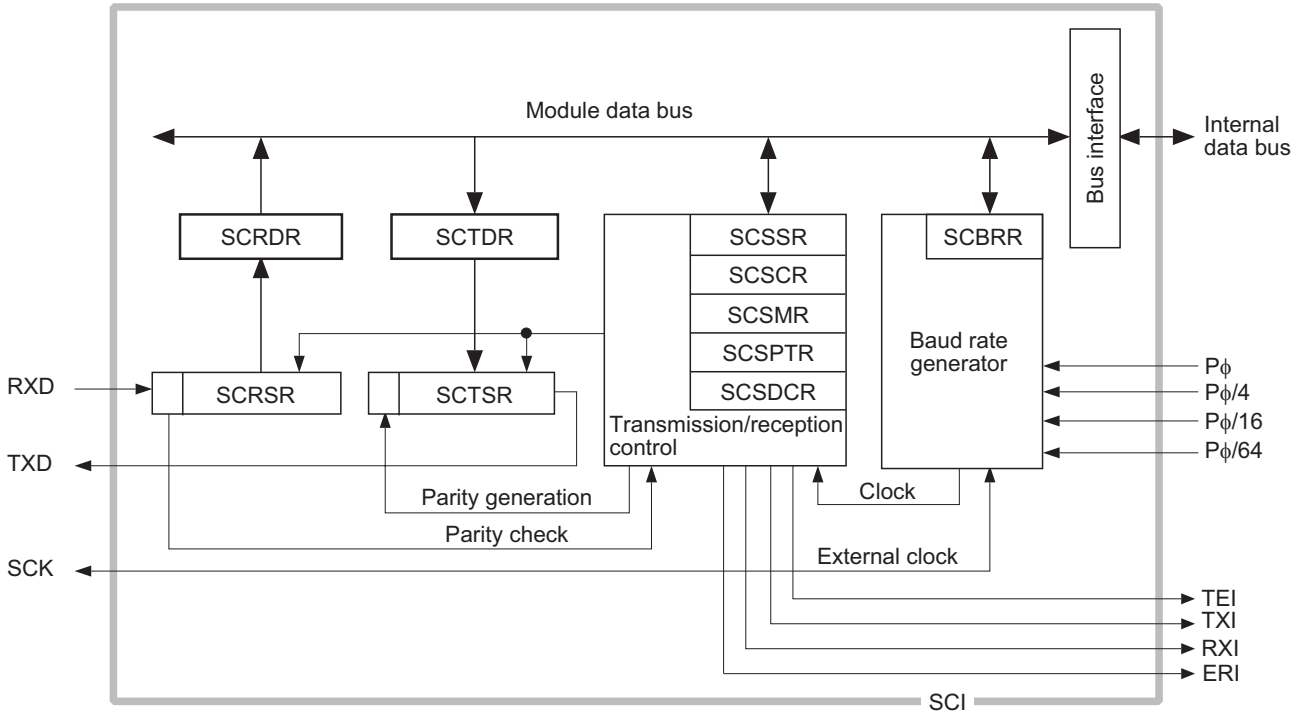
One serial character consists of a start bit (low), data (LSB first), parity bit (high or low), and stop bit (high), in this order.

For details on the SCI, please refer to the section on Serial Communication Interface (SCI) in the *SH7216 Group Hardware Manual* (REJ09B0543).

Table 1 gives an overview of serial communications in asynchronous mode. Figure 2 shows a block diagram of the SCI.

Table 1 Overview of Serial Data Communications in Asynchronous Mode

Item	Description
Number of interfaces	4 (SCI0, SCI1, SCI2 and SCI4)
Clock sources	For internal clock: Pϕ, Pϕ/4, Pϕ/16 and Pϕ64 (Pϕ: peripheral clock) For external clock: input clock on the SCK pin
Data format	Transfer data length: 7 or 8 bits Order: LSB first and MSB first are selectable
Baud rate	Asynchronous mode: 110 to 1,562,500 bps (Pϕ = 50 MHz)
Error detection	Framing, parity and overrun errors Breaks can also be detected.
Interrupt requests	Transmit-data-empty interrupt (TXI) Receive-data-full interrupt (RXI) Receive error interrupt (ERI) Transmit end interrupt (TEI)
Clock sources	Internal and external clocks are selectable • Internal clock: When the internal clock has been selected, the clock from the baud-rate generator is used to operate the SCI and a clock signal at 16 times the frequency of the bit rate can be output. • External clock: When the external clock has been selected, input of a clock signal at 16 times the frequency of the bit rate is required. (The on-chip baud rate generator is not used.)



[Legend]
SCRSR: Receive shift register
SCRDR: Receive data register
SCTSR: Transmit shift register
SCTDR: Transmit data register
SCSMR: Serial mode register
SCSCR: Serial control register
SCSSR: Serial status register
SCBRR: Bit rate register
SCSPTR: Serial port register
SCSDCR: Serial direction control register

Figure 2 Block Diagram of the SCI

2.2 Operation of the Sample Program

Table 2 lists the settings for the SCI communications function of this sample program.

Table 2 Settings for Communications Function of the Sample Program

Item	Description
Module	SCI1
Transfer mode	Asynchronous mode
Transfer rate	9600 bps
Number of data to be received	8 bytes
Data length	8-bit data
Stop bit	1 stop bit
Parity	None
Bit order	LSB-first

2.3 Procedure for Setting Module Used

This section describes the procedure for setting up SCI1 for asynchronous mode operation.

Figure 3 shows the flow of processing by the sample program, figure 4 shows the flow for initialization of data transmission and reception in asynchronous mode, figure 5 shows the flow of transmission processing in asynchronous mode, and figure 6 shows the flow of reception processing in asynchronous mode. For details on the settings of individual registers, see the *SH7216 Group Hardware Manual* (REJ09B0543).

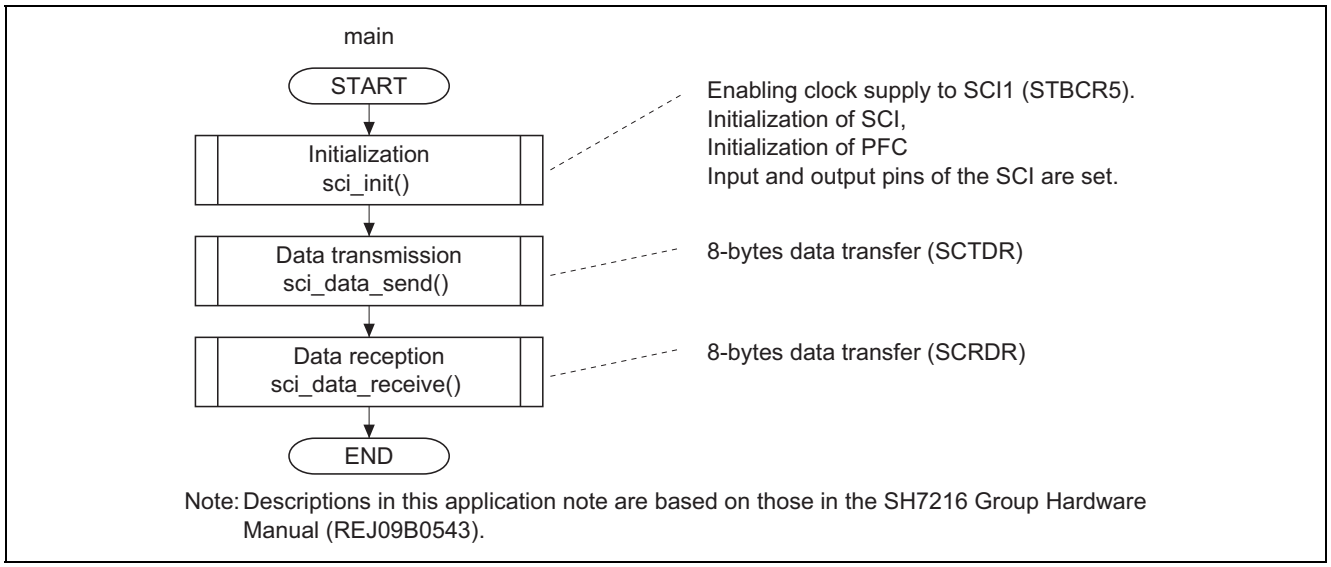


Figure 3 Flow of Processing by the Sample Program

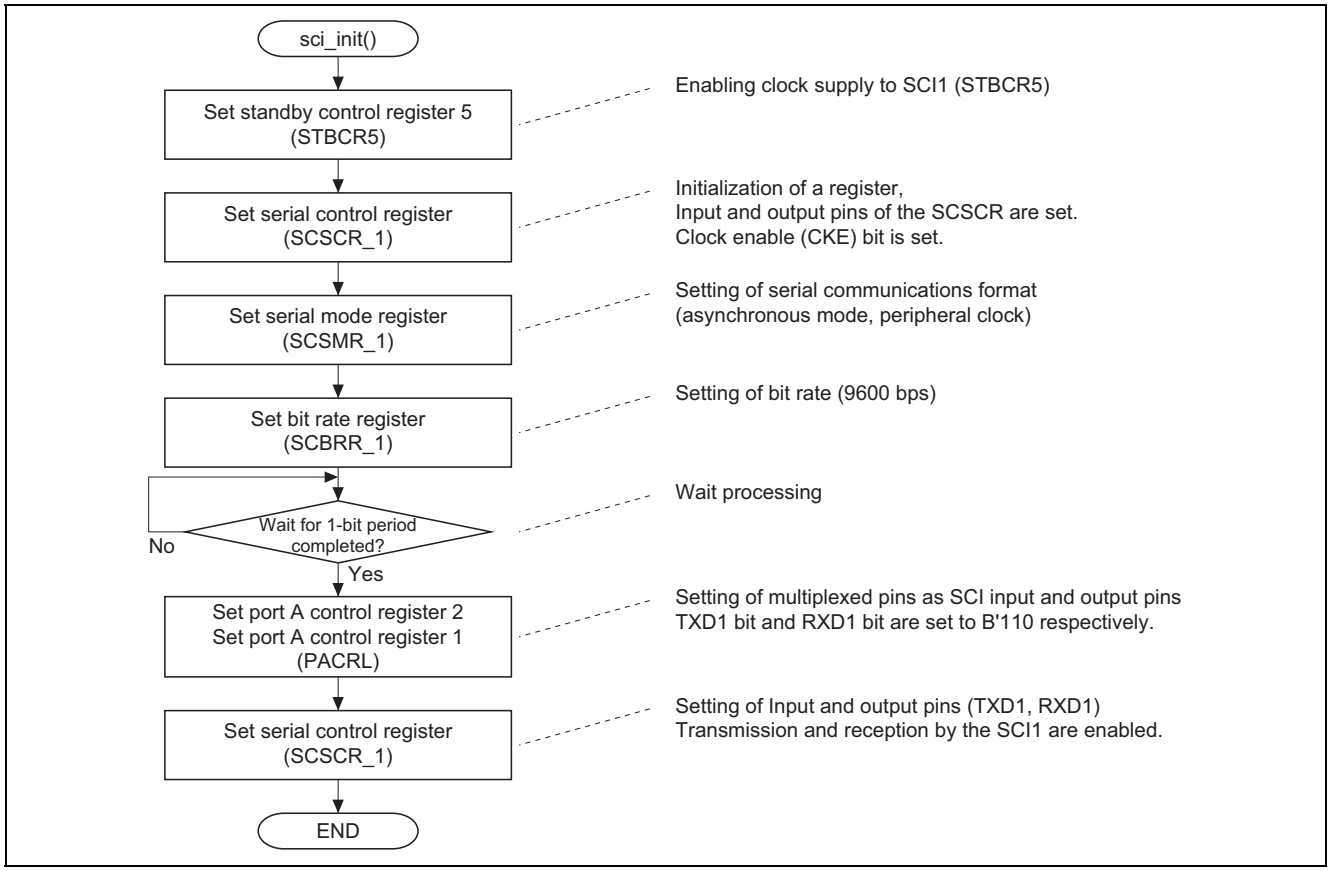


Figure 4 Flow for Initialization of Data Transmission and Reception in Asynchronous Mode

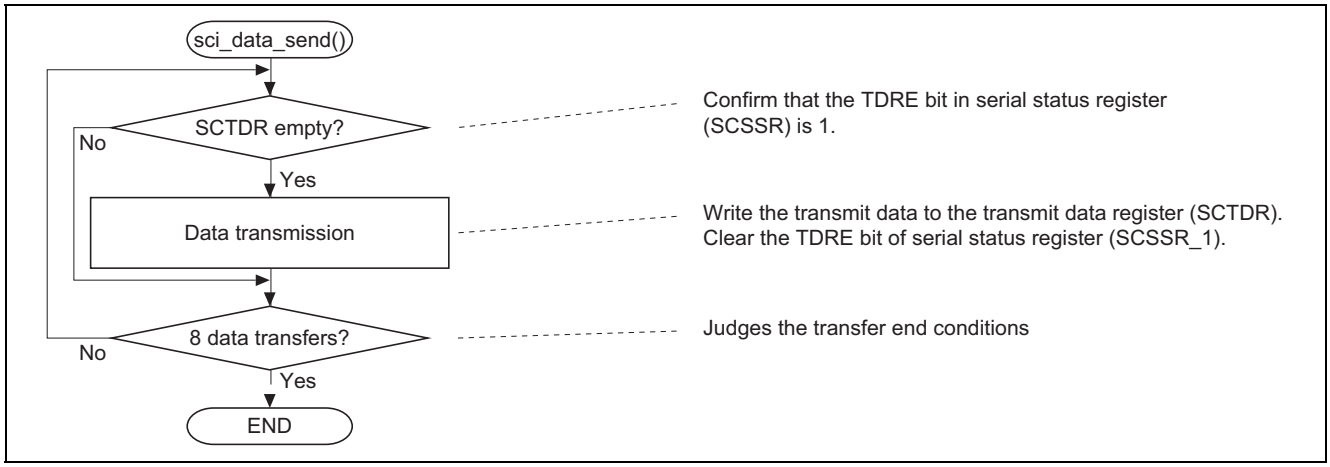


Figure 5 Flow of Transmission Processing in Asynchronous Mode

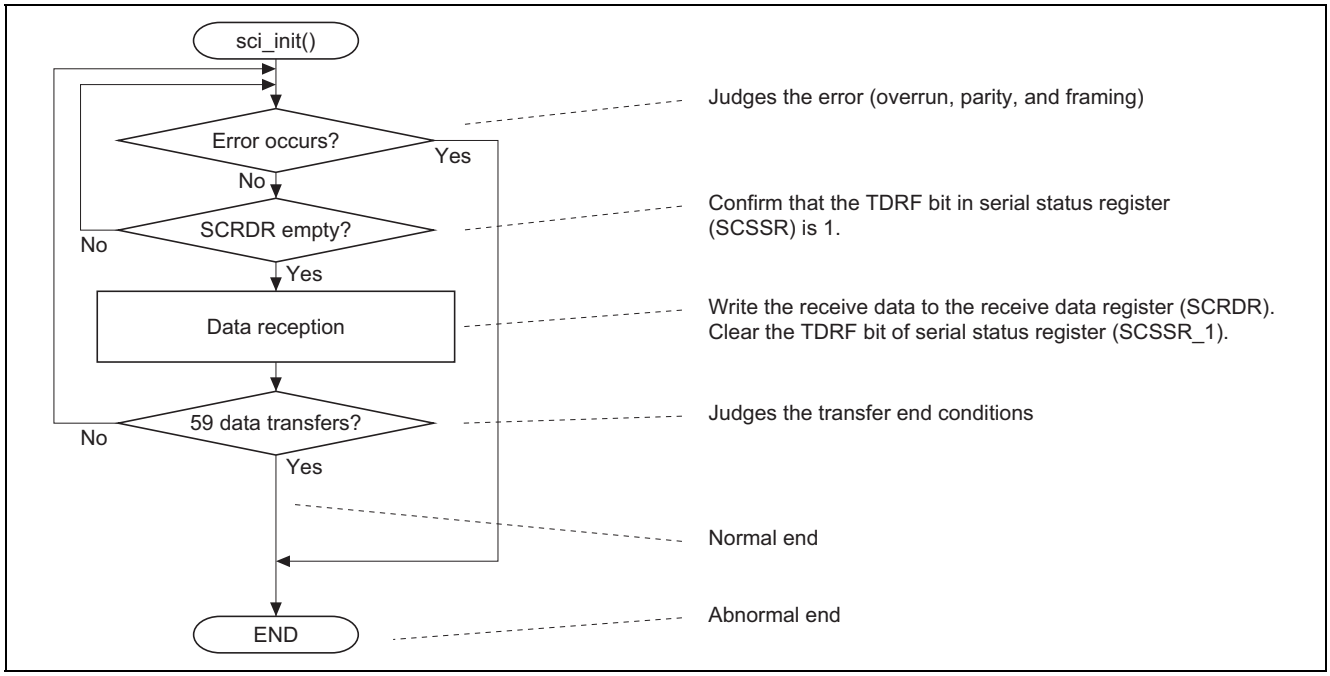


Figure 6 Flow of Reception Processing in Asynchronous Mode

2.4 Procedure for Processing by the Sample Program

Table 3 gives settings for the register in the sample program.

Table 3 Settings for the Register in the Sample Program

Register Name		Address	Setting	Description
Clock pulse generator (CPG)	Frequency control register (FRQCR)	H'FFFE0010	H'0303	STC [2:0] = "B'011": × 1/4 (Bϕ) IFC [2:0] = "B'000": × 1 (Iϕ) PFC [2:0] = "B'011": × 1/4 (Pϕ)
Standby control register	Standby control register 5 (STBCR5)	H'FFFE0418	H'BF	MSTP56 = "B'0": SCI1 operates
Pin function controller (PFC)	Port A control register L2 (PACRL2)	H'FFFE3814	H'0006	PA4MD [2:0] = "B'110": TXD1 output
	Port A control register L1 (PACRL1)	H'FFFE3816	H'6000	PA3MD [2:0] = "B'110": RXD1 input
Serial communications interface (SCI)	Serial mode register_1 (SCSMR_1)	H'FFFF8800	H'00	C/A = "B'0": Asynchronous mode CHR = "B'0": 8-bit data PE = "B'0": Disables adding and checking of parity bits STOP = "B'0": 1 stop bit CKS [1:0] = "B'00": Pϕ clock
	Bit rate register_1 (SCBRR_1)	H'FFFF8802	H'A2	Asynchronous mode Bit rate: 9600 bps
	Serial control register_1 (SCSCR_1)	H'FFFF8804	H'30	When transmitting and receiving operations are enabled TIE = "B'1": Enables transmit-data-empty interrupt (TXI) request TE = "B'0": Enables transmission of data
	Serial status register_1 (SCSSR_1)	H'FFFF8808	H'04	At the time of setting The TDRE flag is cleared to 0.

3. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual (REJ09B0051)
  (The most up-to-date version of this document is available on the Renesas Electronics Website.)
- Hardware Manual
  SH7216 Group Hardware Manual (REJ09B0543)
  (The most up-to-date version of this document is available on the Renesas Electronics Website.)

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.10.09	—	First edition issued
1.01	Jun.25.10	—	Modifications to source project due to change in FRQCR setting method

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
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