To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

H8/300L SLP Series

Transition to Subsleep Mode

Introduction

This sample task shows an example of making transition to the subsleep mode. The system in the high-speed active mode enters the subactive mode by executing a SLEEP instruction under certain conditions. It then goes to the subsleep mode.

Target Device

H8/38024

Contents

1. Specifications

1. This sample task shows an example of making transition to the subsleep mode.
2. The system goes to the subactive mode by executing a SLEEP instruction when SSBY is 1 and LSON is 1 in SYSCR1, DTON in SYSCR2 is 1, and TMA3 in TMA is 1 in the high-speed active mode.
3. The system goes to the subsleep mode by executing a SLEEP instruction when SSBY is 0 and LSON is 1 in SYSCR1, and TMA3 in TMA is 1 in subactive mode.
4. The subsleep mode is terminated by a Timer A interrupt and the system returns to the subactive mode.
5. The Timer A interrupt handling routine controls the LED and counts the number of Timer A interrupts. A Timer A interrupt is generated every 0.5 sec. When the 120th Timer A interrupt has been generated, Timer A interrupt requests are disabled and the processing ends. The LED is turned on and off alternately every 0.5 sec.
6. When a Timer A interrupt occurs and the mode changes to the subactive mode, the Timer A interrupt count is checked and the mode again changes to the subsleep mode. This process is repeated until 120 Timer A interrupts are generated.
7. The LED is connected to P92 output pin of port 9.
8. P92 is a large-current port.

2. Description of Functions

1. In this sample task, the operating mode is changed to the subsleep mode, a power down mode. Figure 2.1 is a diagram of mode transition to the subsleep mode. The function of the subsleep mode is described below.
   - When a SLEEP instruction is executed in the high-speed active mode while SSBY is set to 1 and LSON is set to 1 in SYSCR1, DTON in SYSCR2 is set to 1, and TMA3 in TMA is set to 1, the mode changes to the subactive mode.
   - When a SLEEP instruction is executed in the subactive mode while SSBY in SYSCR1 is set to 0 and LSON in SYSCR2 is set to 1, and TMA3 in TMA is set to 1, the mode changes to the subsleep mode.
   - In the subsleep mode, the on-chip peripheral functions are halted except for Timer A, Timer C, Timer F and Timer G.
   - The contents of the CPU registers, some on-chip peripheral module registers, and on-chip RAM are retained as long as the rated voltage is supplied. The I/O ports hold their states they had before the transition.
   - The subsleep mode is terminated by an interrupt (Timer A, Timer C, Timer F, Timer G, SCI3, IRQ4, IRQ3, IRQ1, IRQ0, IRQAEC, WKP7 to WKP0, AEC) or by $\overline{\text{RES}}$ pin input.
   - In the case of terminating the mode by an interrupt, the subsleep mode is terminated and an interrupt exception handling starts when an interrupt request is generated. If the I bit in CCR is 1, or an acceptance of interrupts is disabled by the interrupt enable register, the subsleep mode will not be terminated.
   - In the case of terminating the watch mode by $\overline{\text{RES}}$ pin, the oscillation of the system clock starts when the $\overline{\text{RES}}$ pin is driven "Low". When the $\overline{\text{RES}}$ pin is driven "High" after the specified oscillation stabilization time has elapsed, the CPU starts reset exception handling. It should be noted that the system clock is supplied to the entire LSI at the moment the system clock oscillation has started. The $\overline{\text{RES}}$ pin must be kept "Low" until the oscillation of the system clock stabilizes.
   - In this sample task, the subsleep mode is terminated by a Timer A interrupt. After the subsleep mode is terminated, the mode changes to the subactive mode.
   - If a SLEEP instruction is executed in the subactive mode while SSBY is set to 1 and LSON is set to 0 in SYSCR1, MSON is set to 0 and DTON is set to 1 in SYSCR2, and TMA3 in TMA is set to 1, the mode changes directly to the high-speed active mode via the watch mode after the time set by STS2 to STS0 in SYSCR1 has elapsed.
   - The oscillation stabilization time after the termination of subactive mode is set by STS2 to STS0 in SYSCR1.
   - In this sample task, the oscillation stabilization time is set to 1.638 ms.

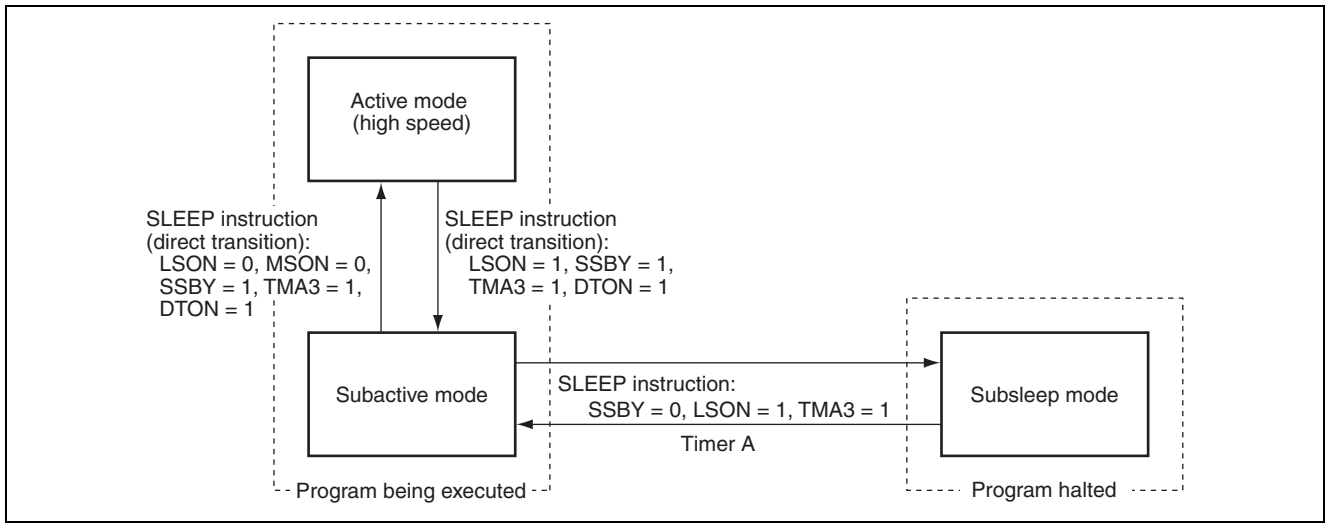


Figure 2.1 Mode Transition from/to Subsleep Mode

2. Table 2.1 shows the assignment of functions in this sample task. Mode transition to the subsleep mode is performed by assigning the functions as shown in table 2.1.

Table 2.1 Function Assignment

Function	Assignment
PSW	A 5-bit up counter using the subclock (32.768 KHz)/4 as input.
SYSCR1	Controls power down modes.
SYSCR2	Controls power down modes.
PDR9	P92 output pin data storage
P92	LED output
TMA	Sets Timer A clock time-base function and TCA overflow period.
TCA	An 8-bit up-counter which overflows every 0.5 sec. by the clock time-base function
IRRTA	Indicates whether or not a Timer A interrupt request has been generated.
IRRDT	Indicates whether or not a direct transition interrupt request has been generated.
IENTA	Enables or disables Timer A interrupt requests.
IENDT	Enables direct transition interrupt requests

3. Principle of Operation

1. Figure 3.1 illustrates the operation of this sample task. Transition to the subsleep mode is made through hardware and software processing as shown in the figure.

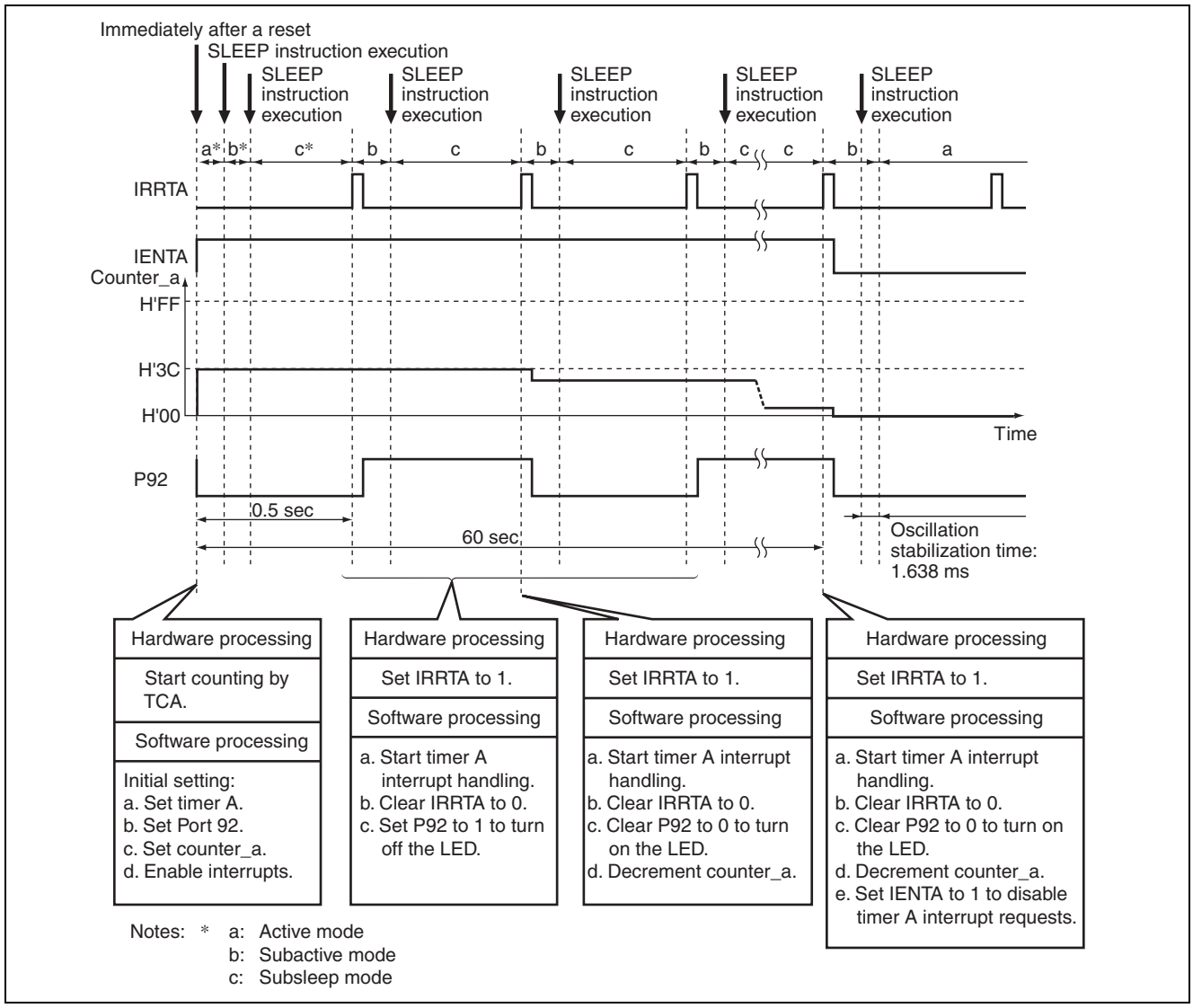


Figure 3.1 Operation Principle of Making Transition to Subsleep Mode

4. Description of Software

4.1 Modules

The modules used in this sample task are shown in table 4.1.

Table 4.1 Description of Module

Module	Label	Function
Main routine	main	Makes settings for Timer A interrupt, port 9, and counter_a, enables interrupts, and makes transition to the subactive mode, watch mode and high-speed active mode.
LED control	taint	A Timer A interrupt handling routine which controls the LED, decrements counter_a, and disables Timer A interrupt requests after 60 sec.
Direct transition	dtint	A direct transition interrupt handling routine which clears the direct transition interrupt request flag.

4.2 Arguments

This sample task does not use arguments.

4.3 Internal Registers

Table 4.2 shows the internal registers used in this sample task.

Table 4.2 Description of Internal Registers

Register		Function	Address	Setting
TMA		Timer Mode Register A If TMA = H'19, Timer A function is set to the clock time-base function and TCA overflow period is set to 0.5 sec.	H'FFB0	H'19
TCA		Timer Counter A An 8-bit up-counter which overflows every 0.5 sec by the clock time-base function and uses PSW output clock as input.	H'FFB1	H'00
PDR9	P92	Port Data Register 9 (Port Data Register 92) If P92 = 0, the output level of P92 pin is "Low". If P92 = 1, the output level of P92 pin is "High".	H'FFDC Bit 2	1
SYSCR1	STS2 STS1 STS0	System Control Register 1 (Standby Timer Select 2,1,0) If STS2 = 0, STS1 = 0, and STS0 = 0, oscillation stabilization time after the standby or subsleep mode is terminated is set to 1.638 ms.	H'FFF0 Bit 6 Bit 5 Bit 4	STS2 = 0 STS1 = 0 STS0 = 0
	SSBY	System Control Register 1 (Software Standby) If SSBY = 0, a transition is made to the sleep mode after a SLEEP instruction is executed in the active mode. A transition is made to the subsleep mode after a SLEEP instruction is executed in the subactive mode. If SSBY = 1, a transition is made to the standby mode or watch mode after a SLEEP instruction is executed in the active mode. A transition is made to the subsleep mode after a SLEEP instruction is executed in the subactive mode.	H'FFF0 Bit 7	1
	LSON	System Control Register 1 (Low Speed ON Flag) If LSON = 0, the CPU operating clock is set to the system clock after the watch mode is terminated. If LSON = 1, the CPU operating clock is set to the subsystem clock after the watch mode is terminated.	H'FFF0 Bit 3	0

Register		Function	Address	Setting
SYSCR2	DTON	System Control Register 2 (Direct Transfer ON Flag) If DTON = 0, a transition is made to the standby, watch or sleep mode when a SLEEP instruction is executed in the active mode. a transition is made to the watch or subsleep mode when a SLEEP instruction is executed in the subactive mode. If DTON = 1, A direct transition is made to the high-speed active mode (when SSBY = 1, TMA3 = 1,LSON = 0, MSON = 0) or to the medium-speed active mode (when SSBY = 1, TMA3 = 1, LSON = 0, MSON = 1) when a SLEEP instruction is executed in the subactive mode.	H'FFF1 Bit 3	1
	MSON	System Control Register 2 (Middle Speed ON Flag) If MSON = 0, the system operates in the high-speed active mode after terminating the standby, watch or sleep mode. The system operates in the high-speed sleep mode when a SLEEP instruction is executed in the active mode. If MSON = 1, the system operates in the medium-speed active mode after terminating the standby, watch or sleep mode. The system operates in the medium-speed sleep mode when a SLEEP instruction is executed in the active mode.	H'FFF1 Bit 2	0
	SA1 SA0	System Control Register 2 (Subactive Mode Clock Select 1, 0) If SA1 = 0 and SA0 = 0, the CPU operating clock in the subactive mode is set to $\phi_w/8$.	H'FFF1 Bit 1 Bit 0	SA1 = 0 SA0 = 0
IENR1	IENTA	Interrupt Enable Register 1 (Timer A Interrupt Enable) If IENTA = 0, Timer A interrupt requests are disabled. If IENTA = 1, Timer A interrupt requests are enabled.	H'FFF3 Bit 7	1
IENR2	IENDT	Interrupt Enable Register 2 (Direct Transition Interrupt Enable) If IENDT = 0, interrupt requests by direct transition are disabled. If IENDT = 1, interrupt requests by direct transition are enabled.	H'FFF4 Bit 7	1
IRR1	IRRTA	Interrupt Request Register 1 (Timer A Interrupt Request Flag) If IRRTA = 0, a Timer A interrupt is not requested. If IRRTA = 1, a Timer A interrupt has been requested.	H'FFF6 Bit 7	0
IRR2	IRRDT	Interrupt Request Register 2 (Direct Transition Interrupt Request Flag) If IRRDT = 0, an interrupt by direct transition is not requested. If IRRDT = 1, an interrupt by direct transition has been requested.	H'FFF7 Bit 7	0

4.4 Description of RAM

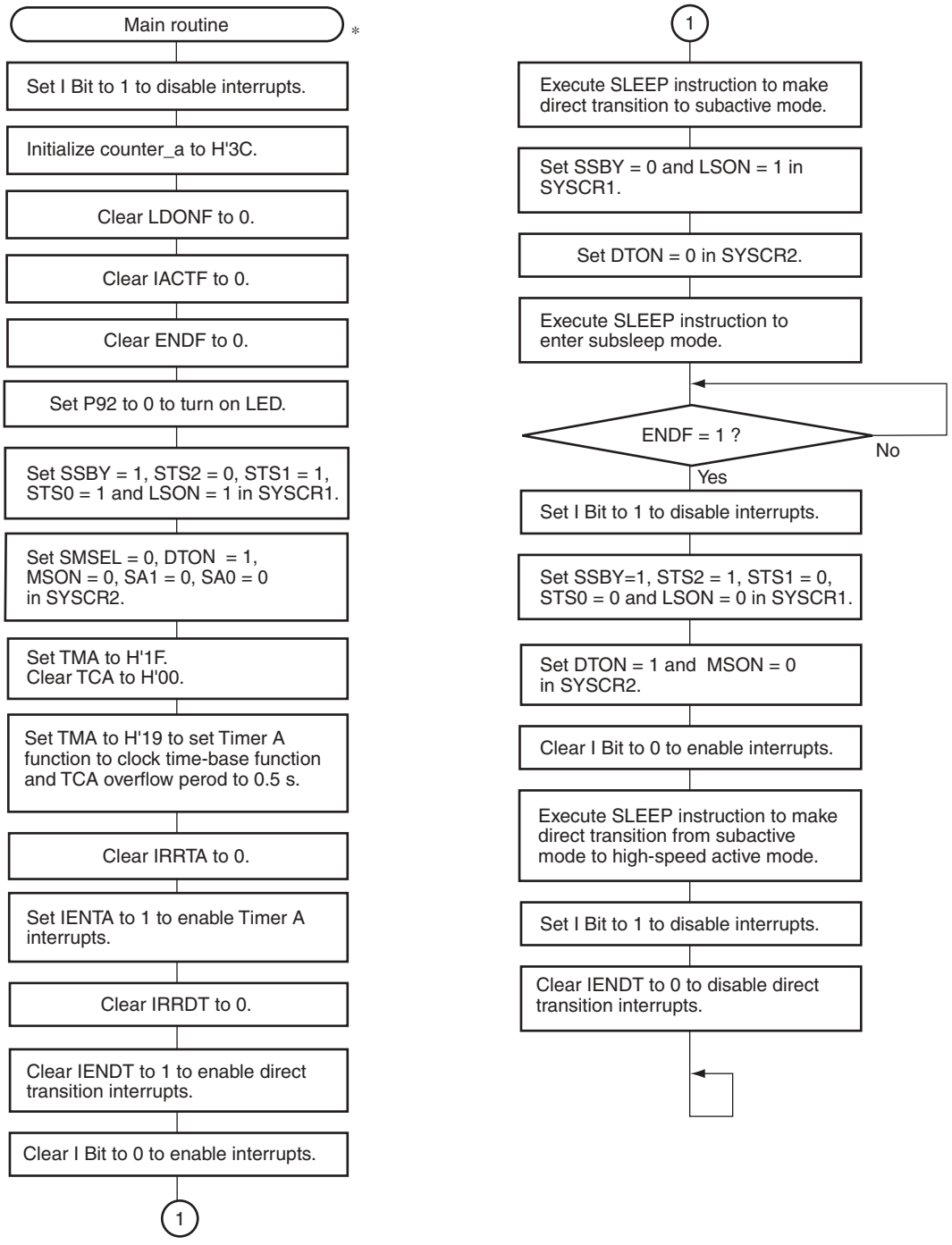
Table 4.3 describes the RAM area used in this sample task.

Table 4.3 Description of RAM

Label		Function	Address	Used in
counter_a		Down-counter to count Timer A interrupts	H'FB80	Main routine LED control
USRF	ENDF	Flag to judge whether 60 sec. has elapsed	H'FB81 Bit 2	Main routine LED control
	IACTF	Flag to judge whether the Timer A interrupt count is odd or even.	H'FB81 Bit 1	Main routine LED control
	LDONF	Flag to judge whether the LED is on or off	H'FB81 Bit 0	Main routine LED control

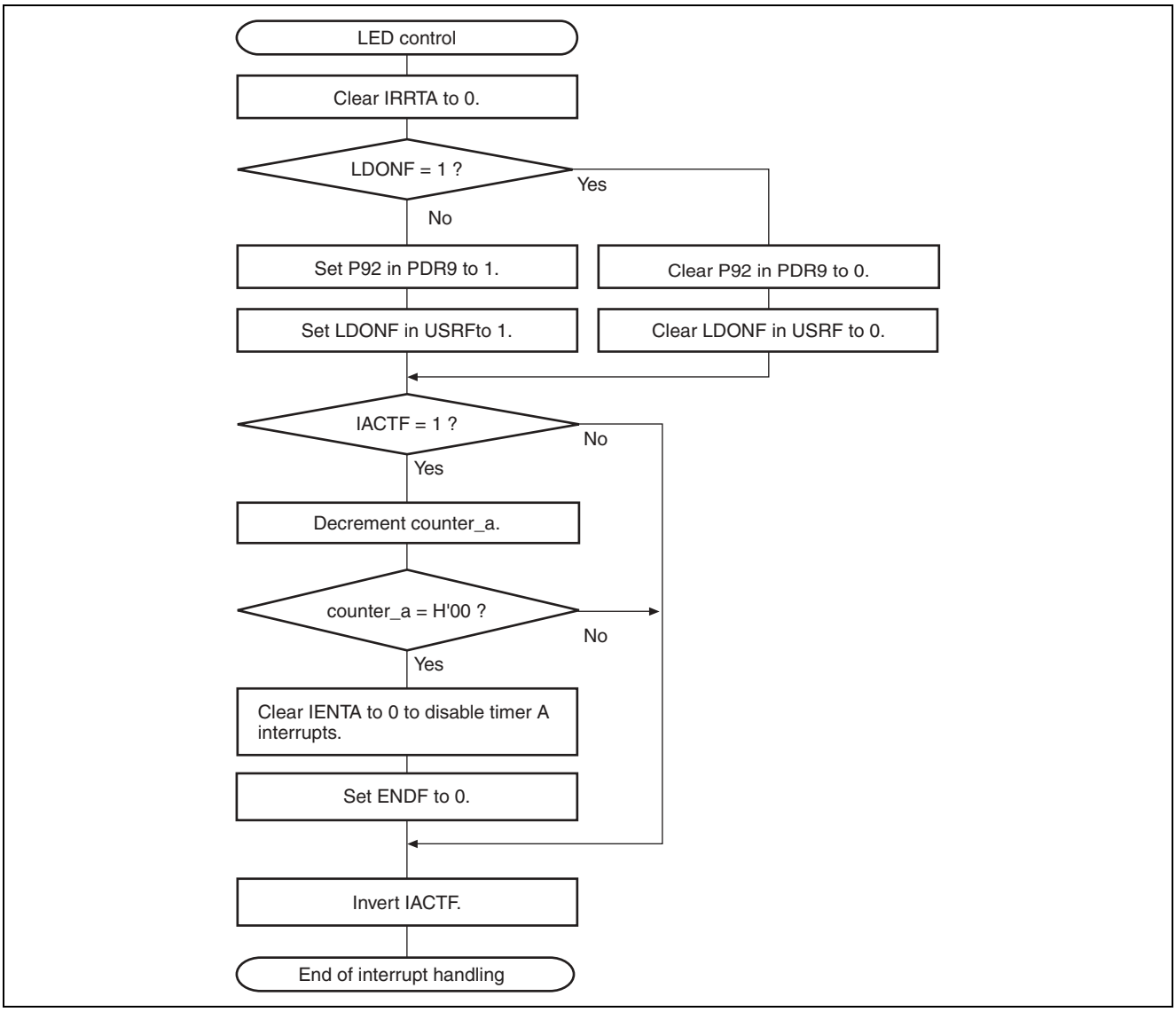
5. Flowchart

1. Main routine

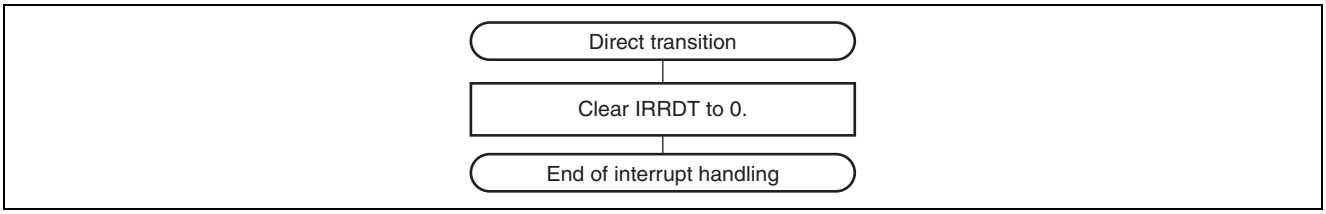


Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

2. Timer A interrupt handling routine



3. Direct transition interrupt handling routine



6. Program Listing

INIT.SRC (Program listing)

```
    .EXPORT   _INIT
    .IMPORT   _main
;
    .SECTION  P,CODE
_INIT:
    MOV.W     #H'FF80,R7
    LDC.B     #B'10000000,CCR
    JMP       @_main
;
    .END
```

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*  H8/300L Super Low Power Series                                                                                      */
/*      -H8/38024 Series-                                                                                               */
/*  Application Note                                                                                                    */
/*                                                                                                                      */
/*  'Transition to subsleep Mode'                                                                                       */
/*                                                                                                                      */
/*  Function                                                                                                            */
/*  : Power-Down Mode                                                                                                   */
/*     Subsleep Mode                                                                                                    */
/*                                                                                                                      */
/*  External Clock : 10MHz                                                                                              */
/*  Internal Clock : 5MHz                                                                                               */
/*  Sub Clock      : 32.768kHz                                                                                          */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*  Symbol Definition                                                                                                   */
/************************************************************************************************************************/
struct BIT {
    unsigned char   b7:1;       /* bit7 */
    unsigned char   b6:1;       /* bit6 */
    unsigned char   b5:1;       /* bit5 */
    unsigned char   b4:1;       /* bit4 */
    unsigned char   b3:1;       /* bit3 */
    unsigned char   b2:1;       /* bit2 */
    unsigned char   b1:1;       /* bit1 */
    unsigned char   b0:1;       /* bit0 */
};

#define     TMA         *(volatile unsigned char *)0xFFB0       /* Timer Mode Register A                */
#define     TCA         *(volatile unsigned char *)0xFFB1       /* Timer Counter A                      */
#define     PDR9_BIT    (*(struct BIT *)0xFFDC)                 /* Port Data Register 9                 */
#define     P92         PDR9_BIT.b2                             /* Port Data Register 92                */
#define     SYSCR1      *(volatile unsigned char *)0xFFF0       /* System Control Register 1            */
#define     SYSCR1_BIT  (*(struct BIT *)0xFFF0)                 /* System Control Register 1            */
#define     SSBY        SYSCR1_BIT.b7                           /* Software Standby                     */
#define     STS2        SYSCR1_BIT.b6                           /* Standby Timer Select 2               */
#define     STS1        SYSCR1_BIT.b5                           /* Standby Timer Select 1               */
#define     STS0        SYSCR1_BIT.b4                           /* Standby Timer Select 0               */
```

```
#define     LSON        SYSCR1_BIT.b3                       /* Low Speed On Flag                        */
#define     MA1         SYSCR1_BIT.b1                       /* Active Mode Clock Select 1               */
#define     MA0         SYSCR1_BIT.b0                       /* Active Mode Clock Select 0               */
#define     SYSCR2      *(volatile unsigned char *)0xFFF1   /* System Control Register 2                */
#define     SYSCR2_BIT  (*(struct BIT *)0xFFF1)             /* System Control Register 2                */
#define     NESEL       SYSCR2_BIT.b4                       /* Noise Elimination Sampling               */
                                                            /*                           Frequency Select */
#define     DTON        SYSCR2_BIT.b3                       /* Direct Transfer On Flag                  */
#define     MSON        SYSCR2_BIT.b2                       /* Middle Speed On Flag                     */
#define     SA1         SYSCR2_BIT.b1                       /* Subactive Mode Clock Select 1            */
#define     SA0         SYSCR2_BIT.b0                       /* Subactive Mode Clock Select 0            */
#define     IENR1_BIT   (*(struct BIT *)0xFFF3)             /* Interrupt Enable Register 1              */
#define     IENTA       IENR1_BIT.b7                        /* Timer A Interrupt Enable                 */
#define     IENR2_BIT   (*(struct BIT *)0xFFF4)             /* Interrupt Enable Register 2              */
#define     IENDT       IENR2_BIT.b7                        /* Direct Transfer Interrupt Enable         */
#define     IRR1_BIT    (*(struct BIT *)0xFFF6)             /* Interrupt Request Register 1             */
#define     IRRTA       IRR1_BIT.b7                         /* Timer A Interrupt Request Flag           */
#define     IRR2_BIT    (*(struct BIT *)0xFFF7)             /* Interrupt Request Register 2             */
#define     IRRDT       IRR2_BIT.b7                         /* Direct Transfer Interrupt Request Flag   */

#pragma interrupt   (taint)
#pragma interrupt   (dtint)
/************************************************************************************************************/
/*  Function define                                                                                         */
/************************************************************************************************************/
extern void INIT ( void );                                  /* SP Set                                   */
void        main ( void );
void        dtint ( void );
void        taint ( void );

/************************************************************************************************************/
/*  RAM define                                                                                              */
/************************************************************************************************************/
unsigned char    counter_a;
unsigned char    USRF;                                      /* User Flag Area                           */

#define     USRF_BIT    (*(struct BIT *)&USRF)
#define     ENDF        USRF_BIT.b2                         /* End Flag                                 */
#define     IACTF       USRF_BIT.b1                         /* Timer A Interrupt Counter Flag           */
#define     LDONF       USRF_BIT.b0                         /* LED On Flag                              */

/************************************************************************************************************/
/*  Vector Address                                                                                          */
/************************************************************************************************************/
#pragma section     V1                                      /* Vector Section Set                       */
void (*const VEC_TBL1[])(void) = {
    INIT                                                    /* 0x0000 Reset Vector                      */
};
#pragma section     V2                                      /* Vector Section Set                       */
void (*const VEC_TBL2[])(void) = {
    taint                                                   /* 0x0016 timer A  Interrupt Vector         */
};
#pragma section     V3                                      /* Vector Section Set                       */
void (*const VEC_TBL3[])(void) = {
    dtint                                                   /* 0x0028 Direct Transfer Interrupt Vector  */
};

#pragma section                                             /* P                                        */
```

```
/*****************************************************************************************************************/
/*  Main Program                                                                                                 */
/*****************************************************************************************************************/
void    main ( void )
{
    set_imask_ccr(1);                                   /* Interrupt Disable                        */

    counter_a = 0x3C;                                   /* Initialize 8bit Timer A Interrupt Counter*/
    LDONF = 0;                                          /* Initialize LDONF                         */
    IACTF = 0;                                          /* Initialize IACTF                         */
    ENDF = 0;                                           /* Initialize ENDF                          */

    P92 = 0;                                            /* Initialize P92                           */

    SYSCR1 = 0x8F;                                      /* Initialize Function of Subactive Mode 1  */
    SYSCR2 = 0xE8;                                      /* Initialize Function of Subactive Mode 2  */

    TMA = 0x1F;                                         /* Initialize Timer Counter A               */
    TMA = 0x19;                                         /* Initialize Timer A Function              */
    IRRTA = 0;                                          /* Clear IRRTA                              */
    IENTA = 1;                                          /* Timer A Interrupt Enable                 */

    IRRDT = 0;                                          /* Clear IRRDT                              */
    IENDT = 1;                                          /* Direct Transfer Interrupt Enable         */

    set_imask_ccr(0);                                   /* Interrupt Enable                         */

    sleep();                                            /* Transition to Subactive Mode             */

    SYSCR1 = 0x0F;                                      /* Set SYSCR1                               */
    SYSCR2 = 0xE0;                                      /* Set SYSCR2                               */

    do{
        sleep();                                        /* Transion to Subsleep Mode                */
    }while(ENDF ! =  1);                                /* ENDF = "1" ?                             */

    set_imask_ccr(1);                                   /* Interrupt Disable                        */

    SYSCR1 = 0x87;                                      /* Initialize Function of Active Mode 1     */
    SYSCR2 = 0xE8;                                      /* Initialize Function of Active Mode 2     */

    set_imask_ccr(0);                                   /* Interrupt Enable                         */
    sleep();                                            /* Transition to Active Mode                */
    set_imask_ccr(1);                                   /* Interrupt Disable                        */
    IENDT = 0;                                          /* Direct Transfer Interrupt Enable         */

    while(1){
        ;
    }
}
```

```
/*****************************************************************************************************************/
/*  Timer A Interrupt                                                                                            */
/*****************************************************************************************************************/
void    taint ( void )
{
    IRRTA = 0;                                          /* Clear IRRTA                              */

    if(LDONF == 1){                                     /* LDONF = "1" ?                            */
        P92 = 0;                                        /* Turn Off LED                             */
        LDONF = 0;                                      /* Clear LDONF                              */
    }
    else{
        P92 = 1;                                        /* Turn On LED                              */
        LDONF = 1;                                      /* Set LDONF                                */
    }

    if(IACTF == 1){                                     /* IACTF = "1" ?                            */
        counter_a--;                                    /* Decrement 8bit Timer A Interrupt Counter */
        if(counter_a == 0x00){                          /* 8bit Timer A Interrupt Counter = H'00 ?  */
            IENTA = 0;                                  /* Timer A Interrupt Disable                */
            ENDF = 1;                                   /* Set ENDF                                 */
        }
    }

    IACTF = ~IACTF;                                     /* Invert IACTF                             */
}

/*****************************************************************************************************************/
/*  Direct Transfer Interrupt                                                                                    */
/*****************************************************************************************************************/
void    dtint ( void )
{
    IRRDT = 0;                                          /* Clear IRRDT                              */
}
```

Link address specifications

Section Name	Address
CV1	H'0000
CV2	H'001A
CV3	H'0026
P	H'0100
B	H'FB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Dec.19.03	—	First edition issued

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.