code should return to its expected range and the event can be recorded as a SEFI. If the ADC output code does not return to the expected range after these steps, the ADC may have permanent damage.

3. Alternate FPGA Method

Alternatively, an FPGA can be used to collect and observe the SAR ADC output data. While the exact implementation is a little different, the algorithm itself uses the same method to identify and collect the SET data. When using an FPGA, there is no need to have a CPLD to perform the serial to parallel conversion of the data. Instead, the serial data output from the ADC can be converted to parallel data within the FPGA where it can be analyzed for SET. In this case, the FPGA would need to monitor the sample data for SET and only push the samples exhibiting SET to an on-board memory such as a RAM (Random Access Memory). There should be a method to allow for time stamping the SET event so that consecutive SET events can be detected. This could be achieved using something such as an internal counter and recording the count value along with each SET event. Like the maximum count value in the logic analyzer, the FPGA can be programmed for a maximum number of SET. When the maximum number is reached, the FPGA would exit the test routine and push the SET data to a memory. The data from the memory could then be pushed to a computer where software can be used to process the data. This separate software would perform post-processing of the data to determine the number and magnitude of single and multiple sample events. At the completion of each test, the ADC should be read to detect any potential SEFIs in a similar manner to the logic analyzer method. The final data can then be used to generate Weibull fit curves.

4. Summary

A test algorithm has been presented that provides detection of SET and SEFI for precision SAR ADCs. This test algorithm offers the user detection of single sample transient events, multiple sample transient events, and SEFI. The ADC is operated in a manner during SEE test to allow for both positive and negative excursions of the digital output codes. This test method exercises and observes the full range of the ADC to mimic the experience of a real application. The results of testing with this method allow for the heavy ion performance of the ADC to be projected in an application by plotting the Weibull fit curves for the saturation cross section and using the CRÈME96 model for the appropriate orbit.

4.1 Next Steps

Visit the Rad Hard Data Converters page.

5. Revision History

Revision	Date	Description
1.00	Nov 4, 2022	Initial release.