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April 1st, 2010
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H8SX Family

Transfer of Longword Data to Odd Addresses—DMAC Edition

Introduction

Data in memory are accessible to an H8SX CPU as words or longwords. Data thus accessed can be allocated to any address, regardless of whether it is odd or even. The DMAC is capable of operating in the same way.

In the example given in this application note, the DMAC is used to transfer longword data, altering the boundaries to odd addresses from even addresses.

Target Device

H8SX/1653F

Contents

1. Specification

Data in memory are accessible to an H8SX CPU as words or longwords. Data thus accessed can be allocated to any address, regardless of whether it is odd or even.

The DMAC is used to transfer data allocated to odd addresses. When an H8SX MCU transfers data allocated to odd addresses as the boundary in memory, the user doesn't have to think about the operation since the hardware handles boundary-related control.

1. The DMAC is used to transfer data from the on-chip ROM area to the on-chip RAM area.
2. Data in the on-chip ROM are allocated to even addresses as the longword boundaries, and the on-chip RAM area is set to odd addresses.
3. Data access size is set to longword and the transfer mode is set to block transfer, then four longwords (16 bytes) of data are transferred.

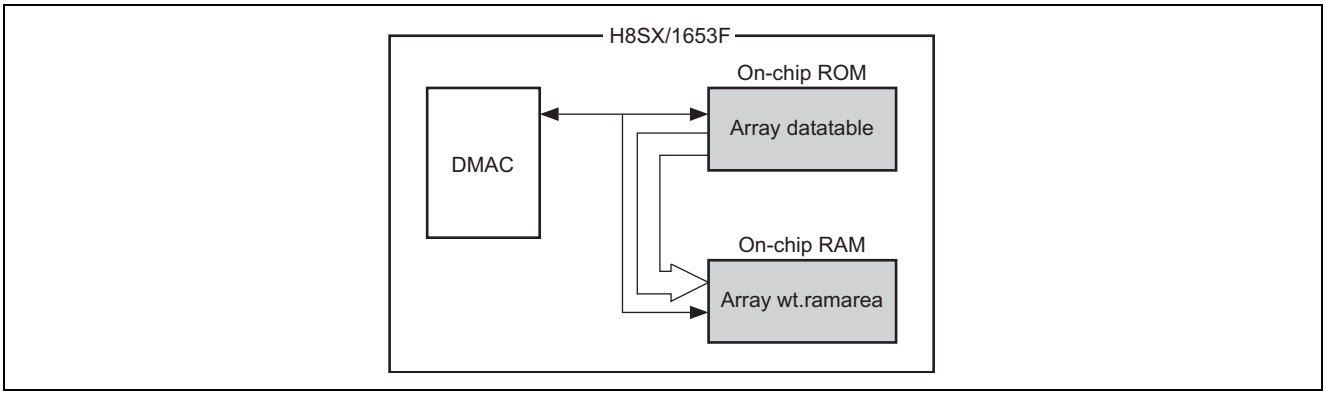


Figure 1 DMAC Transfer of Data Allocated to Odd Addresses

Table 1 DMA Transfer Settings

Item	Setting
DMA transfer request	Auto request mode
Bus mode	Cycle stealing
Transfer mode	Block transfer
Address mode	Dual address
Transfer size	Longword

2. Applicable Conditions

Table 2 Applicable Condition

Item	Details
Operating frequency	Input clock: 12 MHz System clock (Iϕ): 48 MHz Peripheral module clock (Pϕ): 24 MHz External bus clock (Bϕ): 48 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)

3. Description of Functions Used

Figure 2 shows a block diagram of the DMAC. The block diagram is explained below.

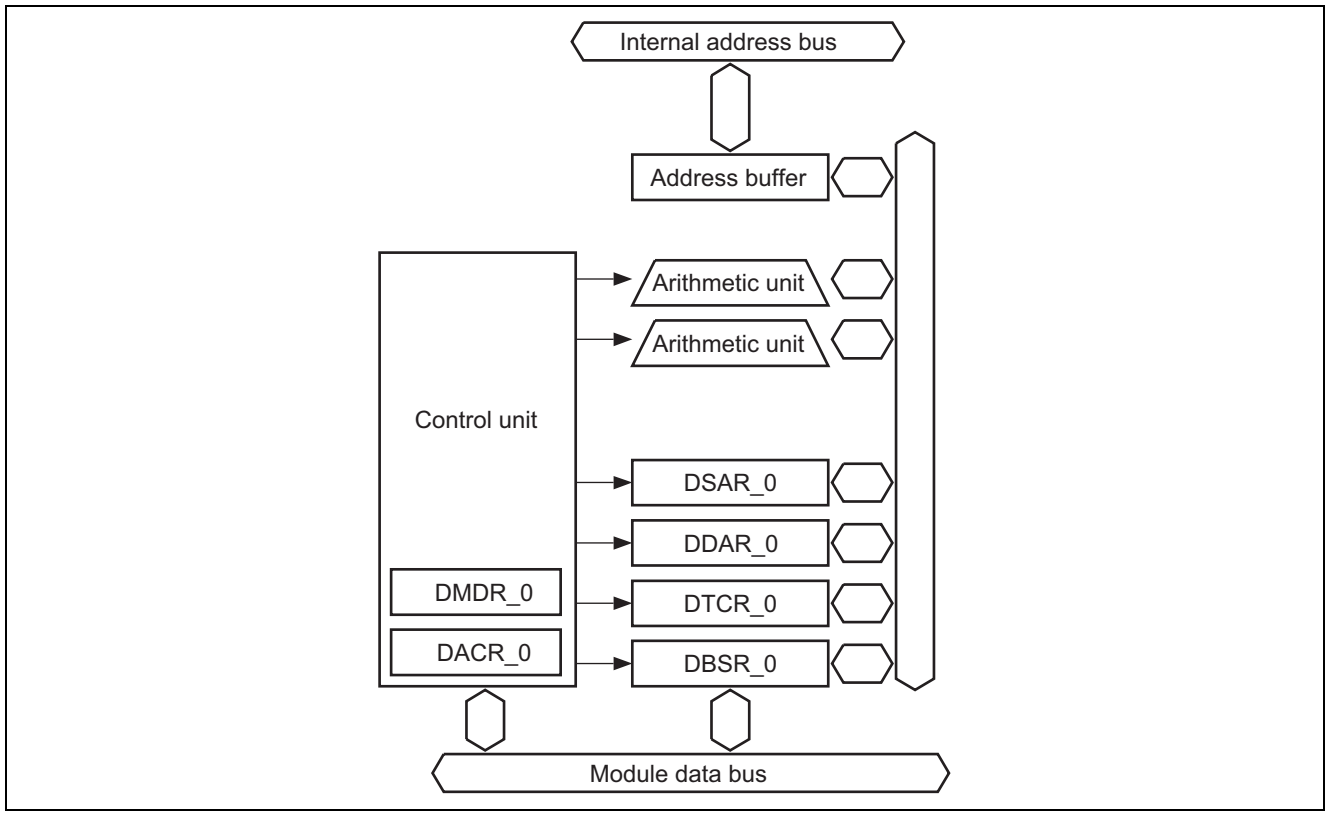


Figure 2 Block Diagram of DMAC

- DMA source address register_0 (DSAR_0)
  DSAR_0 is a 32-bit readable/writable register that specifies the transfer source address. DSAR_0 has an address updating function, and is thus updated to the next transfer source address after each data transfer.
- DMA destination address register_0 (DDAR_0)
  DDAR_0 is a 32-bit readable/writable register that specifies the transfer destination address. DDAR_0 has an address updating function, and is thus updated to the next transfer destination address after each data transfer.
- DMA transfer count register_0 (DTCR_0)
  DTCR_0 is a 32-bit readable/writable register that specifies the amount of data to be transferred (the total amount) in bytes. The value is decremented in accord with the transferred data access size after each data transfer. In this sample task, this register is set to 16 bytes and the data access size is set to longword. DTCR_0 is thus decremented by 4 per transfer while the DMA is operating, so that it shows the remaining amount to be transferred.
- DMA block size register_0 (DBSR_0)
  DBSR_0 is valid in repeat transfer mode and block transfer mode, and is used to set the repeat size and block size. This register is invalid in normal mode. In this sample task, operation is in block transfer mode, and the block size is set to four longwords (16 bytes).
- DMA mode control register_0 (DMDR_0)
  DMDR_0 controls DMAC operation.
- DMA address control register_0 (DACR_0)
  DACR_0 specifies the operating mode, method of transfer, etc.

4. Principle of Operation

4.1 Example of Data Transfer to Odd Addresses

Figure 3 is a schematic view of the data transfer to odd addresses. Four longwords (16 bytes) of data are transferred from H'003000 to H'FF2001 by longword access in block transfer mode.

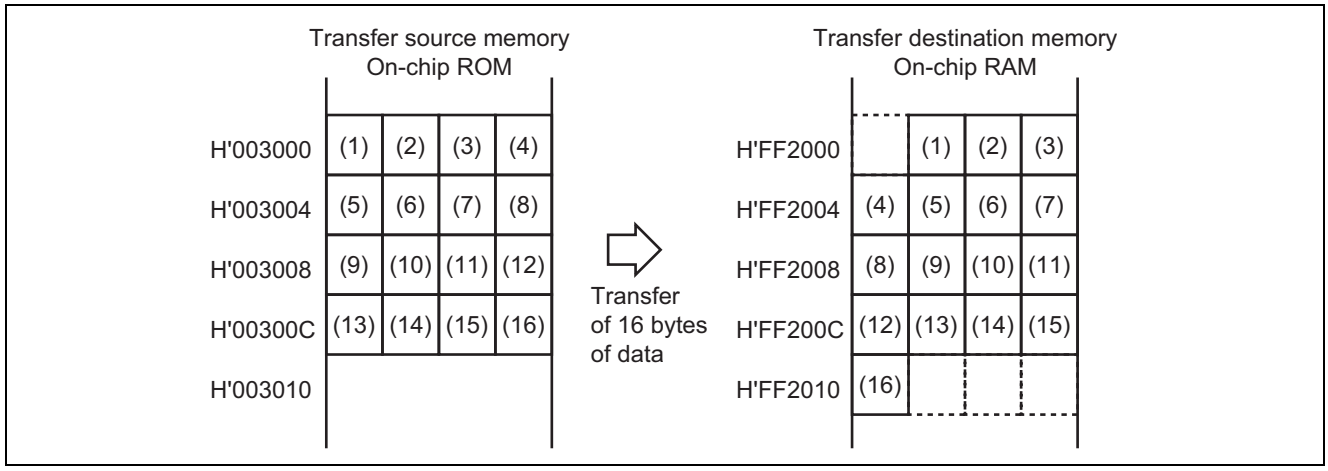


Figure 3 Example of Data Transfer to Odd Addresses

4.2 Timing of Data Transfer to Odd Addresses

Figure 4 is a timing chart for the data transfer to odd addresses. Data in on-chip ROM allocated to an address aligned with a longword boundary are read in one cycle of longword access, then written to an odd address in on-chip RAM in a total of three cycles, for byte, word, and byte access.

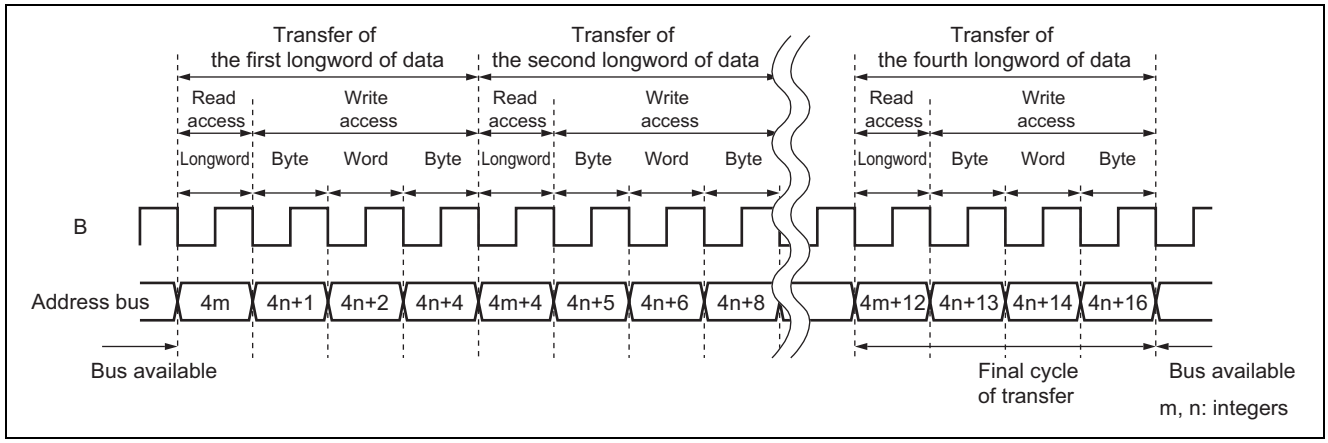


Figure 4 Timing of Data Transfer to Odd Addresses

5. Description of Software

5.1 Operating Environment

Table 3 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Version 4.00.03
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Ver.6.01.01 (manufactured by Renesas Technology)
H8SX compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)

Table 4 Setting of Sections

Address	Section	Description
H'001000	P	Program area
H'003000	C	Data table Array datatable is allocated here.
H'FF2000	B	Non-initialized data area (RAM area) The wt structure is allocated here.

Table 5 Interrupt and Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Reset	0	H'000000	init

5.2 List of Functions

Table 6 List of Functions

Function Name	Functions
init	Initialization routine Sets the CCR and configures the clocks, releases the required modules from module stop mode, and calls the main function.
main	Main routine Makes settings for the DMAC block transfer mode and enabling transfer.

5.3 RAM Usage

Table 7 RAM Usage

Type	Variable Name	Description	Used in
unsigned char	wt.dummy	wt structure This dummy variable is used to set wt.ramarea to an odd address.	main
unsigned char	wt.ramarea[16]	wt structure Transfer destination area in RAM	main

5.4 Constants

Table 8 Constants

Type	Variable Name	Setting	Description	Used in
unsigned long	datatable[4]	H'00010203, H'04050607, H'08090A0B, H'0C0D0E0F	Holds source data for transfer.	main

5.5 Description of Functions

5.5.1 init Function

1. Functional overview

Initialization routine which releases the required modules from module stop mode, makes clock settings, and calls the main function.

2. Argument

None

3. Return value

None

4. Description of internal registers

The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
11	MDS3	Undefined*	R	Mode Select 3 to 0
10	MDS2	Undefined*	R	These bits indicate the operating mode selected by the mode pins (MD2 to MD0) (see table 9). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latches are released by a reset.
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Determined by pins MD3 to MD0.

Table 9 Settings of Bits MDS3 to MDS0

MCU Operating Mode	Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock signal, which is provided to the CPU, DMAC, and DTC.
8	ICK0	0	R/W	000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit to 1 places the corresponding module in module stop mode, while clearing the bit to 0 releases the module from module stop mode.
- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable This bit enables/disables all-module-clock-stop mode for reducing current consumption by stopping the bus controller and I/O port operation when the CPU executes the SLEEP instruction after module stop mode has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	0	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

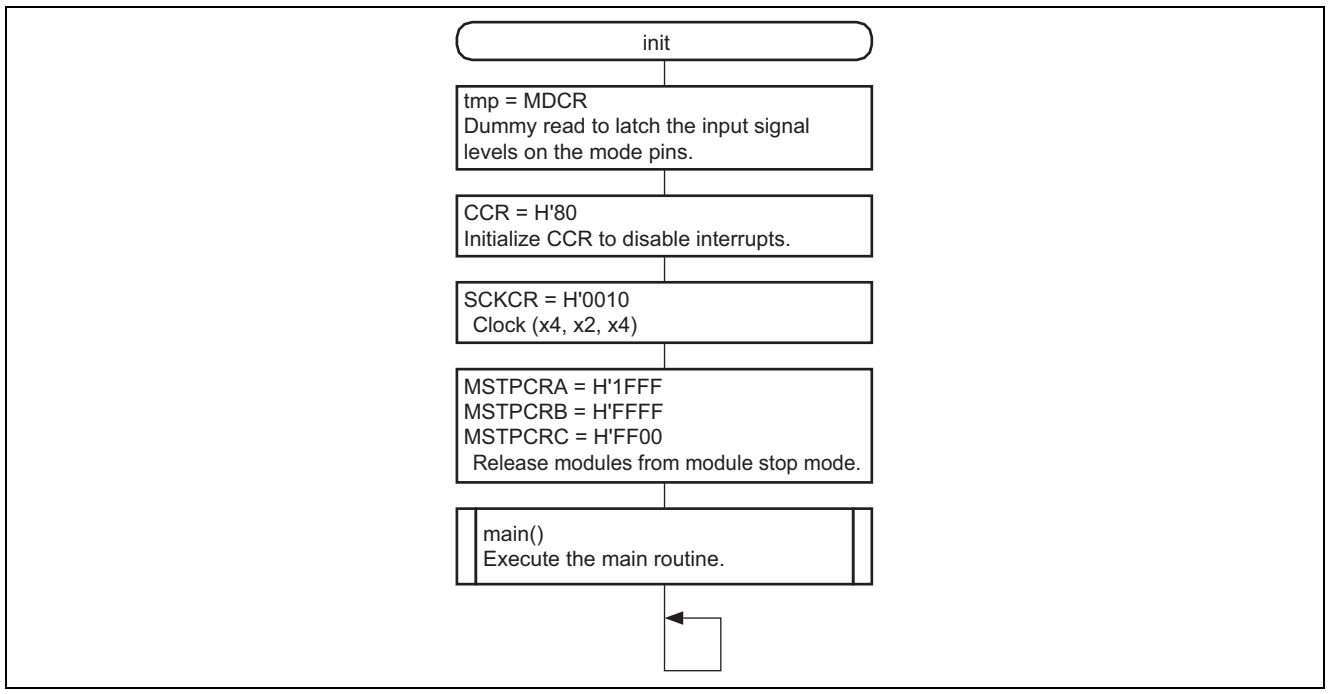
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communication interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communication interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communication interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communication interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communication interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check module
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart


init
tmp = MDCR
Dummy read to latch the input signal levels on the mode pins.
CCR = H'80
Initialize CCR to disable interrupts.
SCKCR = H'0010
Clock (x4, x2, x4)
MSTPCRA = H'1FFF
MSTPCRB = H'FFFF
MSTPCRC = H'FF00
Release modules from module stop mode.
main()
Execute the main routine.

5.5.2 main Function

1. Functional overview

Main routine which sets up the DMAC for transfer and performs transfer start processing.

2. Argument

None

3. Return value

None

4. Description of internal registers

The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- DMA source address register_0 (DSAR_0) Number of bits: 32 Address: H'FFFC00

Function: Setting the transfer source address
Setting: datatable

- DMA destination address register_0 (DDAR_0) Number of bits: 32 Address: H'FFFC04

Function: Setting the transfer destination address
Setting: wt.ramarea

- DMA transfer count register_0 (DTCR_0) Number of bits: 32 Address: H'FFFC0C

Function: Setting the amount of data for transfer
Setting: 16

- DMA block size regiser_0 (DBSR_0) Number of bits: 32 Address: H’FFFC10

Function: Setting the block size when data are to be transferred in block transfer mode. When DBSR_0=H’00040004, the block size is four longwords (16 bytes) of data
Setting: H’00040004

- DMA mode control register_0 (DMDR_0) Number of bits: 32 Address: H'FFFC14

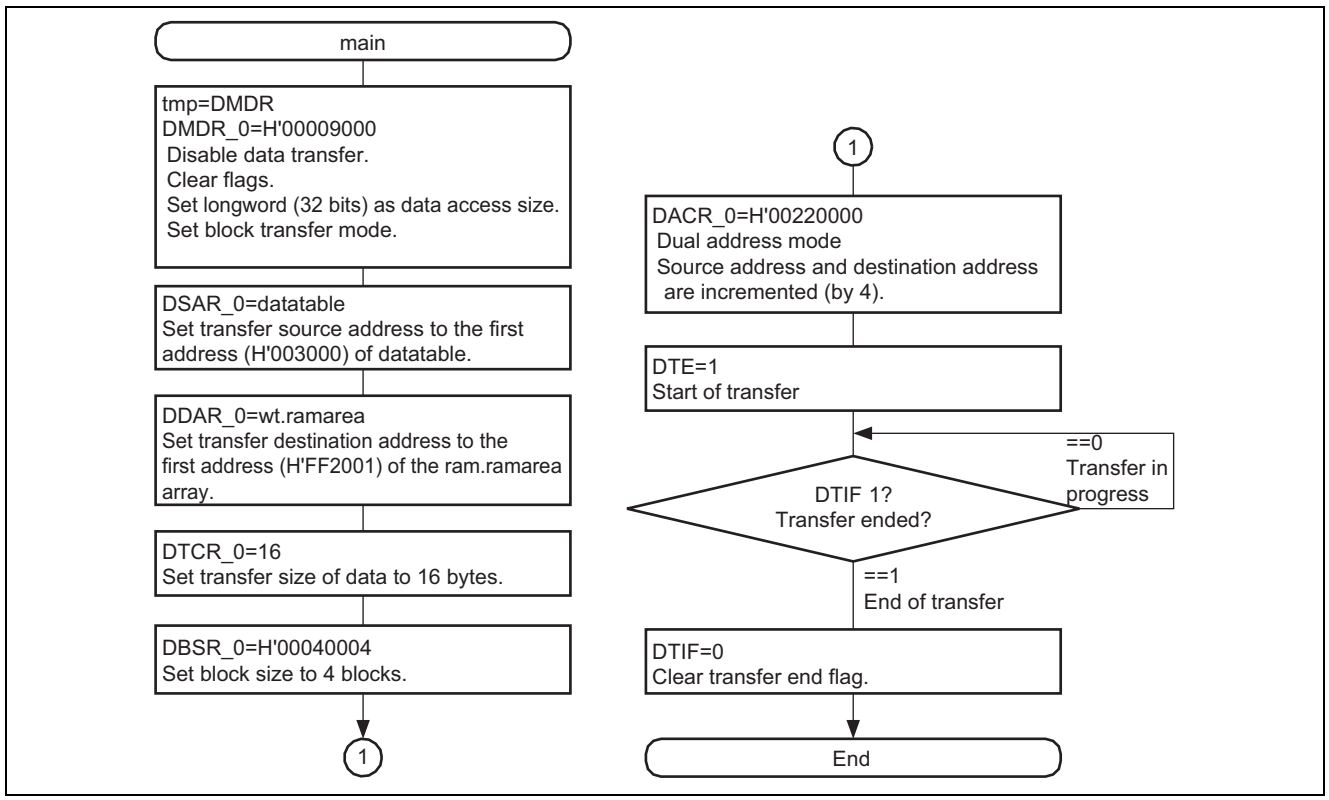
Bit	Bit Name	Setting	R/W	Description
31	DTE	0/1	R/W	Data Transfer Enable 0: Disables data transfer. 1: Enables data transfer.
26	NRD	0	R/W	Next Request Delay 0: Starts accepting the next transfer request after completion of the current transfer. 1: Starts accepting the next transfer request one cycle after completion of the current transfer.
16	DTIF	0	R/(W)*	Data Transfer Interrupt Flag 0: The transfer counter has not requested a transfer end interrupt. 1: The transfer counter has requested a transfer end interrupt.
15	DTSZ1	1	R/W	Data Access Size 1 and 0
14	DTSZ0	0	R/W	10: Access size of data to be transferred is longword (32 bits)
13	MDS1	0	R/W	Transfer Mode Select 1 and 0
12	MDS0	1	R/W	01: Set to block transfer mode.
9	ESIE	0	R/W	Transfer Escape Interrupt Enable 0: Disables transfer escape end interrupts. 1: Enables transfer escape end interrupts.
8	DTIE	0	R/W	Data Transfer End Interrupt Enable 0: Disables transfer end interrupts by the transfer counter. 1: Enables transfer end interrupts by the transfer counter.
7	DTF1	0	R/W	Data Transfer Factors 1 and 0
6	DTF0	0	R/W	00: The DMAC activation source is the automatic request (cycle stealing).

Note: * Only 0 can be written to this bit after having been read as 1, to clear the flag.

- DMA address control register_0 (DACR_0) Number of bits: 32 Address: H'FFFC18

Bit	Bit Name	Setting	R/W	Description
31	AMS	0	R/W	Address Mode Select 0: Dual address mode 1: Single address mode
26	RPTIE	1	R/W	Repeat Size End Interrupt Enable 0: Disables repeat size end interrupts. 1: Enables repeat size end interrupts.
25	ARS1	0	R/W	Area Select 1 and 2
24	ARS0	0	R/W	00: The block area in block transfer mode is specified for the source side.
21	SAT1	1	R/W	Source Address Update Mode 1 and 0
20	SAT0	0	R/W	10: Source address is updated by adding 4 when data access size is longword.
17	DAT1	1	R/W	Destination Address Update Mode 1 and 0
16	DAT0	0	R/W	10: Destination address is updated by adding 4 when data access size is longword.

5. Flowchart


main
tmp=DMDR
DMDR_0=H'00009000
Disable data transfer.
Clear flags.
Set longword (32 bits) as data access size.
Set block transfer mode.
DSAR_0=datatable
Set transfer source address to the first address (H'003000) of datatable.
DDAR_0=wt.ramarea
Set transfer destination address to the first address (H'FF2001) of the ram.ramarea array.
DTCR_0=16
Set transfer size of data to 16 bytes.
DBSR_0=H'00040004
Set block size to 4 blocks.
1
1
DACR_0=H'00220000
Dual address mode
Source address and destination address are incremented (by 4).
DTE=1
Start of transfer
DTIF 1?
Transfer ended?
==0
Transfer in progress
==1
End of transfer
DTIF=0
Clear transfer end flag.
End

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