To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

H8SX Family

Transfer between Synchronous DRAM and External SRAM with EXDMAC (Extended Repeat Area Function)

Introduction

The extended repeat area function of the EXDMAC in normal transfer mode is used to transfer data from the synchronous DRAM area (hereafter referred to as SDRAM) to the SRAM area.

The EXDMAC can be used to transfer data between external memories, reducing the load on the CPU.

Furthermore, with the extended repeat area function, values of the higher-order bits in the transfer address register are fixed, and values of the lower-order bits are incremented or decremented so that data can be transferred for repeated address values in a specified range.

Target Device

H8SX/1668R

Preface

The writing of this application note is in accord with the hardware manual for the H8SX/1668R Group, and the program covered herein can be run on the target device indicated above. However, since some functional modules may be changed for the addition of functionality, etc., be sure to perform a thorough evaluation by confirming the details with the hardware manual for the target device.

Contents

1. Specifications

An overview of operation in this application note is given in figure 1, and connections between the external memory and the CPU are shown in figure 2.

The operation in this application note is explained as follows:

- EXDMAC is activated on the falling edge of the $\overline{\text{EDREQ}}$ pin.
- TPU compare match output is used as the input to the $\overline{\text{EDREQ}}$ pin.
- The transfer source is specified as extended repeat area function (the three lower-order bits (8-byte area) of transfer source address are designated as extended repeat area).
- EXDMAC transfers 256-byte data from the SDRAM area to the SRAM area.
- SDRAM and SRAM use area 2 and area 4, respectively.
- After an EXDMAC transfer, the source and destination data are compared, and the result of the comparison is output to an I/O port.

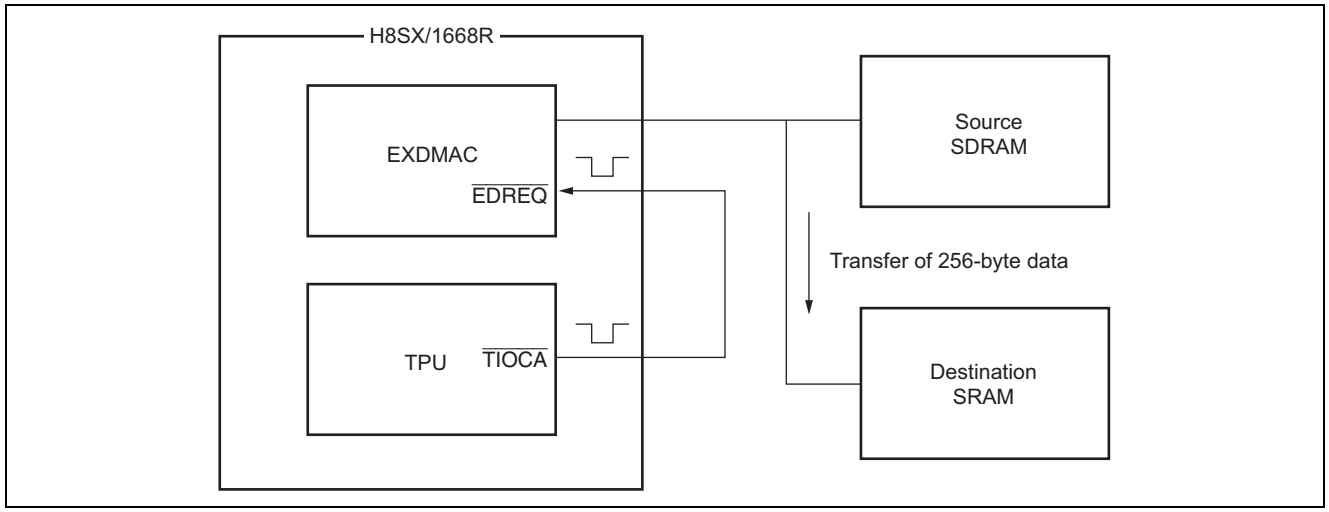

Figure 1 Overview of Operation

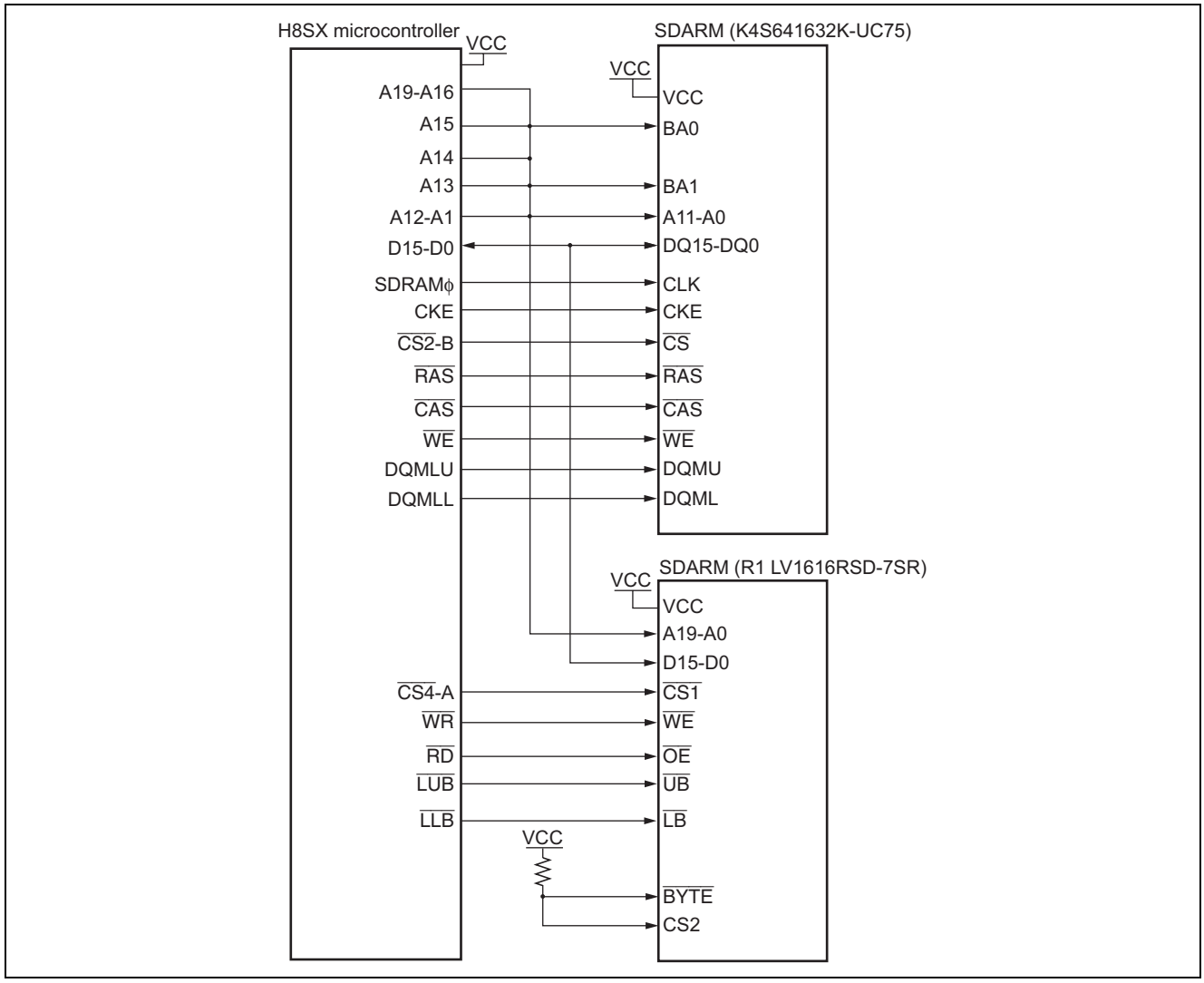

Figure 2 Connections between External Memory and CPU

EXDMAC transfer settings are listed in table 1.

In addition, comparison of data transferred is listed in table 2.

Table 1 EXDMAC Transfer Settings

Item	Setting
EXDMAC transfer request	External request mode
Bus mode	Cycle stealing mode
Transfer mode	Normal transfer mode
Address mode	Dual address mode
Transfer size	Byte
Source/destination address update	Incremented according to the data access size
Extended repeat area	Source addresses

Table 2 Comparison of Data Transferred

Comparison Result	Output Value (using port 3)
Matched	H'55
Unmatched	H'FF

2. Applicable Conditions

Table 3 Applicable Conditions

Item	Detail	
Operation frequency	Input clock	: 12.5 MHz
	System clock (Iϕ)	: 50 MHz (12.5 MHz multiplied by 4)
	Peripheral module clock (Pϕ)	: 25 MHz (12.5 MHz multiplied by 2)
	External bus clock (Bϕ)	: 50 MHz (12.5 MHz multiplied by 4)
Operation voltage	3.3 V	
Operation mode	Mode 6 (MD3 = 1, MD2 = 1, MD1 = 1, MD0 = 0, MD_CLK = 0)	
External memory	• SDRAM (area 2)	: K4S641632K-UC75
	• SRAM (area 4)	: R1LV1616RSD-7SR
Development tool	High-performance Embedded Workshop (HEW) Ver.4.03.00	
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Ver.6.01.03 from Renesas Technology	
Compiler options	-cpu = H8SXA:24MD, -optimize = 1	
Linker options	start = PResetPRG, PIntPRG/0400, P, C$DSEC, C$BSEC, D/0800, B, R/0FF2000, S/0FFBE00	

Table 4 SDRAM Specifications

Item	Detail
Product name	K4S641632K-UC75 (Samsung Electronics Corp.)
Configuration	1 Mword × 16 bits × 4 banks
Capacity	64 Mbits
CAS latency	2/3 (programmable)
Refresh interval	4,096 refresh cycles per 64 ms
Row address	A11 to A0
Column address	A7 to A0
Number of banks	Four banks for operation controlled by BA0 and BA1.

Table 5 SRAM Specifications

Item	Detail
Product name	R1LV1616RSD-7SR (Renesas Technology Corp.)
Configuration	1 Mword × 16 bits
Capacity	16 Mbits

Note: The upper 1 Mbyte of SRAM is used for this application note (because 1 Mbyte is the maximum space in area 4).

Table 6 SDRAM Mode Settings

Item	Setting
Operation code (OPCODE)	Burst read/single write
CAS latency (LMODE)	2
Burst type (BT)	Sequential
Burst length (BL)	1
SDRAM access address	H'400440

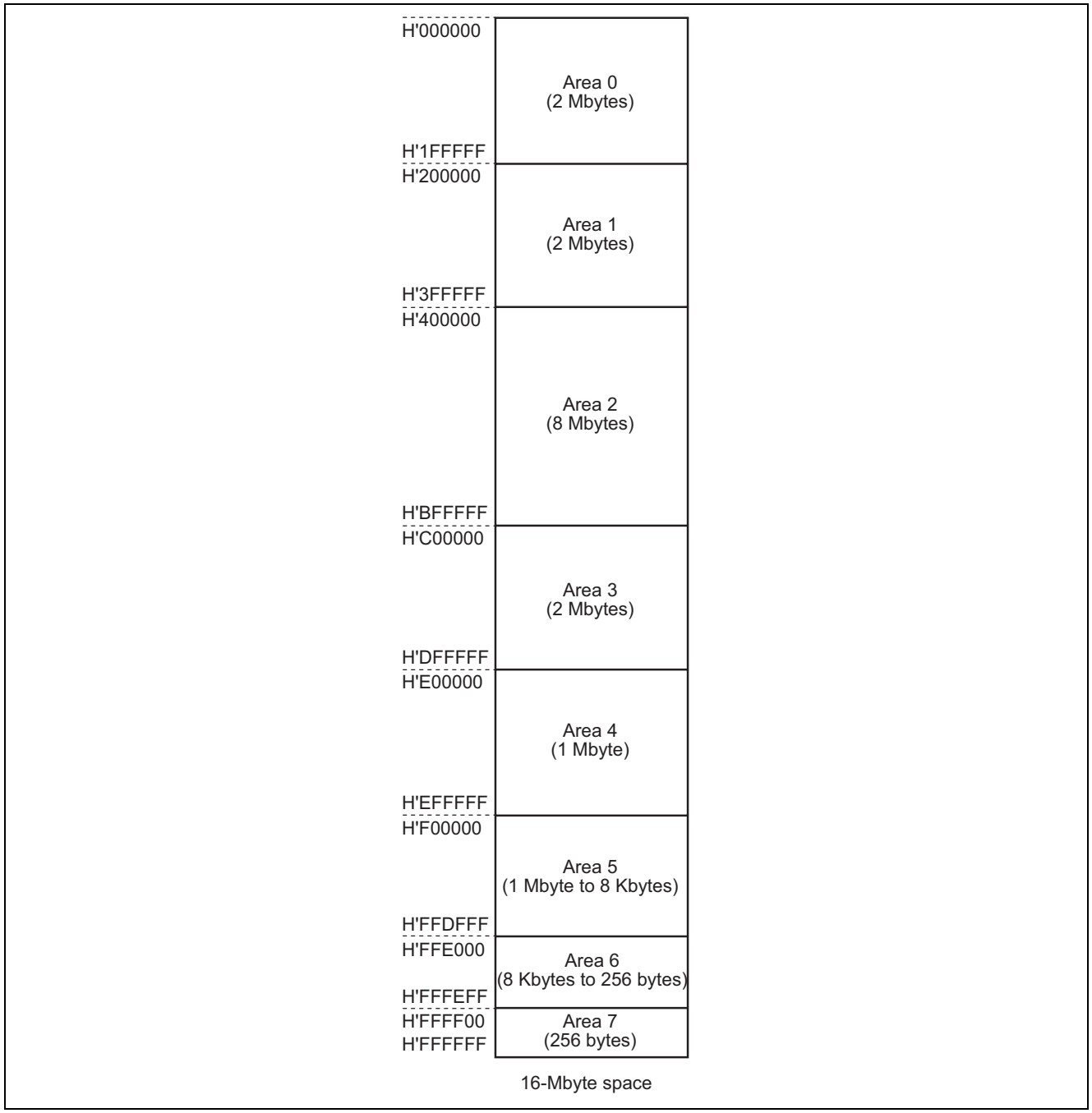

Figure 3 Address Space Area Division

3. Description of Modules Used

3.1 Normal Transfer Mode

In normal transfer mode, data are transferred in one-data access size units in response to each transfer request. Total transfer size can be set up to 4 Gbytes in the EXDMA transfer count register (EDTCR).

Examples of timing and operation in this mode are shown in figure 4 and figure 5, respectively.

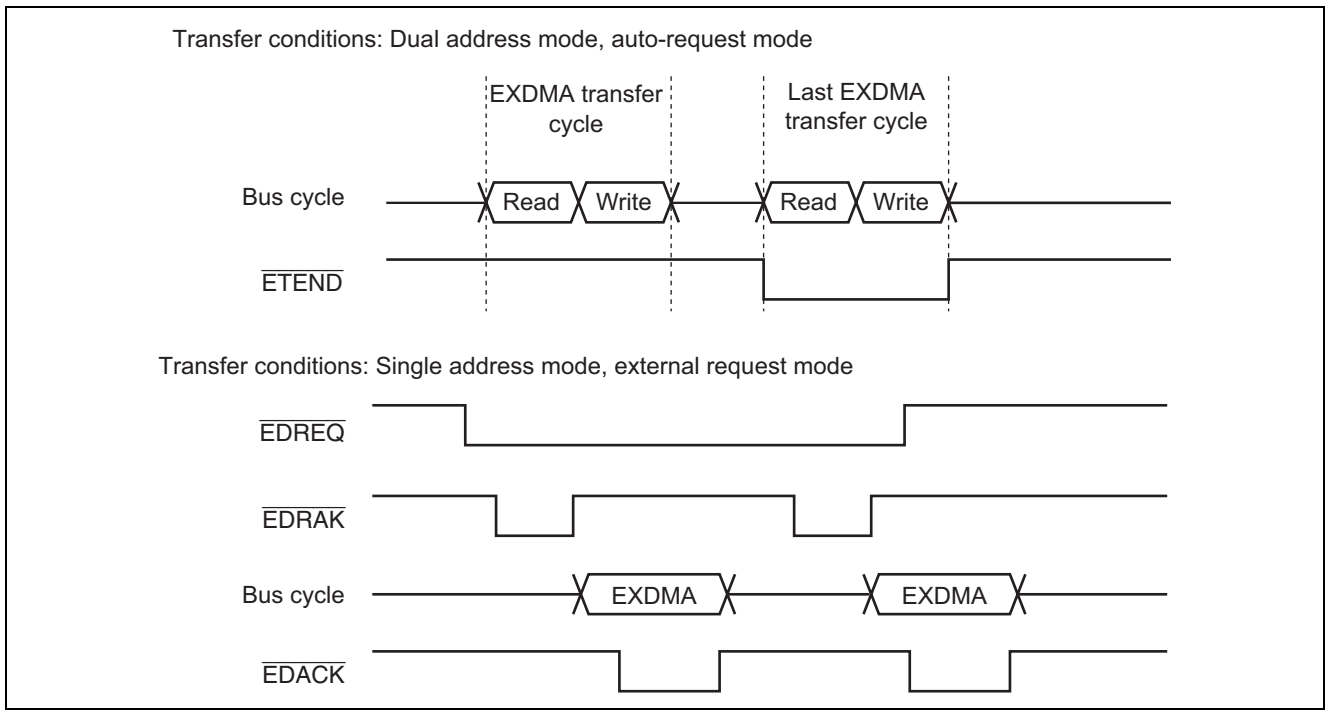

Figure 4 Example of Timing in Normal Transfer Mode

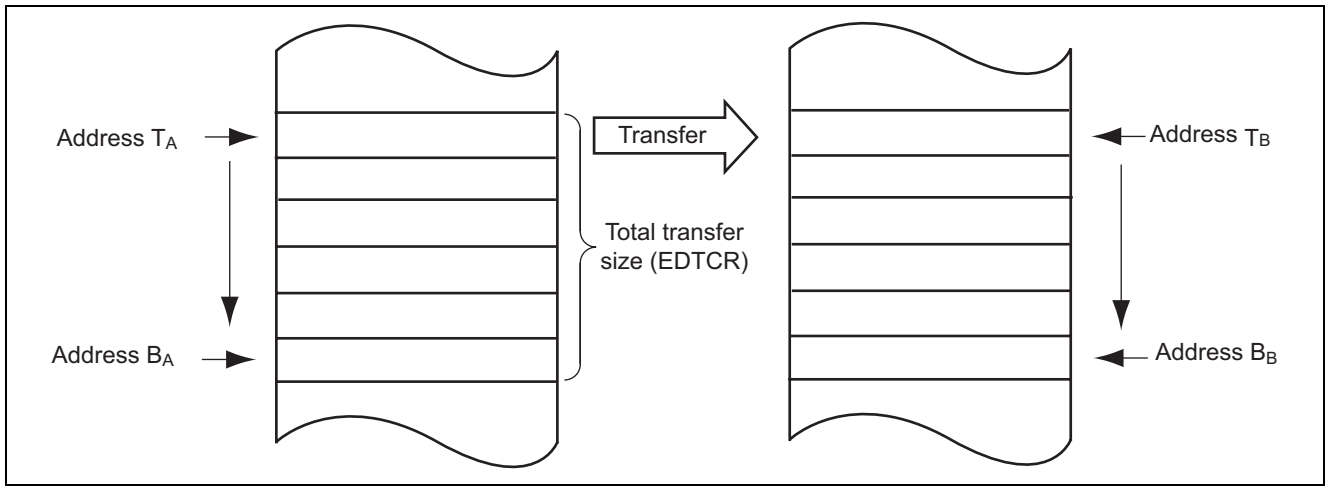

Figure 5 Example of Operation in Normal Transfer Mode

3.2 Extended Repeat Area Function

The EXDMAC has a function for designating an extended repeat area for source addresses and/or destination addresses. When an extended repeat area is designated, the address register values repeat within the range specified as the extended repeat area. Normally, when a ring buffer is involved in a transfer, an operation is required to restore the address register value to the buffer start address each time the address register value becomes the last address in the buffer (i.e. when ring buffer address overflow occurs). However, if the extended repeat area function is used, the operation that restores the address register value to the buffer start address is processed automatically within the EXDMAC.

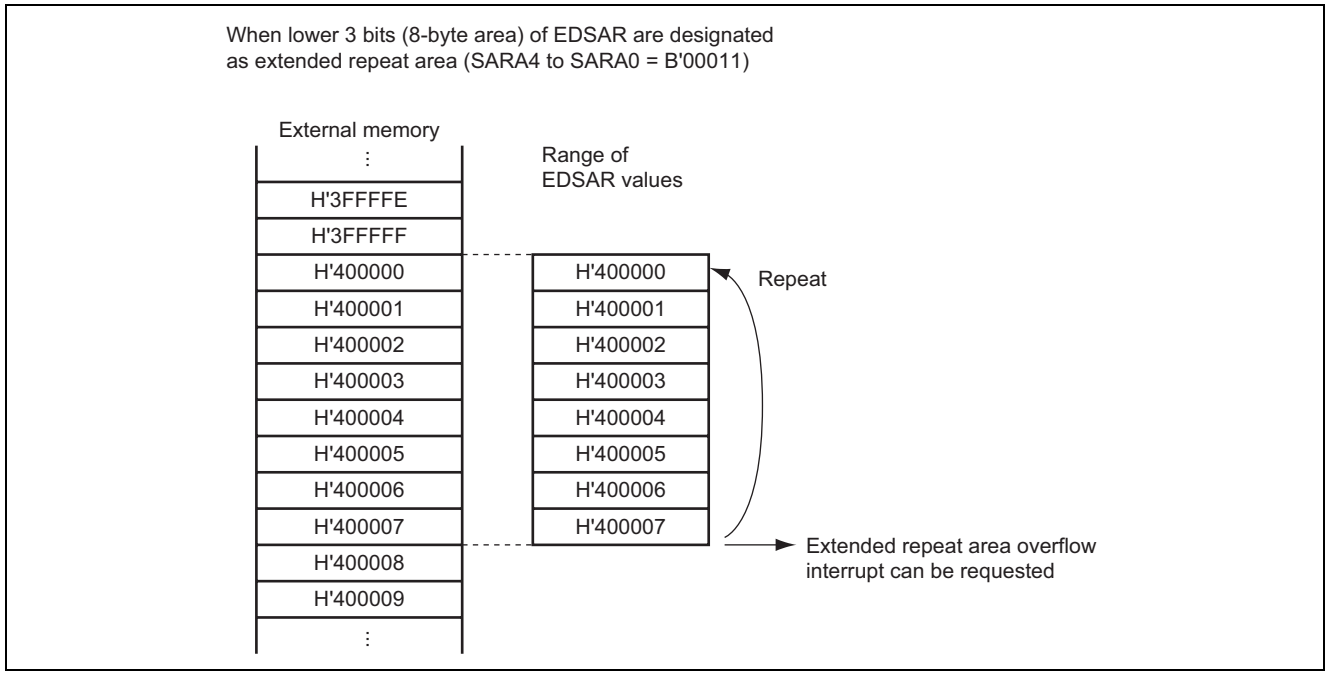

Figure 6 Example of Extended Repeat Area Function Operation

4. Principle of Operation

Operation in this application note is shown in figure 7.

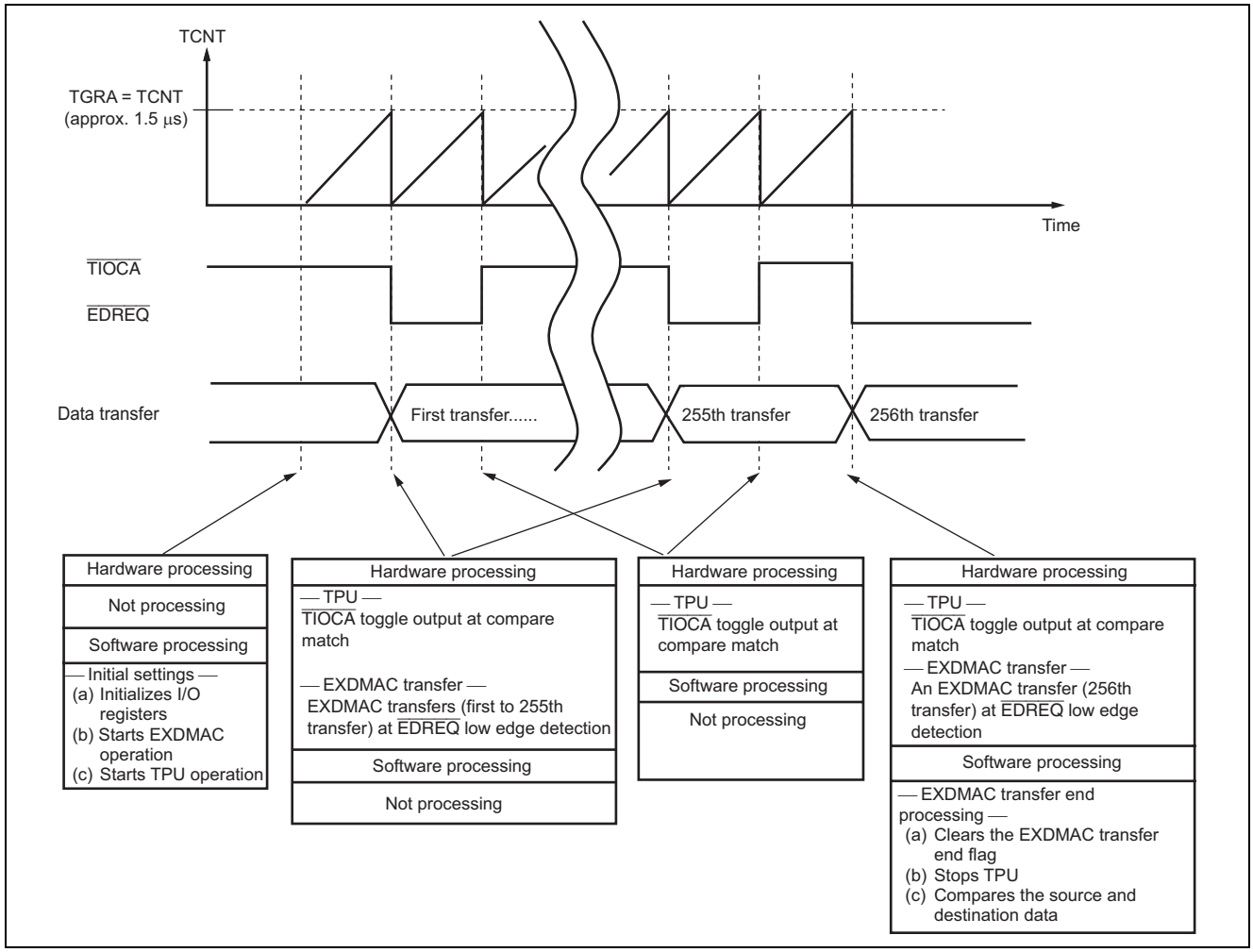

Figure 7 Operation

5. Description of Software

5.1 List of Functions

Table 7 List of Functions

Function Name	Description
main	• Main routine Calls functions of init and cmp_data, sets operations of EXDMAC and TPU, and judges whether an EXDMAC transfer is ended.
init	• Initialization routine Initializes registers and memory areas to be used, and sets data in the EXDMAC transfer source area.
cmp_data	• Transfer data compare routine Compares the source and destination data

5.2 Description of Functions

5.2.1 main Function

1. Functional overview
   The main function initializes registers and RAM by calling function init, and operates the EXDMAC and TPU. After the end of transfer by the EXDMAC, it calls function cmp_data to compare the transfer source data with the transfer destination data.
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- EXDMA mode control register (EDMDR) Number of bits: 32 Address: H'FFFC94

Bit	Bit Name	Setting Value	R/W	Description
31	DTE	1	R/W	Data Transfer Enable Enables or disables data transfer on the corresponding channel. When this bit is set to 1, this indicates that an EXDMA operation is in operation. With external requests, transfer processing begins when a transfer request is issued after this bit has been set to 1. 1: Data transfer enabled (during an EXDMA operation)
16	DTIF	0	R/W	Data Transfer Interrupt Flag Flag indicating that a transfer end interrupt request has occurred by the transfer counter. 0: Transfer end interrupt request is not generated by the transfer counter

- Timer start register (TSTR) Number of bits: 8 Address: H'FFFFBC

Bit	Bit Name	Setting Value	R/W	Description
0	CST0	1	R/W	Counter Start 0 Selects operation or stoppage for TCNT. 1: TCNT_0 performs count operation

5. Flowchart

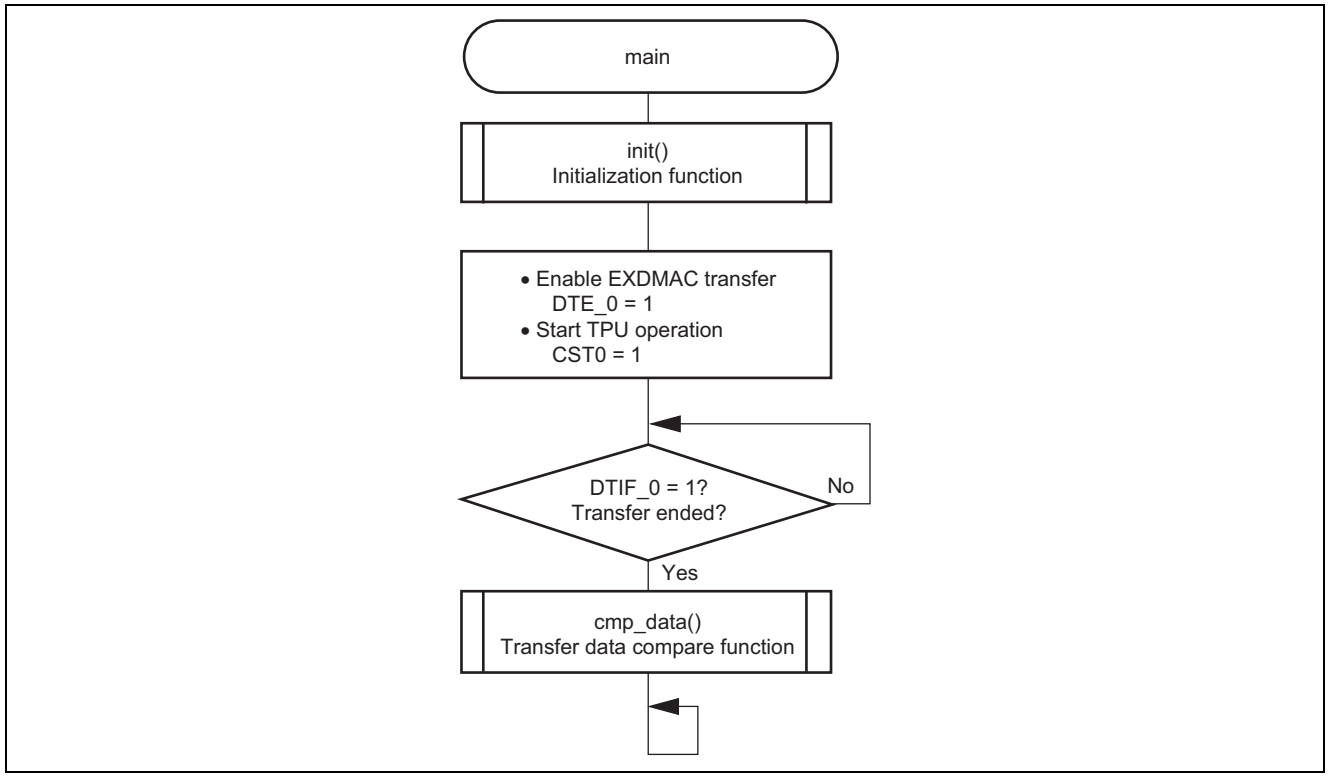

Figure 8 Flowchart (main)

5.2.2 init Function

1. Functional overview
   The init function initializes I/O registers and memory, and sets transfer source data.
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting Value	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0		Select the frequency of the system clock and the clock provided
8	ICK0	0		to the CPU, EXDMAC, DMAC, and DTC.
				000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0		Select the frequency of the peripheral module clock.
4	PCK0	1		001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0		Select the frequency of the external bus clock.
0	BCK0	0		000: Input clock × 4

- MSTPCRA controls module stop mode. Setting a bit to 1 makes the corresponding module enter the stop mode, while clearing the bit to 0 makes the module exit the stop mode.

- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting Value	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current consumption after the bus controller and I/O ports operation stop when the CPU executes the SLEEP instruction after all the on-chip peripheral modules controlled by MSTPCR has entered module stop mode 0: All-module-clock-stop mode disabled
14	MSTPA14	0	R/W	EXDMA controller (EXDMAC)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

- Bus width control register (ABWCR) Number of bits: 16 Address: H'FFFD84

Bit	Bit Name	Setting Value	R/W	Description
12	ABWH4	0	R/W	Area 7 to 0 Bus Width Control
10	ABWH2	0		Select whether the corresponding area is to be designated as
4	ABWL4	1		8-bit access space or 16-bit access space.
2	ABWL2	1		ABWHn ABWLn (n = 7 to 0)
				0 1: Area n is designated as 16-bit access space

- Access state control register (ASTCR) Number of bits: 16 Address: H'FFFD86

Bit	Bit Name	Setting Value	R/W	Description
12	AST4	1	R/W	Select whether the corresponding area is to be designated as 2- or 3-state access space. 1: Area n is designated as 3-state access space
10	AST2	1		

- Wait control register A (WTCRA) Number of bits: 16 Address: H'FFFD88

Bit	Bit Name	Setting Value	R/W	Description
2	W42	1	R/W	Area 4 Wait Control 2 to 0 Select the number of program wait cycles when accessing area 4. 111: 7 program wait cycles inserted
1	W41	1		
0	W40	1		

- Wait control register B (WTCRB) Number of bits: 16 Address: H'FFFD8A

Bit	Bit Name	Setting Value	R/W	Description
10	W22	0	R/W	Area 2 Wait Control 2 to 0 Select the number of program wait cycles when accessing area 2. When SDRAM is connected, the CAS latency is specified. At this time, W22 is ignored. 01: SDRAM with a CAS latency of 2 is connected.
9	W21	0		
8	W20	1		

- Idle control register (IDLCR) Number of bits: 16 Address: H'FFFD90

Bit	Bit Name	Setting Value	R/W	Description
15 to 12	IDLS2 to 0	0	R/W	Idle Cycle Insertion 3 to 0 Insert an idle cycle between bus cycles 0: No idle cycle is inserted

- Endian control register (ENDIANCR) Number of bits: 8 Address: H'FFFD95

Bit	Bit Name	Setting Value	R/W	Description
4	LE4	0	R/W	Little Endian Select Select the endian for the corresponding area. 0: Big endian
2	LE2	0		

- SRAM mode control register (SRAMCR) Number of bits: 16 Address: H'FFFD98

Bit	Bit Name	Setting Value	R/W	Description
12	BCSEL4	1	R/W	Byte Control SRAM Interface Select Select the bus interface for the corresponding area. 0: Basic bus interface 1: Byte control SRAM interface
10	BCSEL2	0		

- DRAM control register (DRAMCR) Number of bits: 16 Address: H'FFFDA0

Bit	Bit Name	Setting Value	R/W	Description
15	DRAME	1	R/W	Area 2 DRAM Interface Select Selects whether or not area 2 is specified as the DRAM/SDRAM interface. When this bit is set to 1, select the type of DRAM to be used in area 2 with the DTYPE bit. When this bit is set to 1, the BCSEL2 bit in SRAMCR should be set to 0. 1: DRAM/SDRAM interface
14	DTYPE	1	R/W	DRAM select Selects the type of DRAM to be connected to area 2. 1: SDRAM is connected to area 2
11	OEE	1	R/W	$\overline{OE}$ output enable The $\overline{OE}$ signal is output when DRAM with the EDO page mode is connected, whereas the CKE signal is output when SDRAM is connected. 1: $\overline{OE}$/CKE signal enabled
7	BE	1	R/W	Burst Access Enable Enables or disables a burst access to the DRAM/SDRAM. The DRAM/SDRAM is accessed in high-speed page mode. 1: DRAM/SDRAM is accessed in high-speed page mode

- DRAM access control register (DRACCR) Number of bits: 16 Address: H'FFFDA2

Bit	Bit Name	Setting Value	R/W	Description
13	TPC1	0	R/W	Precharge Cycle Control
12	TPC0	0		Select the number of RAS precharge cycles on a normal access and a refresh. 00: One cycle
9	RCD1	0	R/W	$\overline{RAS}$-$\overline{CAS}$ Wait Control
8	RCD0	0		Determine whether to insert wait cycles between $\overline{RAS}$ and $\overline{CAS}$ assert cycles. 00: No wait cycle inserted

- Synchronous DRAM control register (SDCR) Number of bits: 16 Address: H'FFFDA4

Bit	Bit Name	Setting Value	R/W	Description
15	MRSE	0/1	R/W	Mode Register Set Enable Enables the setting in the SDRAM mode register. 0: Disables to set the SDRAM mode register 1: Enables to set the SDRAM mode register

Note: Setting the MRSE bit in SDCR to 1 enables the SDRAM mode register setting to set the SDRAM mode. After this, write to the SDRAM space in bytes.
After write access, clear the MRSE bit to 0 to disable the SDRAM mode setting.

- Refresh control register (REFCR) Number of bits: 16 Address: H'FFFDA6

Bit	Bit Name	Setting Value	R/W	Description
10	RTCK2	0	R/W	Refresh Counter Clock Select
9	RTCK1	1		Select a clock used to count up the refresh counter from the seven internal clocks generated by dividing the on-chip peripheral module clock (Pϕ). When the clock is selected, the refresh counter starts to count up.
8	RTCK0	0		010: Counts on Pϕ/8
7	RFSHE	1	R/W	Refresh Control Enables or disables refresh control. 1: Refresh control enabled

- Refresh timer counter (RTCNT) Number of bits: 8 Address: H'FFFDA8

  Description: RTCNT counts up on the internal clock selected by bits RTCS2 to RTCK0 in REFCR. When the RTCNT value matches the RTCOR value (compare match), the CMF flag in REFCR is set to 1 and RTCNT is cleared to H'00. At this time, when the RFSHE bit in REFCR is 1, a refresh cycle is generated.

  Setting Value: H'00

- Refresh time constant register (RTCOR) Number of bits: 8 Address: H'FFFDA9

  Description: RTCOR specifies intervals at which a compare match for RTCOR and RTCNT is generated. The RTCOR value is always compared with the RTCNT value. When they match, the CMF flag in REFCR is set to 1 and RTCNT is cleared to H'00.

  Setting Value: H'30 (Refresh intervals: approx. 15.36 μs)

- Port function control register 0 (PFCR0) Number of bits: 8 Address: H'FFFBC0

Bit	Bit Name	Setting Value	R/W	Description
4	CS4E	1	R/W	CS7 to CS0 Enable
2	CS2E	1		Enable/disable the corresponding $\overline{CS}$ output. 1: Pin functions as $\overline{CS}$ output pin

- Port function control register 1 (PFCR1) Number of bits: 8 Address: H'FFFBC1

Bit	Bit Name	Setting Value	R/W	Description
1	CS4SA	0	R/W	$\overline{CS4}$ Output Pin Select
0	CS4SB	0		Select the output pin for $\overline{CS4}$ when $\overline{CS4}$ output is enabled (CS4E = 1) 00: Specifies pin PB0 as $\overline{CS4}$-A output

- Port function control register 2 (PFCR2) Number of bits: 8 Address: H'FFFBC2

Bit	Bit Name	Setting Value	R/W	Description
6	CS2S	1	R/W	$\overline{CS2}$ Output Pin Select Selects the output pin for $\overline{CS2}$ when $\overline{CS2}$ output is enabled (CS2E = 1). 1: Specifies pin PB1 as $\overline{CS2}$-B output

- Port function control register 4 (PFCR4) Number of bits: 8 Address: H'FFFBC4

Bit	Bit Name	Setting Value	R/W	Description
7 to 0	A23E to A16E	1	R/W	Address A23 to A16 Enable Enable/disable the address output (A23 to A16). 1: Enables the A23 to A16 output

- Port function control register 8 (PFCR8) Number of bits: 8 Address: H'FFFBC8

Bit	Bit Name	Setting Value	R/W	Description
1	EDMAS0A	0	R/W	EXDMAC Control Pin Select
0	EDMAS0B	0		Select the I/O port to control EXDMAC_0. 00: Specify pins P10 to P13 as EXDMAC control pin

- Data direction register (P2DDR) Number of bits: 8 Address: H'FFFB81
- Data direction register (P3DDR) Number of bits: 8 Address: H'FFFB82
- Data direction register (PDDDR) Number of bits: 8 Address: H'FFFB8A
- Data direction register (PEDDR) Number of bits: 8 Address: H'FFFB8D
- Data direction register (PFDDR) Number of bits: 8 Address: H'FFFB8E

  Description: DDR is an 8-bit write-only register that specifies a port I/O for each bit.
  Setting value: H'FF

- Data register (P3DR) Number of bits: 8 Address: H'FFFF52

  Description: DR is an 8-bit readable/writable register that stores output data of the pins to be used as the general output port.
  Setting value: H'FF

- Input buffer control register (P1ICR) Number of bits: 8 Address: H'FFFB90

  Description: ICR is an 8-bit readable/writable register that controls the port input buffers.
  Setting value: H'01
  Note: This value is set to H'01 to use the $\overline{\text{EDREQ}}$ pin as the input pin.

- EXDMA source address register (EDSAR) Number of bits: 32 Address: H'FFFC80

  Description: EDSAR is a 32-bit readable/writable register that specifies the transfer source address. An address update function is provided that updates the register contents to the next transfer source address each time transfer processing is performed.
  Setting value: the start address of area 2.

- EXDMA destination address register (EDDAR) Number of bits: 32 Address: H'FFFC84

  Description: EDDAR is a 32-bit readable/writable register that specifies the transfer destination address. An address update function is provided that updates the register contents to the next transfer destination address each time transfer processing is performed.
  Setting value: the start address of area 4

- EXDMA transfer count register (EDTCR) Number of bits: 32 Address: H'FFFC8C

  Description: EDTCR is a 32-bit readable/writable register that specifies the size of data to be transferred (total transfer size). The value according to the data access size is decremented every data transfer.

  Setting value: H'100

- EXDMA mode control register (EDMDR) Number of bits: 32 Address: H'FFFC94

Bit	Bit Name	Setting Value	R/W	Description
31	DTE	0	R/W	Data Transfer Enable Enables or disables data transfer on the corresponding channel. 0: Data transfer disabled
27	EDREQS	1	R/W	$\overline{\text{EDREQ}}$ select Selects whether low level or falling edge detection of the $\overline{\text{EDREQ}}$ signal is used in external request mode. 1: Falling edge detection (the first transfer is detected on a low level after a transfer is enabled.)
15 14	DTSZ1 DTSZ0	0 0	R/W	Data Access Size 1 and 0 Select the data access size for a transfer. 00: Byte-size (8 bits)
13 12	MDS1 MDS0	0 0	R/W	Transfer Mode Select 1 and 0 Select the transfer mode. 00: Normal transfer mode
8	DTIE	0	R/W	Data Transfer Interrupt Enable Enables or disables a transfer end interrupt request by the transfer counter. 0: Transfer end interrupt request disabled
7 6	DTF1 DTF0	1 1	R/W	Data Transfer Factor 1 and 0 Select a source to activate EXDMAC. 11: External request
2 1 0	EDMAP2 EDMAP1 EDMAP0	1 1 1	R/W	EXDMA Priority Levels 2 to 0 Select the EXDMAC priority level to determine the priority over CPU. 111: Priority level 7 (highest)

- EXDMA address control register (EDACR) Number of bits: 32 Address: H'FFFC98

Bit	Bit Name	Setting Value	R/W	Description
31	AMS	0	R/W	Address Mode Select Selects single address mode or dual address mode. 0: Dual address mode
21	SAT1	1	R/W	Source Address Update Mode 1 and 0
20	SAT0	0		Specify incrementing/decrementing of the transfer source address (EDSAR). 10: Incremented
17	DAT1	1	R/W	Destination Address Update Mode 1 and 0
16	DAT0	0		Specify incrementing/decrementing of the transfer destination address (EDDAR). 10: Incremented
12	SARA4	0	R/W	Source Address Extended Repeat Area
11	SARA3	0		Specify the extended repeat area on the transfer source
10	SARA2	0		address register (EDSAR). With the extended repeat area, the
9	SARA1	1		specified lower address bits are updated and the remaining
8	SARA0	1		upper address bits are fixed. 00011: The three lower-order bits (for 8 bytes) of transfer source address are specified as the extended repeat area.

- Timer control register (TCR) Number of bits: 8 Address: H'FFFFC0

Bit	Bit Name	Setting Value	R/W	Description
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0		Select the TCNT counter clearing source.
5	CCLR0	1		001: TCNT cleared by TGRA compare match/input capture
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0		Select the input clock edge. 00: Counted at an internal clock falling edge
2	TPSC2	0	R/W	Timer Prescaler 2 to 0
1	TPSC1	0		Select the TCNT counter clock.
0	TPSC0	0		000: Counts on internal clock Pϕ/1

- Timer I/O control register _H (TIOR_H) Number of bits: 8 Address: H'FFFFC2

Bit	Bit Name	Setting Value	R/W	Description
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	1		Specify the function of TGRA.
1	IOA1	1		0111 TIOCA0 pin initial value is 1. Toggle output at compare
0	IOA0	1		match.

- Timer interrupt enable register (TIER) Number of bits: 8 Address: H'FFFFC4

Bit	Bit Name	Setting Value	R/W	Description
0	TGIEA	0	R/W	TGR Interrupt Enable A Enables/disables interrupt requests (TGIA) by the TGFA bit when the TGFA bit in TSR is set to 1. 0: Interrupt requests (TGIA) by TGFA bit disabled

- Timer counter (TCNT) Number of bits: 16 Address: H'FFFFC6
  Description: TCNT is a 16-bit readable/writable counter.
  TCNT is initialized to H'0000 by a reset or in hardware standby mode.
  Setting Value: H'0000

- Timer general register (TGR) Number of bits: 16 Address: H'FFFFC8
  Description: TGR is a 16-bit readable/writable register for use in output compare and input capture.
  Setting Value: H'0025 (TPU period: approx. 1.5 µs)

- Timer start register (TSTR) Number of bits: 8 Address: H'FFFFBC

Bit	Bit Name	Setting Value	R/W	Description
0	CST0	0	R/W	Counter Start 0 Selects operation or stoppage for TCNT. 0: TCNT_0 count operation is stopped

5. Flowchart

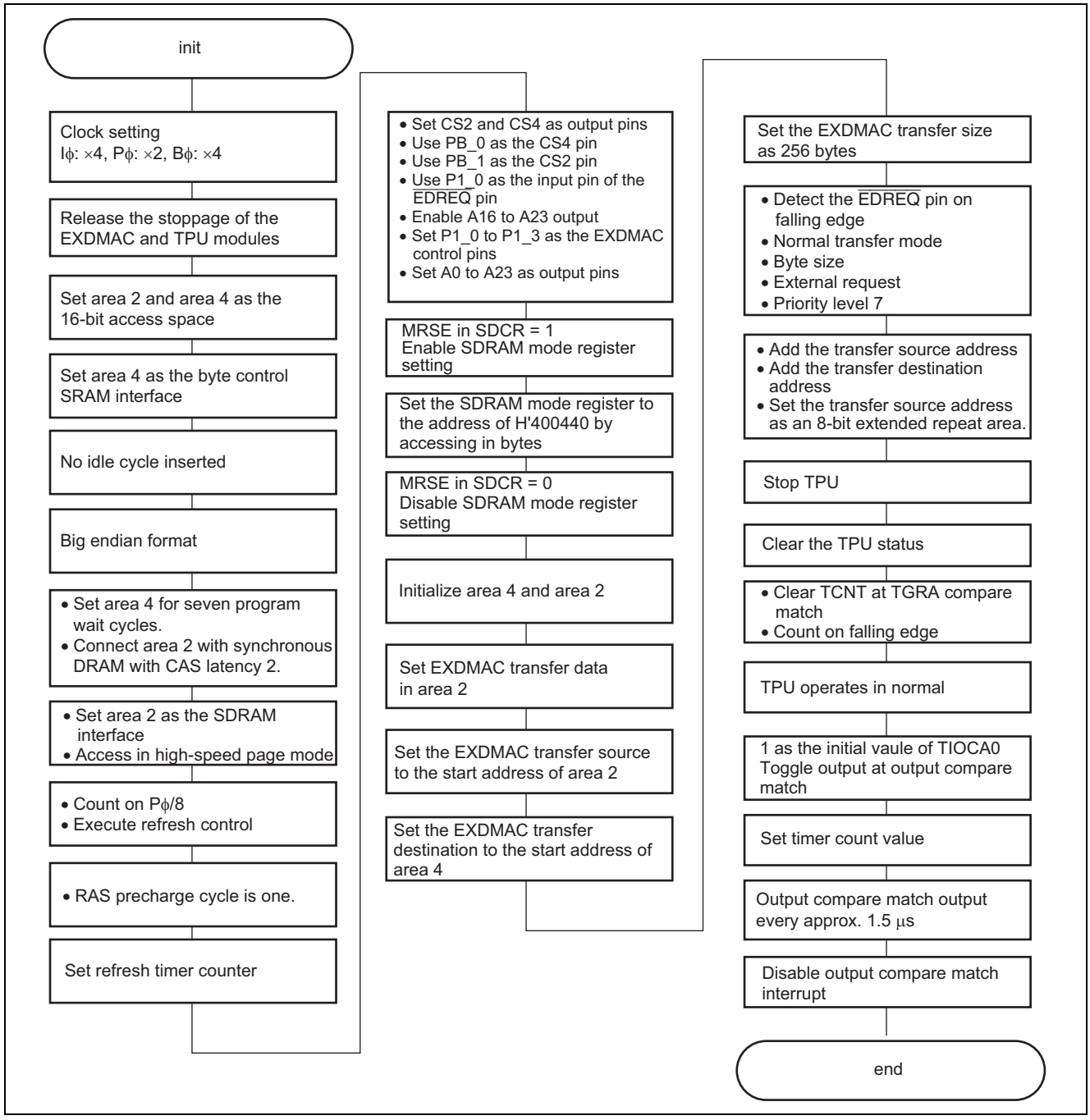

Figure 9 Flowchart (init)

5.2.3 cmp_data Function

1. Functional overview
   The cmp_data function compares the transfer source data with the transfer destination data and outputs the result to a port.
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- EXDMA mode control register (EDMDR) Number of bits: 32 Address: H' 'FFFC94

Bit	Bit Name	Setting Value	R/W	Description
16	DTIF	0	R/W	Data Transfer Interrupt Flag Flag indicating that a transfer end interrupt request has occurred by the transfer counter. 0: Transfer end interrupt request is not generated by the transfer counter

- Timer start register (TSTR) Number of bits: 8 Address: H'FFFFBC

Bit	Bit Name	Setting Value	R/W	Description
0	CST0	0	R/W	Counter Start 0 Selects operation or stoppage for TCNT. 0: TCNT_0 count operation is stopped

- Data Register (P3DR) Number of bits: 8 Address: H'FFFF52
  Description: DR is an 8-bit readable/writable register that stores output data of the pins to be used as the general output port.
  Setting Value: H'55, H'FF

5. Flowchart

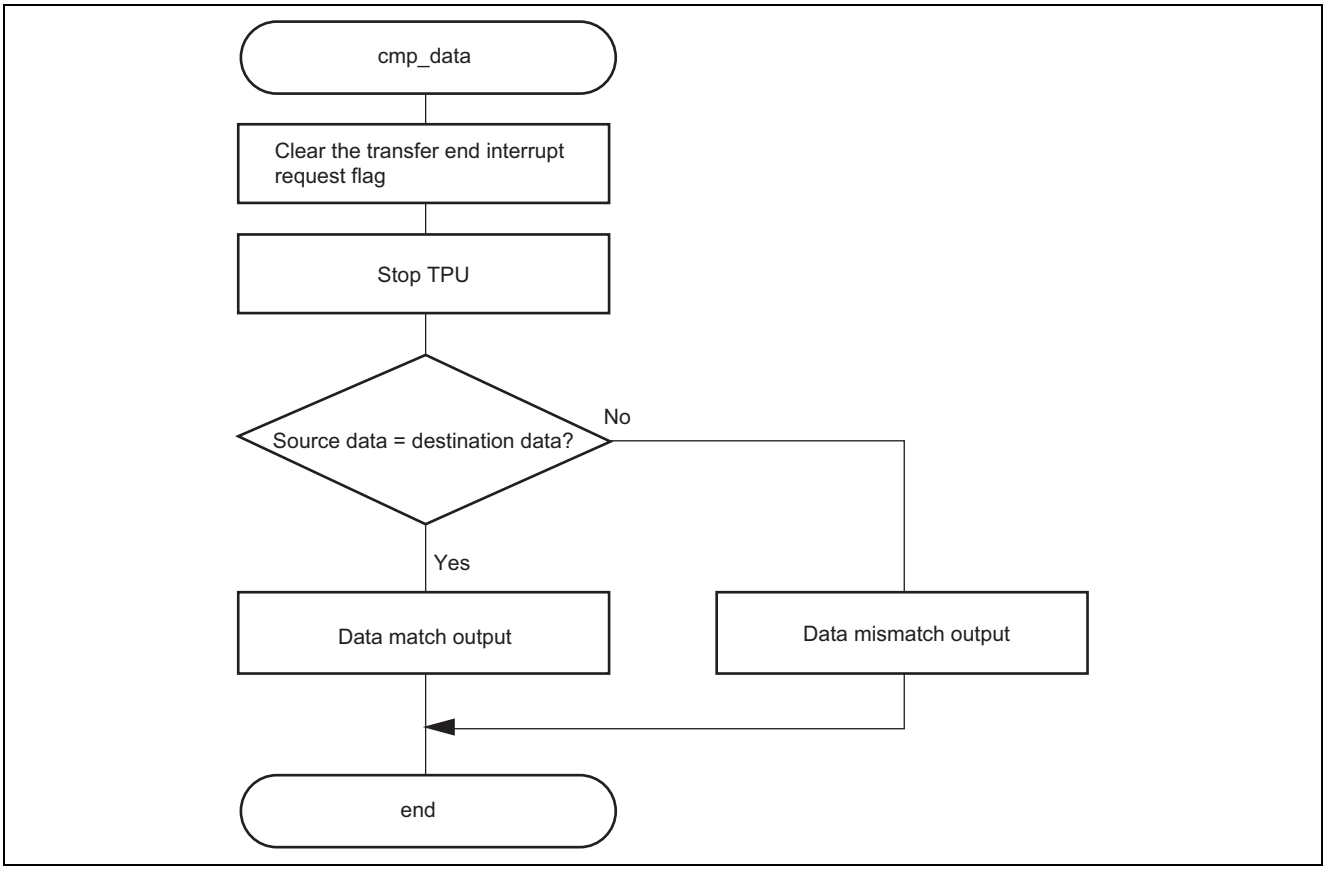

Figure 10 Flowchart (cmp_data)

6. Precautions

1. When pins of the device are used as the input pins of peripheral module, the corresponding bit in the input buffer control register (PnICR) is set to 1.
   For details, refer to the following appropriate hardware manual.
2. Interrupt requests from the on-chip peripheral modules cannot be used as the sources of EXDMAC activation.
   For details, refer to the following appropriate hardware manual.

7. Documents for Reference

- Hardware Manual
  H8SX/1668R Group Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Technical News and Technical Updates
  The most up-to-date information is available on the Renesas Technology Website.
- H8SX Family Application Note
  Synchronous DRAM Interface: document No. REJ06B0659-0200
  The most up-to-date version of this document is available on the Renesas Technology Website.

Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	May.20.08	—	First edition issued

Notes regarding these materials

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (http://www.renesas.com)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guaranties regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
   (1) artificial life support devices or systems
   (2) surgical implantations
   (3) healthcare intervention (e.g., excision, administration of medication, etc.)
   (4) any other purposes that pose a direct threat to human life

   Renesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.